DATA SHEET

N4891A

400GBASE FEC-aware Receiver Test

Keysight's N4891A 400GBASE FEC-aware receiver test solution allows measuring frame loss ratio in 400G Ethernet links using FEC by supplying one stressed lane, while maintaining the proper FEC striped test pattern data across all lanes. This solution provides unique insights to understand how component and system design tradeoffs are affected by Forward Error Correction (FEC) requirements and to predict the system margin under real conditions

KEYSIGHT TECHNOLOGIES

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400GbE is revolutionary not evolutionary

The steadily increasing demand for more computing power and bandwidth fueled by cloud applications has accelerated the deployment of higher speed interfaces in datacenters. The move from NRZ-based 100G interfaces to PAM4-based 400G interfaces is revolutionary, rather than evolutionary: New technologies such as linear broadband amplifiers and drivers as well as adaptive digital equalizers have become a mandatory part of the design but are not sufficient to ensure error-free operation. 400G links typically operate at rather high intrinsic bit error rates (BER) and forward error correction (FEC) is therefore required.

The combination of adaptive equalization and FEC has drastically increased the level of complexity in the characterization and validation of silicon devices, application-specific integrated circuits (ASICs), fiber and copper interconnects, optical transceivers, and the port electronics of switches and routers. Identifying potential performance and interoperability issues at an early stage is critical as answers are complex and time-consuming to solve.

FEC proofed Designs

The combination of adaptive digital equalizers combined with forward error correction has drastically increased the level of complexity for the design, characterization and validation process of 400GE components and interfaces.

Testing FEC-enabled links

The IEEE 400GBASE standard clauses require the use of the Reed-Solomon code RS (544,514), also known as KP4, to ensure error-free operation. When bit errors are randomly distributed, the system margin and resulting Frame Loss Ratio (FLR) can be easily derived from the pre-FEC BER. However, besides jitter mechanisms and pattern-dependent effects (like inter-symbol interference, ISI), adaptive Decision Feedback Equalizer (DFE) which are necessary to cancel impact of reflection in the links are a major source of error bursts, which can exceed the error correction capability of the FEC, resulting in loss of the entire FEC code word – several thousands of bits of lost data. As such effects have a direct impact on interoperability, 400G Ethernet standards compliance tests for electrical and optical interface require meeting both a conventional BER limit, as well as a Frame Loss Ratio (FLR) measurement.

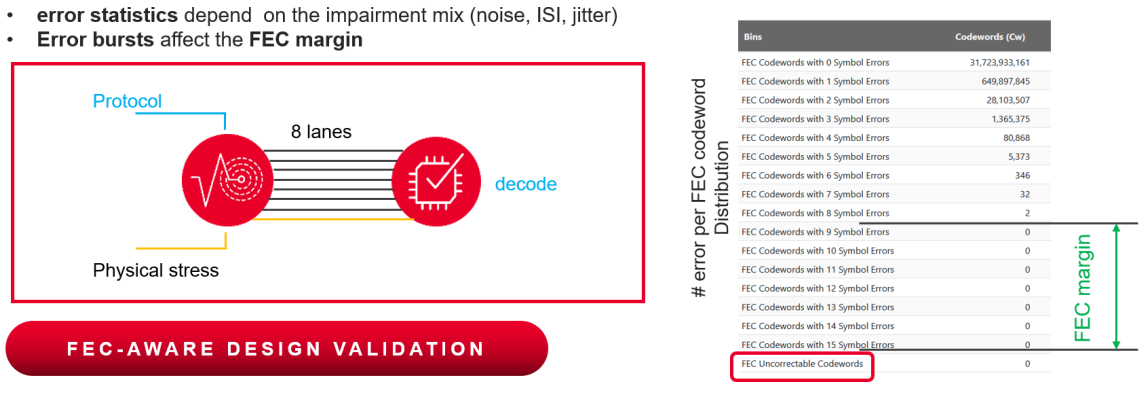

Figure 1. Principle of 400GAUI-8 FEC-aware layer 1 testing.

N4891A FEC-aware Receiver Test Solution

The N4891A is a flexible solution designed to test PAM4-based 50G, 100G, 200G and 400G host ASICs and transceiver modules requiring a loopback to an error analyzer. The table below provides a high-level overview of the N4891A solution capabilities compared to a classical BERT system and a protocol analyzer.

Applications	Protocol tester	Bit Error Tester	N4891A Solution
Layer 1 functional test	✓	✓	✓
Layer 2,3 functional test	✓	-	-
Performance characterization	-	✓	✓
Layer 1 - FLR and FEC margin measurements	✓	-	✓
BER measurements under stress condition as defined by IEEE 802.3	-	✓	✓
FLR and FEC margin measurements under stress condition as defined by IEEE 802.3	-	-	✓

Overview

Standard compliance tests are performed by stressing one lane at the time, with all other lanes carrying traffic. This is a challenge when coping with the KP4 FEC encoding, which is distributed over all lanes (*FEC-striping*). N4891A combines the M8040A 64 Gbaud high performance BERT to generate the correct striped FEC test pattern on the single lane under test, along with a N4891A-00x 2- or 4-port 400GE Layer 1 BERT QSFP-DD test system to provide the proper aligned striped FEC traffic on the other 7 lanes enabling it to measure the FLR of the tested interface under stress conditions. This test method is prescribed in the IEEE 802.3 standard clauses 121,122, 124 and 138, 139,140 (802.3bs and 802.3cd respectively).

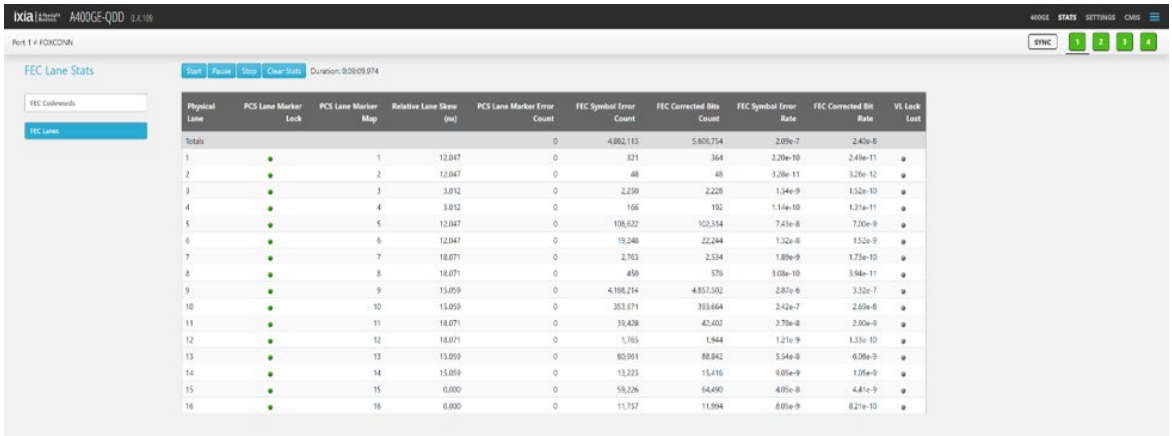

Figure 2. PCS lanes statistics in 400GE KP4 mode view

For compliance testing, the lane under stress of the device under test (DUT) can be calibrated with compliance test applications *software* such as *IEEE 802.3bs M8091BSPA Receiver Test Pre-Compliance Application* or *M809256PB OIF-CEI CEI-56G Receiver Test Application*. For this, additional equipment such as a sampling oscilloscope or an interference source may be needed. For detailed information, please refer to the documentation of above-mentioned *software*. The DUT is then connected in loopback mode using a breakout cable to one of the QSFP-DD port for FEC decoding.

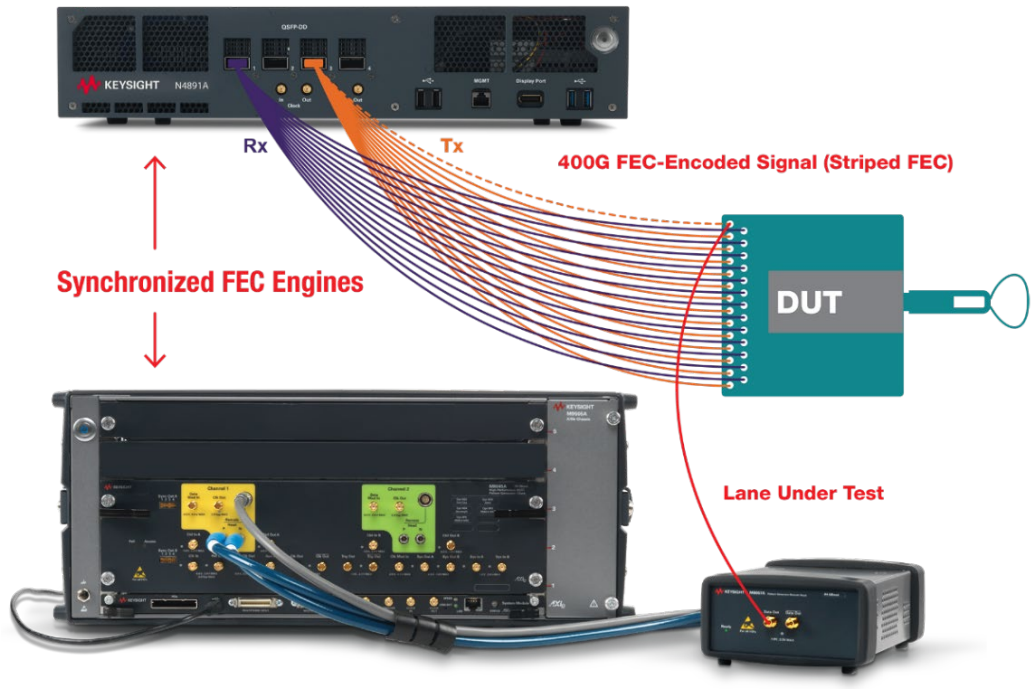

Figure 3. Example setup for a FEC-aware standard-compliant electrical receiver test.

The inferred FEC feature (N4891A-BRT option) is an alternative to real-time FEC encoding / decoding (N4891A-KP4/SYC option). Here FEC performance are estimated from PRBS error statistics analyzed and updated in real time. The impact of striping can be taken into account.

Optionally individual lanes can be looped back to an M8046A error analyzer for detailed characterization of the error mechanisms (burst errors visualization, error distance diagram).

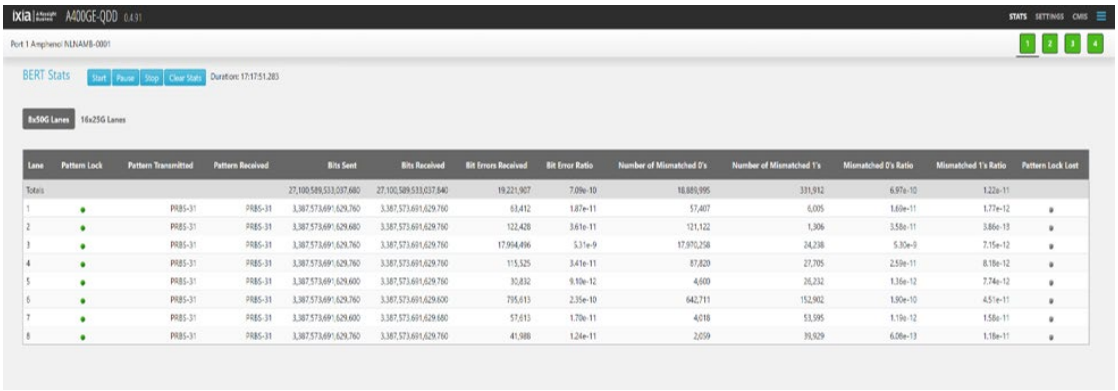

Figure 4. 400GAUI-8 lanes statistics in PRBS mode view.

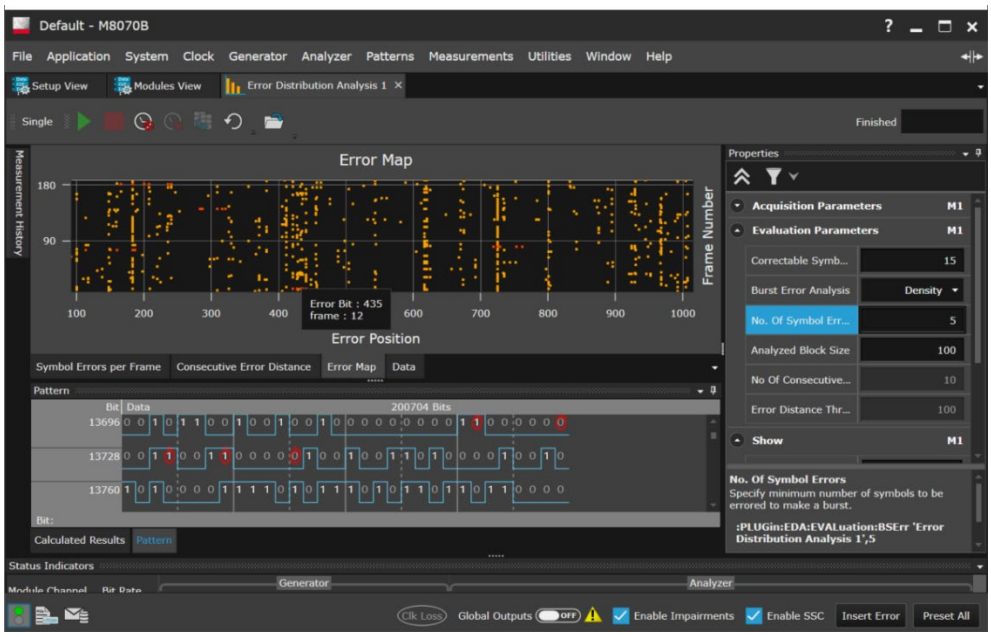

Figure 5. Error Analysis of individual lanes using the M8046A error analyzer (M8070EDAB), providing signature of different error mechanisms (pattern-dependent, burst).

This solution also provides the unique capability to measure FLR and FEC margin of optical transceiver module under optical receiver stress test condition. For this purpose, the optical lane under stress is calibrated using a M8040A-based *N4917BSCB 400G Optical Receiver Stress Test Application software*. The FEC performance can be characterized for different combination of optical transmitter impairments such as inter-symbol-interference, optical noise, jitter, or cross-talk.

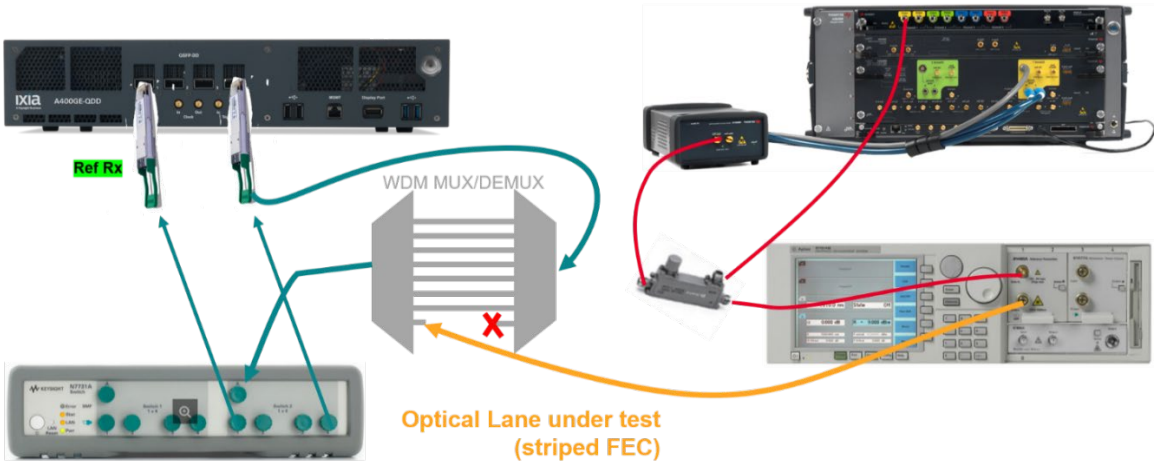

Figure 6. Example setup for a FEC-aware optical Receiver Stress test consisting of a A400GE-QDD multiport test system, a M8040A BERT, an 81491A reference transmitter and an N7731A optical switch

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Features & supported standards

The N4891A solutions generates eight 26.5625 Gbaud PAM4 tributaries according to 50GAUI-1, 100GAUI-2, 200GAUI-4 and 400GAUI-8 recommendations. Interferences can be added on one electrical lane.

Adjustable parameters for the stressed lane

- Data Amplitude (from 100mV to 1.8V pp differential)
- Jitter type (sinusoidal, random, Bounded uncorrelated)
- Periodic jitter frequency (Hz) and amplitude (UI)
- De-emphasis coefficients (2 pre, 2 post)
- Pattern: PRBS, memory pattern and FEC encoded scrambled idle for following interfaces:
  - 50GBASE-R (PCS 0&1),
  - 100GBASE-R (PCS 0-9 on first channel and PCS 10-19 on 2nd channel)
  - 100GBASE-R (PCS 0-19 on the first channel at a 53Gbaud PAM4 coding)
  - 200GASE-R (PCS 0&1)
  - 400GASE-R (PCS 0&1)
- Additional parameters such as Sinusoidal interferer to Gaussian noise ratio, Eye width/height and can be controlled using the N4917BSCB and M809256PB and M8091BSPA compliance application software

Adjustable parameters for aggressor lanes

- Data Amplitude (from 250mV to 1025mV pp differential)
- De-emphasis (2 pre, 1 post)
- Pattern: 50GE-FEC, 100GE-FEC, 200GE-FEC, 400GE-FEC codewords with scrambled idle, PRBS31Q, PRBS23Q, PRBS20Q, PRBS15Q, PRBS13Q, PRBS11Q, PRBS9Q and PRBS7Q, SSPRQ
- Adjustable frequency range of +/- 100 ppm

Measurements

- FEC mode
  - Per lane PCS and FEC statistics
  - PCS lane marker lock & marker map
  - FEC port statistics with count and rate
  - FEC symbol bit error distribution analysis statistics
- PRBS mode
  - Per lane BER statistics
  - Pattern re-lock
- Enhanced BERT mode
  - Verbose error stats
  - Inferred FEC performance
  - Burst error stats

The list of currently supported test procedures recommendation as well as planed extensions to the solution can be found in the table below.

Interface	Type of Test	Companion Solution	Availability
Electrical Receiver Test			
400GAUI-8	the OIF-CEI-04.0 Common Electrical I/O (CEI), Clauses 16, 17 and 21 and IEEE 802.3 and Annex 120E, 135G	M809256PB[1] M8091BSPA[2]	Yes
200GAUI-4			
100GAUI-2			
50GAUI-1			
Optical Receiver Stress Test			
400GBASE-LR8/-FR8	IEEE 802.3 clauses 121,122,124,138,139 & 140	N4917BSCB[3]	Yes
400GBASE-DR4 400G-FR4/LR4[4]			Please contact Keysight
200GBASE-DR4/-LR4/ER4			
100GBASE-DR			Yes
50GBASE-DR/-SR/-			Yes
400GBASE-SR8 400G-BiDi [5]	IEEE 802.3.cm		Yes

1 IEEE 802.3bs Receiver Test Pre-Compliance Application
2 M809256PB OIF-CEI CEI-56G Receiver Test Application
3 N4917BSCB Optical Receiver Stress Test
4 100G Lambda Multi-Source Agreement
5 400G BiDi Multi-Source Agreement

N4891A Requirements

The software components of the N4891A solution run on an external PC or on M9537A embedded controller.

PC hardware requirements

- Operating system: Microsoft Windows 7, Windows 8, Windows 10, (64 bit)
- Memory: 8 GB RAM minimum
- Monitor resolution: WXGA+ (1440 x 900) minimum

PC installed software requirements

- Keysight IO Libraries Suite rev. 17.3x or later
- M8070B system software for M8000 Series, version 6.7.500 or later
- M8070ADVB Advanced Measurement Package for M8000 Series of BERT Test Solutions, version 1.1.550.2 or later

PC interfaces

- USB 2.0 or higher, LAN
- Monitor with Display-Port

Instrument firmware requirements

- M8040A BERT: M8070B system software as above
- N4891A/A400GE-QDD: KiOS version 3.0 or above

Configuration Guide

The N4891A 400GBASE FEC-aware receiver test solution is built up from various instruments and software. This configuration guide is designed to help you determine the best configuration for your needs. The options marked * are recommended but not mandatory.

Select the configuration for the M8040A 64 Gbaud high-performance BERT

Step 1. BERT chassis configuration	
M8040A	High-performance BERT 64 Gbaud
M8040A-BU2	M9505A 5-slot AXIe chassis with USB option, (requires external PC with USB connection)
Step 2. BERT module minimum required configuration	
M8045A	Pattern generator and clock module 32/64 Gbaud, 3 slot AXIe
M8045A-G32	Pattern generator one channel NRZ, data rate up to 32 Gbaud
M8045A-0G9	Forward Error Correction (FEC) Encoding, Module-wide License
M8045A-0P3	PAM-4 encoding up to 32 Gbaud, module-wide license
M8045A-0G3*	Advanced jitter sources for receiver characterization, license
M8045A-0G4	De-emphasis, module-wide license
M8045A-801	Short cable 1.85 mm (m) to 1.85 mm (m), 0.15 m, absolute matching 699 ps ± 1 ps, Qty 2 recommended
M8057A/B	Remote head for M8045A pattern generator, 1 channel
Step 3. Single Lane Error Detector (optional)	
M8046A*	Analyzer module, 32/64 Gbaud, 1-slot AXIe
M8046A-A32*	Analyzer, one channel, data rate up to 32 Gbaud, NRZ
M8046A-0A4 *	Clock recovery for 32 Gbaud, license
M8046A-0P3*	PAM-4 decoding up to 32 Gbaud, license
Step 4. M8000 system software configuration	
M8070B	System software for M8000 Series of BER test solutions
M8070ADVB-1xx	Advanced Measurement Package for M8000 Series of BERT Test Solutions (node-locked, transportable, floating or USB license)
M8070EDAB-1xx*	Error Distribution Analysis Package for M8000 Series BER Test Solutions (node-locked, transportable, floating or USB license) - only in combination with M8046A

Select the configuration for the A400GE-QDD 400GE layer 1 BERT and KP4 FEC multiport test system

Step 5. Select one configuration	
N4891A-002/KP4/SYC	2-port 400GE Layer 1 BERT QSFP-DD test system with KP4 FEC option and synchronized to M8040A option
N4891A-004/KP4/SYC	4-port 400GE Layer 1 BERT QSFP-DD test system with KP4 FEC option and synchronized to M8040A option
N4891A-002/BRT	2-port 400GE Layer 1 BERT QSFP-DD test system with Enhanced BERT option
N4891A-004/BRT	4-port 400GE Layer 1 BERT QSFP-DD test system with Enhanced BERT option

Select the accessories components of the solution (either bundle or individual RF accessories)

Step 6. Bundles incl. QSFP-DD module control board & breakout adapter	
N4891A-810	QSFP-DD 400G HCB Tx Test Adapter
N4891A-811	QSFP-DD 400G HCB Rx Test Adapter
N4891A-820	QSFP-DD 400G MCB Receptable, HCB Tx Test Adapter
Step 7. RF adaptors, cables for clock / trigger connection	
M8041A-801	2.92 mm Matched Cable Pair for M8000 Series (optional)
M8045A-801	External DUT Cable (2 required)
15442A	cable with Male SMA connectors for clock and trigger connection between M8040A and 400GE Layer 1 BERT QSFP-DD test system (2 required)
83059A	Coaxial Adapter, 3.5mm Male-Male, HCB-Tx to MCB connection (16 required)
11901D	2.4mm female to APC-3.5mm male adapter, M8040A to MCB connection (4 required)
M8195A-820	Termination 50 Ohm, 26.5GHz
Step 8. Power Supply (power requirements depend on the device under test)	
E3632A	DC power supply. single output, dual range: 0-15V, 7A; 0-30V, 4A 105/120W. GPIB
E36313A	DC power supply, triple-output, 6 V, 10 A and 2 x 25 V, 2 A, 160 W: LAN, USB
E36102B	DC power supply, single-output, 6 V, 5 A, 30 W

Recommended Software

Step 9. Automated Stress Signal calibration	
N4917BSCB-1xx*	Optical Receiver Stress Test compliance app single mode 200G and 400G IEEE (node-locked, transportable, floating or USB license)
M809256PB-1xx*	OIF-CEI CEI-56G Receiver Test Application (node-locked, transportable, floating or USB license)

Example connection diagrams

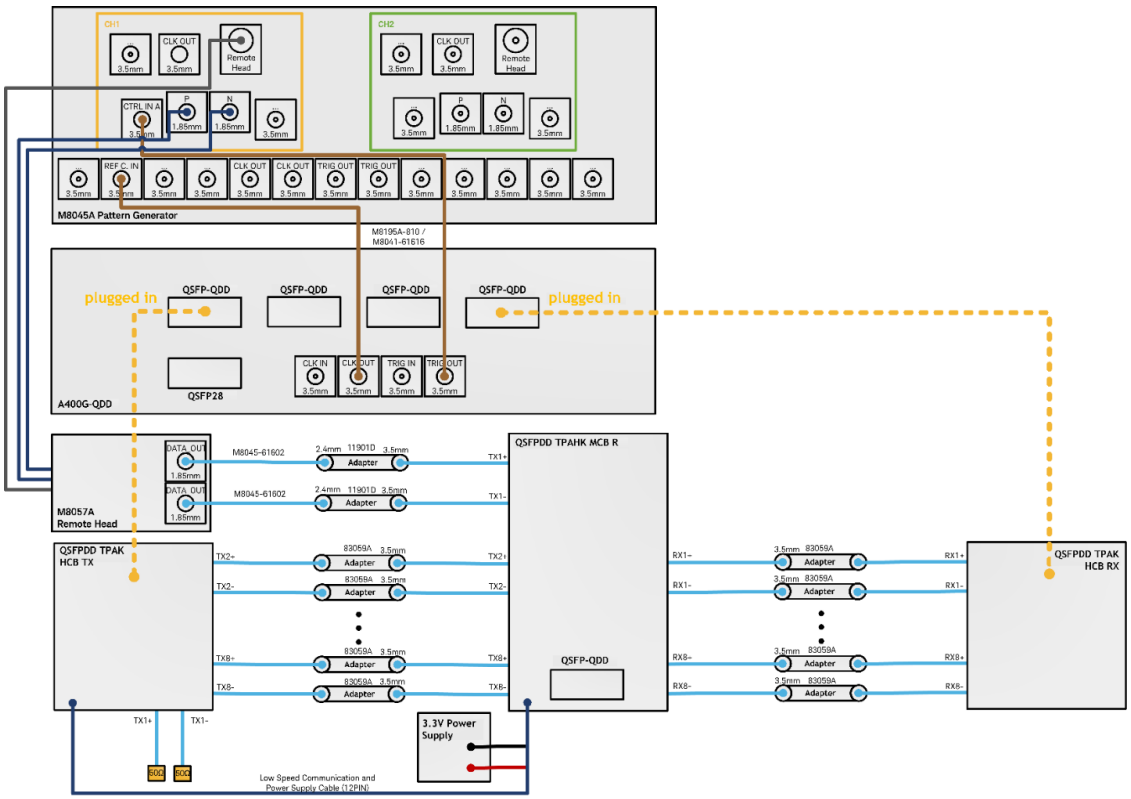

Figure 7. Connection diagram for testing the electrical Rx of an optical transceiver module with 400GAUI-8 interface (with loopback to error detector through HCB-Rx adapter).

Conclusion

Keysight's N4891A 400GBASE FEC-aware receiver test solution allows measurement of frame loss ratio in 400G Ethernet links using FEC by supplying one stressed lane, while maintaining the proper FEC striped test pattern data across all lanes. The test method is prescribed in the IEEE 802.3 standard clauses 121,122,123, 124, 138, 139,140 and Annex 120E and 135G (802.3bs and 802.3cd respectively). This solution provides unique insights to understand how component and system design tradeoffs are affected by Forward Error Correction (FEC) requirements and to predict the system margin under real conditions.

Related literature

- N4891A User Guide, N4891-90119
- M8040A datasheet, 5992-1525EN
- A400GE-QDD data sheet, product page
- M809256PB datasheet, 5992-4334EN
- M8091BSPA datasheet, 5992-3288EN
- N4917BSCB datasheet, 5992-4040EN
- Forward Error Correction Solutions - ABCs of Bit Error Rate Testers - White Paper, 5992-3454EN
- 400GE FEC Encode/Decode Processing, 5992-3405EN

More information

www.keysight.com/find/FEC-RX-Test

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