Errata

Title & Document Type: **5344S Microwave Source Synchronizer Operating and Service Manual**

Manual Part Number: **05344-90009**

Revision Date: **September 1983**

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HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, life sciences, and chemical analysis businesses are now part of Agilent Technologies. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A. We have made no changes to this manual copy.

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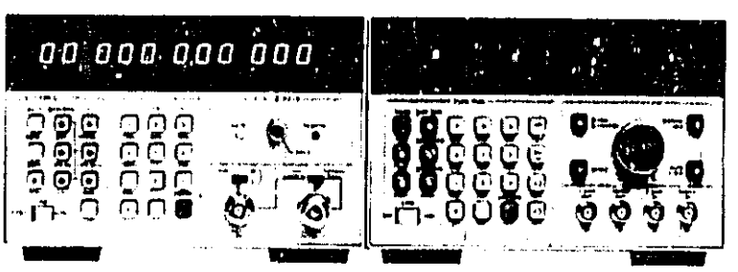
Agilent Technologies

OPERATING AND SERVICE MANUAL

HP-IB SYSTEMS

5344S

Microwave Source Synchronizer



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Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

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HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

5344S
Microwave Source Synchronizer

SERIAL PREFIX: 2314A

This manual applies to Serial Prefix 2314A, unless accompanied by a Manual Change Sheet indicating otherwise.

5301 STEVENS CREEK BOULEVARD, SANTA CLARA, CA 95050

MANUAL PART NUMBER 05344-90009
Microfiche Part Number 05344-90010
Operating Information Supplement Part Number 05344-90011

Printed: SEPTEMBER 1983

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SAFETY CONSIDERATIONS

GENERAL

This is a Safety Class I instrument. This instrument has been designed and tested according to IEC Publication 348, "Safety Requirements for Electronic Measuring Apparatus".

This manual contains information, cautions, and warnings which must be followed by the service person to ensure safe operation and to retain the instrument in safe condition.

WARNINGS

SAFETY

If this instrument is to be energized via an autotransformer for voltage reduction, make sure the common terminal is connected to the earthed pole of the power source.

BEFORE SWITCHING ON THIS INSTRUMENT, the protective earth terminals of this instrument must be connected to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding).

Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the short-circuiting of fuse holders must be avoided.

Whenever it is likely that the protection offered by fuses has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

GROUNDING

Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal is likely to make this instrument dangerous. Intentional interruption is prohibited.

HIGH VOLTAGE

Warning — These servicing instructions are for use by qualified personnel only. To avoid dangerous electric shock, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so.

CAUTIONS

LINE VOLTAGE SELECTION

BEFORE SWITCHING ON THIS INSTRUMENT, make sure the instrument is set to the voltage of the power source. Verify that the power module is matched to the available line voltage. Verify that the correct fuse is installed.

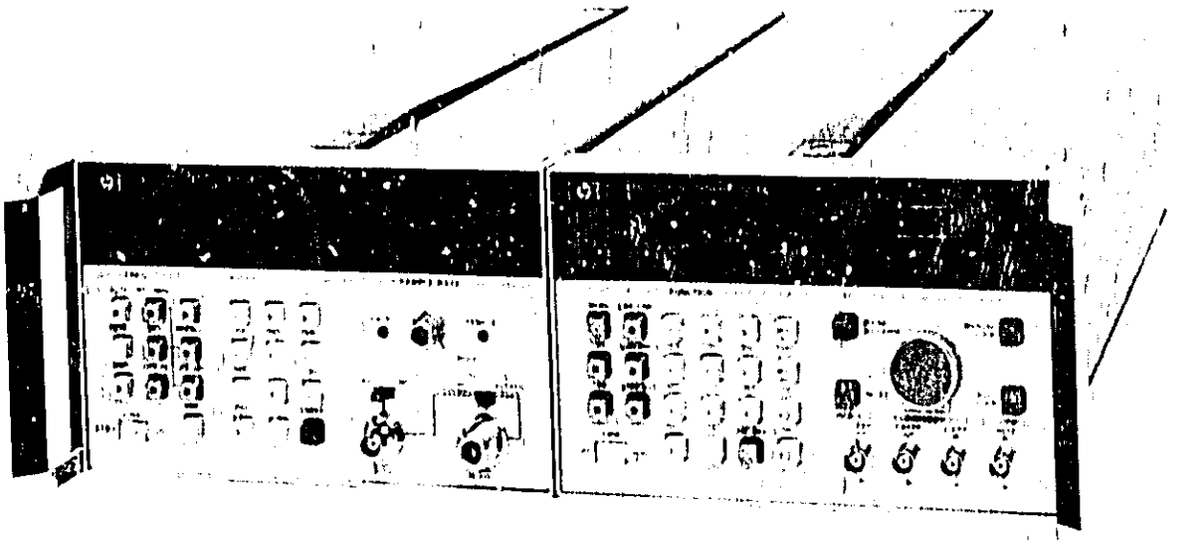
GROUNDING

BEFORE SWITCHING ON THIS INSTRUMENT, ensure that all devices connected to this instrument are connected to the protective (earth) ground. (Grounding one conductor of a two-conductor outlet is not sufficient.)

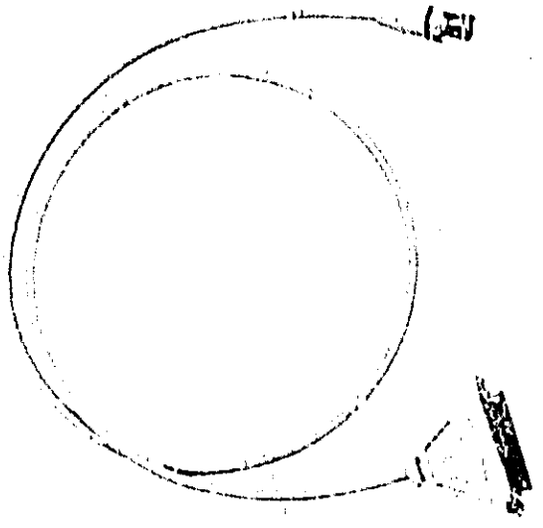
⚠ ATTENTION ⚠

This symbol: ⚠ , which appears on the instrument means: Read the instruction manual before operating the instrument. If the instrument is operated without reading the instructions, it may not operate correctly.

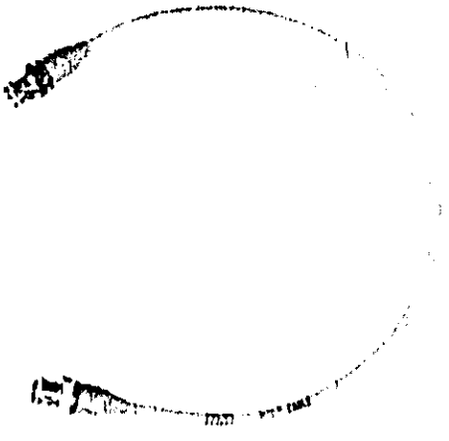
5342A/5344A



5344S SOURCE SYNCHRONIZER



8350A EXTERNAL SWEEP TRIGGER CABLE
Part Number 8120-3545



IF AND 10 MHz 18" BNC-BNC CABLES (2)
Part Number 8120-3370

NOTE: Refer to *Figure 4-1* for cable installation.

Figure 1-1. Model 53445 Source Synchronizer and Equipment Supplied

SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION

1-2. This manual provides information pertaining to the installation, operation, programming, testing, adjustments, and maintenance of the HP Model 5344S Microwave Source Synchronizer, shown in *Figure 1-1*.

1-3. The 5344S is comprised of the 5344A Source Synchronizer and the 5342A Microwave Frequency Counter with an Option 001 High Stability Timebase and Option 001 HP-IB Interface. These two instruments are electrically and mechanically connected at the factory, before shipment. The 5344S Option 043 replaces the 5342A with the 5343A (26.5 GHz) Microwave Frequency Counter.

1-4. INSTRUMENTS COVERED BY MANUAL

1-5. This manual covers the operation of the 5344S Microwave Source Synchronizer system and covers the service of the 5344A instrument. The service and specific operation of the 5342A/5343A counter is described in its own Operating and Service Manual. The 5344A has a two-part serial number. The first four digits and the letter comprise the serial number prefix. The last five digits form the sequential suffix that is unique to each instrument. The contents of this manual apply directly to instruments having the same serial number prefix(es) as listed under SERIAL PREFIX on the title page. There is no serial number for the 5344S system, only the individual serial numbers for the instruments (5344A and 5342A/5343A counter).

1-6. An instrument manufactured after the printing of this manual may have a serial prefix that is not listed on the title page. This unlisted serial prefix indicates that the instrument is different from those documented in this manual. The manual for this instrument is supplied with a yellow Manual Changes supplement that contains change information that documents the differences. Older instruments have lower serial prefix numbers and the differences are described in Section VII.

1-7. OPERATING MANUAL

1-8. Packaged with this manual is an Operating Information Supplement. This is a copy of the first three sections of this manual. This supplement should be kept with the instrument for use by the operator. Additional copies of the Operating Information Supplement or the Operating and Service Manual can be ordered through your nearest Hewlett-Packard Sales and Support Office (a list of these offices is provided at the end of the manual.) The part numbers are listed on the title page of this manual.

1-9. SPECIFICATIONS

1-10. The specifications for the 5344S are listed in *Table 1-1*. These specifications are the performance standards or limits against which the 5344S may be tested.

1-11. Also listed on the title page of this manual following the Operating and Service Manual and the Operating Information Supplement part numbers are the Microfiche part numbers for these publications. These numbers can be used to order 4- X 6-inch microfilm transparencies of these publications. The Microfiche package includes the latest Manual Changes supplement and all pertinent Service Notes.

Table 1-1. Model 5344A Specifications

INPUT CHARACTERISTICS

INPUT 1:	5342A 500 MHz – 18 GHz	5343A (5344S Option 043) 500 MHz – 26.5 GHz
Frequency Range:		
Sensitivity:		
500 MHz – 12.4 GHz	-25 dBm	-33 dBm
12.4 GHz – 18.0 GHz	-20 dBm	-28 dBm
18.0 GHz – 26.5 GHz		-23 dBm
Maximum Input:	+7 dBm	+7 dBm
Dynamic Range:		
500 MHz – 12.4 GHz	42 dB	40 dB
12.4 GHz – 18.0 GHz	27 dB	35 dB
18.0 GHz – 26.5 GHz		30 dB
Damage Level:	+25 dBm, peak	+25 dBm, peak
Impedance:	50 ohms, NOMINAL	50 ohms, NOMINAL
Connector:	Precision Type N female	APC 3.5 male with collar (SMA compatible)
SWR:		
500 MHz – 10 GHz	2:1 TYPICAL	2:1 TYPICAL
10 MHz – 18 GHz	3:1 TYPICAL	3:1 TYPICAL
18 MHz – 26.5 GHz		3:1 TYPICAL
Coupling:	DC to load, AC to instrument	DC to load, AC to instrument
FM Tolerance: switch selectable on rear panel. For modulation rates from DC to 10 MHz	Wide: 50 MHz p-p worst case Normal: 20 MHz p-p worst case	Wide: 50 MHz p-p worst case Normal: 20 MHz p-p worst case Narrow: 6 MHz p-p worst case
AM Tolerance:	Any modulation index provided the minimum signal level is not less than the sensitivity specification	
Modes of Operation:	Automatic: Counter automatically acquires and displays highest level signal within sensitivity range Manual: Center frequency entered to within ±40 MHz (TYPICAL) of true value, ±25 MHz (TYPICAL) below 825 MHz	
Acquisition Time: Automatic mode	Normal FM: 540 ms worst case Wide FM: 2.4 s worst case	Narrow FM: 200 ms worst case Normal FM: 540 ms worst case Wide FM: 2.4 s worst case
Manual mode	80 ms after frequency entered	80 ms after frequency entered
Automatic Amplitude Discrimination Automatically measures the largest of all signals present, providing that signal is	6 dB above any signal within 500 MHz, 20 dB above any signal, 500 MHz – 18 GHz	6 dB above any signal within 500 MHz, 20 dB above any signal, 500 MHz – 26.5 GHz

5342A and 5343A (5344S Option 043)

INPUT 2:	TIME BASE:	
Frequency range: 10 Hz to 520 MHz Direct Count **Sensitivity:** 50Ω 10 Hz to 520 MHz 25 mV rms, 1 MΩ 10 Hz to 25 MHz 50 mV rms **Impedance:** Selectable 1 MΩ, ±50 pF or 50Ω NOMINAL **Coupling:** ac **Connector:** Type BNC female **Maximum Input:** 50Ω 3.5 Vrms (+24 dBm) 5 Vdc fuse protected, 1 MΩ 200 Vdc + 5.0 Vrms	**Crystal frequency:** 10 MHz **Stability:** Aging rate: ±5 x 10^{-10}/day after 24 hour warm up Short term: ±1 x 10^{-9} for 1 s avg time Temperature: ±7 x 10^{-9} over the range 0°C to 50°C Line variation: ±1 x 10^{-10} for 10% change from nominal Warm up: ±5 x 10^{-9} of final value 20 minutes after turn on, at 25°C	**Output frequency:** 10 MHz, +2.4V square wave (TTL compatible), 1.5V peak to peak into 50Ω available from rear panel BNC **External time base:** Requires 10 MHz, 3.0V peak to peak (2.4V peak to peak TYPICAL) sine wave or square wave into 1 kΩ via rear panel BNC connector. Switch selects either internal or external time base

GENERAL

Accuracy: ±1 count ±time base error
Resolution: Front panel pushbuttons select 1 Hz to 1 MHz
Residual stability: When counter and source use common timebase or counter uses external higher stability timebase: ±4 x 10^{-11} rms TYPICAL
Display: 11 digit LED display, sectionalized to read GHz, MHz, kHz, and Hz
Self-check: Selected from front panel pushbuttons. Measures 75 MHz for resolution chosen
Frequency offset: Selected from front panel pushbuttons. Displayed frequency is offset by entered value to 1 Hz resolution
Sample rate: Variable from less than 20 ms between measurements to HOLD which holds display indefinitely
IF out: Rear panel BNC connector provides 25 MHz to 125 MHz output of down converted microwave signal

Remote Programming Interface: HP-IB (Hewlett Packard's implementation of IEEE standard 488)
Functions controlled: All front panel functions with the exception of the line switch and 50Ω/1MΩ switch are programmable
Shorthand interface function codes: SH1, AH1, T1, L2, SR1, RL1, PP0, DC1, DT1, C0, E1

5343A Only (5344S Option 043)

Multiply routine: Selected from front panel pushbuttons. Measured frequency is multiplied by any integer up to 99. Then offset can be added or subtracted for y = mx + b result
Totalize: Input 2 can totalize at rate up to 520 MHz. Readout on CRT is controlled by front panel or HP-IB
External trigger: TTL type low level or contact closure to ground (>50 µs TYPICAL) at rear panel SMC male connector (tA) initiates measurements when in sweep mode
Sweep inhibit: TTL type low level from rear panel SMC male connector (tB) inhibits sweeper during counter measurement when in sweep mode
Sweep mode: Selected from front panel pushbutton. Allows interface to appropriate sweeper (e.g. 8350A) for start, stop, and marker frequency measurements

Specifications describe the instrument's warranted performance. TYPICAL or NOMINAL performance characteristics provide useful applications information but are not warranted.

Table 1-1. Model 5344A Specifications (Continued)

SPECIFICATIONS

Frequency Coverage: 500 MHz – 18 GHz
500 MHz – 26.5 GHz (5344S Option 043)

Resolution: 1 Hz

Long-Term Stability: Equal to timebase in counter

Minimum Lock Level:	Standard (5342A)	Option 043 (5343A)
500 MHz – 12.4 GHz	-22 dBm	-30 dBm
12.4 GHz – 18.0 GHz	-19 dBm	-25 dBm
18.0 GHz – 26.5 GHz		-20 dBm

Lock Time (TYPICAL): Dependent on source
Typical times with 8350A/83592A source

Manual Lock: 900 ms
Auto Lock: 1.5 s
} Apply to CW or LOCK ROLL modes. For CF, ΔF or START STOP add 300 ms

Option 043: All lock times reduced by 400 ms

Accuracy (CW): Equal to counter accuracy

Capture Range† (Manual Mode):

CW or LOCK/ROLL (start frequency): ±25 MHz for sources with FM sensitivity greater or equal to 5 MHz/V. Five volts x FM sensitivity for sources less than 5 MHz/V sensitivity.

CF/ΔF or START/STOP: Above conditions reduced by (0.5) x (span width)

FM Output Connector: Rear panel BNC female

FM Output Drive: ±10 V in series with 250 ohms

Polarity: Automatic selection

Loop Bandwidth: Rear panel switch selectable

Narrowband (NB): 10 kHz TYPICAL
Wideband (WB): 100 kHz TYPICAL

Required Source Characteristics

1. Output frequency and level which meet input specifications for the 5344S
2. An FM input port with a sensitivity between 1 and 50 MHz/V and bandwidth of DC to 2 MHz (minimum) for 5344S wideband mode or DC to 200 kHz (minimum) for narrowband mode
3. Any FM input impedance which will satisfy requirement #2 with a 250 ohm resistance in series with FM input port

Phase Noise — Locked Spectrum:

Dependent on source. Typical values for 8350A/83592A sweeper are:

Single Sideband Phase Noise (1 Hz BW, CW mode, 6 MHz/V, narrowband, F_C = 6 GHz)

Offset from Carrier	10 Hz	100 Hz	1 KHz	10 KHz	100 KHz
SSB Level	-5 dBc	-35 dBc	-45 dBc	-45 dBc	-100 dBc

Operating Characteristics

Instrument Control: Instrument parameters may be set up in three ways. The control knob with coarse and fine modes allows for continuous adjustment of the parameter of interest.

*Auto Lock feature available when 5344S is used with 8350A or 8620C Option 011

†Unless limited by output drive capability

An exact parameter value can be entered through the Data Entry Keyboard. For incrementing or decrementing frequency values, the Step Keys (Step Up/Step Down) can be used. The Step Size is defined by the user.

Bar Meter: A front panel, 10 segment, center scale bar meter indicates the frequency correction signal, from FM OUT connector, being supplied to the signal source.

Operating Modes

CW:

Manual Lock — Source is manually tuned to within capture range of desired frequency. Lock is achieved and is indicated when LOCKED light annunciator turns on. If source frequency is outside capture range, the FREQ HI or FREQ LO light turns on.

Auto Lock* — Source is tuned automatically by the 5344S via the HP-IB to bring it into lock.

Note: Refer to signal source compatibility chart for appropriate source.

CF/ΔF Sweep (Manual Lock or Auto Lock*): Performs a phase continuous locked sweep from CF − 1/2ΔF to CF + 1/2ΔF in a sweep time defined by the user. Sweeps up to 40 MHz are available, dependent on the source. If source is too far from desired frequency range, the user must tune source (Manual Lock) or the 5344S automatically tunes (Auto Lock) via the HP-IB. The LOCKED light indicates a proper locked condition. Marker signals are available within the swept range.

START, STOP Sweep (Manual Lock or Auto Lock*). Performs a phase continuous locked sweep from START frequency to STOP frequency over a sweep time defined by the user. Sweeps up to 40 MHz are available dependent on the source. The STOP frequency must be greater than or equal to START frequency. If the source frequency is too far from the desired frequency range, the user must tune (Manual Lock) source or the 5344S will automatically tune (Auto Lock) via the HP-IB. The LOCKED light indicates a locked sweep condition. Marker signals are available within the swept range.

Accuracy — CF/ΔF and START/STOP modes

Start or Stop Frequencies: 1 kHz TYPICAL.

Linearity: ±0.05% of sweep with respect to Sweep Out voltage (TYPICAL)

Resolution: 1 Hz for CF, ΔF, START, and STOP frequencies

Sweep Time: Available in CF/ΔF and START/STOP modes. Continuously adjustable from 10 ms to 100 s. When sweep time is selected, user may toggle between continuous and single sweep by pressing the ACQUIRE key. The RESET key initiates a sweep when in single sweep sub mode.

Marker Frequencies: Available in CF/ΔF and START/STOP modes. Up to four frequency markers are settable across the swept band. Markers are adjustable with the control knob, data entry keyboard, or step keys to 1 Hz resolution.

Accuracy: 0.3% of sweep width TYPICAL.

Marker Output: Rectangular pulse, 5 volts peak (TYPICAL) available from the Z axis Out connector on front panel. Source impedance approximately 500 ohms.

LOCK/ROLL (Manual Lock or Auto Lock*): Sweep is phase locked by the 5344S to a precise start frequency and then control is transferred to the sweeper to complete the sweep. The source determines sweep time, marker frequencies, and stop frequency.

Table 1-1. Model 5344A Specifications (Continued)

If source is too far from desired frequency, the user must tune source (Manual Lock) or the 5344S can automatically tune (Auto Lock) via the HP-IB. The LOCKED light indicates a proper locked condition.

Start Frequency
- Resolution: 1 Hz
- Accuracy: Equal to counter accuracy
- Residual stability: <50 kHz rms TYPICAL

5344S Option 043: With the 5343A microwave counter installed, special interface cables can be connected to the 8350A to enhance measurements. The marker frequencies and stop frequency can be measured by the counter with improved accuracy (±100 kHz TYPICAL).

Subharmonic/Offset Mode

Mode is selected by rear panel switch and indicated by a decimal point in far right of numeric display. Multiplier type sources (eg., HP 83570A, 83590A, 83592A, 83594A, 83595A, 86290) can be phase locked via the subharmonic frequency available on the Auxiliary Output connector. The actual output frequency is displayed on the 5344S while locking to the subharmonic output.

*Auto Lock feature available when 5344S is used with 8350A or 8620C Option 011.

Offset mode is used for sources that generate RF frequencies by heterodyning a variable oscillator with a fixed oscillator. When the variable oscillator is available at the Auxiliary Output (e.g. HP 83592A, 83595A), the 5344S can display the actual source output frequency, while phase locking to the Auxiliary Output, after entering the appropriate frequency offset on the counter. Accuracy is now limited by stability of the fixed oscillator (±20 kHz rms TYPICAL for 83592A, 83595A).

Subharmonic/Offset mode can be useful for any general purpose sources used with external multipliers and mixers.

Acquire Function

Acquires a frequency measurement from the counter and places the value in the numeric display when unlocked.

HP-IB Operation

Remote Programming

Interface: HP-IB (Hewlett Packard's implementation of IEEE Standard 488)

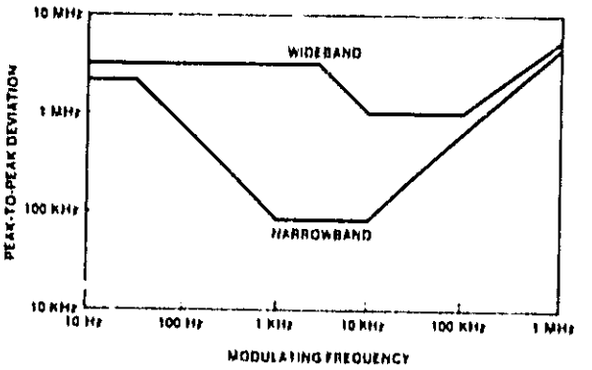
Functions controlled: All front panel functions with the exception of the line switch and Auto Lock are programmable.

Shorthand Interface Function Codes: SH1, AH1, T2, L2, SR1, RL1, PP0, DC1, DT1, C0, E1

Standalone: The 5344A is connected to the source via HP-IB and acts as the controller. Rear panel switch selectable. This mode accomplishes Auto Lock.*

Maximum FM (TYPICAL)

Phase lock will be maintained if the maximum FM on source is not exceeded at the various modulating frequencies.



GENERAL

Z-Axis In: Accepts the Z Axis modulation signal from sweeper. Tied directly to Z Axis Out for LOCK ROLL mode. Otherwise has no effect. Front panel BNC female connector.

Z-Axis Out: Provides a Z Axis modulation signal for display devices. Is generated by the 5344A when in locked sweep modes (CF, ΔF or START STOP) and is a direct coupled rectangular pulse of approximately +5.0 volts peak during retrace. Intensity marker signals are also output through this connector. At all other times is tied directly to Z Axis In. Front panel BNC female connector.

Sweep In: Accepts the sweep out signal from the sweeper as required in LOCK ROLL mode and ties it directly to the Sweep Out connector. Otherwise has no effect. Front panel BNC female connector.

Sweep Out: Provides a linear ramp voltage from 0 to 10 volts synchronous with the swept RF output when in locked sweep mode (CF, ΔF or START STOP). Otherwise, Sweep Out is tied directly to Sweep In. Front panel BNC female connector.

Sweep Trigger: Output signal necessary in LOCK ROLL mode for connection to Ext Trigger connector on sweeper. Signal is greater than +2V dc and wider than 2 ms (TYPICAL). Rear panel BNC female connector.

10 MHz In: Must be connected to the Freq. Std. Out (10 MHz) from the rear panel of counter. Rear panel BNC female connector.

IF In: Must be connected to the IF Out signal from the rear panel of the counter. Rear panel BNC female connector.

Operating Temperature: 0°C to 50°C

Power Requirements: 100, 120, 220, 240 V rms, +5%, -10%, 48-66 Hz; 125 VA max (5344A) plus 100 VA Max (5342A)

Accessories Furnished:

Power cords (2), 229 cm. (7 1/2 ft.)
BNC cables (2), 46 cm (18 in.)
Sweep trigger interface cable for 8350A, 1m (39 in.)

Size: 133 mm H x 426 mm W x 498 mm D (5 1/4" x 16 3/4" x 19 5/8")

Weight: Net 18.7 kg (41 lbs.) Shipping 25.9 kg (57 lbs.)

Signal Source Compatibility Chart — HP Sweepers

8350A Sweep Oscillator. MANUAL LOCK and AUTO LOCK

8620A, B and 8620C (without Option 011) Sweep Oscillator MANUAL LOCK

8620C (Option 011) Sweep Oscillator. MANUAL LOCK and AUTO LOCK except no AUTO LOCK ROLL

8683A, B and 8684A, B Signal Generators: MANUAL LOCK

Specifications describe the instrument's warranted performance. TYPICAL or NOMINAL performance characteristics provide useful applications information but are not warranted.

1-12. SAFETY CONSIDERATIONS

1-13. This product is used as part of a Safety Class I instrument (provided with a protective earth terminal.) Safety information pertinent to the operation and servicing of this instrument is included in appropriate sections of this manual.

1-14. EQUIPMENT SUPPLIED

1-15. The equipment supplied with the 5344S is listed in *Table 1-2.*

Table 1-2. Equipment Supplied

Description	Quantity	Part Number
18" BNC-BNC Cable (See *Figure 4-1*)	2	8120-3370
*Processor Interface Cable (See *Figure 2-3*)	1	8120-3435
Power Cables	2	8120-1378
*Front Handles	2	5060-9899
8350A External Sweep Trigger Cable	1	8120-3545
Locking Hardware (5344A to Counter) *Front Link Locks *Screws for above 8-32 × 1/4"	1 4 4	 0050-0515 2510-0192
*Processor Interface Cable Shield *Screws for above 6-32 × 3/8" *Flat washers for above	1 4 4	05344-00006 2360-0117 3050-0066
IF OUT Modification IF OUT cable assembly Tie-wraps*	 1 3	 05344-60114 1400-0249

*These items are factory installed in a standard 5344S and 5344S Opt 043 (5344A and counter.)

1-16. EQUIPMENT AVAILABLE

1-17. Equipment available for use with the 5344S is listed in *Table 1-3.*

Table 1-3. Equipment Available

*Service Accessory Kit	10842A
Transit Case	P/N 9211-2655
Male BNC to Female SMC cables (5343A) 5343A Sweep Interface Cables	11592-60001
APC-3.5 Adapter (female-to-female)	P/N 1250-1709
APC-3.5 (female) to N (female) Adapter	P/N 1250-1745
Model 5006A Signature Multimeter	See separate data sheet
Model 5001A Microprocessor Exerciser	See separate data sheet
Model 8350A Microwave Sweep Oscillator	See separate data sheet
Model 8620C Microwave Sweep Oscillator	See separate data sheet

*The 10842A contains eleven special extender boards and is supplied with Installation Note 10842-90004.

1-18. DESCRIPTION

1-19. The Hewlett-Packard Model 5344A is a companion instrument for the 5342A or 5343A Microwave Frequency Counter. This two instrument system is called the 5344S Source Synchronizer which provides the ability to obtain high stability and high resolution frequencies from various voltage controllable signal generators, such as the 8620A/B/C, 8640A/B, 8683A/B, 8684A/B, and

8350A. Refer to *Tables 3-7* and *3-8* for details on compatible sweep generators and plug-ins, respectively. The front panel keyboard of the 5344A provides controls to:

1. Select a specific frequency to 1 Hz resolution.
2. Select a center frequency and sweep over a range of ±20 MHz. Sweep time is also selectable.
3. Select a Start and Stop frequency and sweep over this range. Sweep time is also selectable.
4. Make wideband sweeps limited only by the sweep oscillators range.
5. Generate up to four markers during locked sweeps (CF/ΔF and Start/Stop).

NOTE

If the 5344A is to be added to an existing 5342A or 5343A, option 001 high stability oscillator should be installed in the counter. Option 001 determines the stability of the system and is required to maintain its integrity. In addition, the rear panel IF OUT connector must be modified as described in paragraph 2-23. The required materials for this modification are supplied with the 5344S Option 142.

1-20. Model Numbers

1-21. This manual contains operating information for the 5344S Microwave Source Synchronizer. However, at various points it is necessary to discuss different instruments that comprise the 5344S. To help clarify this, the following model numbers are used throughout the manual:

5344S—Used when discussing the complete system (counter and 5344A).

5342A or 5343A—Used when discussing the counter only.

5344A—Used when discussing the 5344A instrument only.

1-22. OPTIONS

1-23. The 5344A Source Synchronizer is typically ordered with a 5342A Microwave Frequency Counter as the 5344S System. However, several options are available with the 5344S, such as deleting the 5342A Microwave Frequency counter and replacing it with the 5343A Microwave Frequency Counter (Option 043). *Table 1-4* lists the available options for the 5344S.

Table 1-4. Available 5344S Options

Option	Description
Standard	5344A and 5342A Option 001*, 011** Microwave Frequency Counter
142	5344A Source Synchronizer Only; deletes the 5342A Microwave Frequency Counter. Includes all interfacing hardware and materials to modify IF OUT BNC. (See paragraph 2-23.)
043	Deletes 5342A Microwave Frequency Counter and replaces it with a 5343A Counter †
908	Adds Rack Mount Flange Kit
910	Adds an extra set of manuals
913	Adds Rack Mount Flange Kit with Handles

*5342A Option 001 and 5343A Option 001 adds the High Stability Oscillator 10544A.
**5342A Option 011 and 5343A Option 011 adds Hewlett-Packard Interface (HP-IB)
†A 5344S System containing a 5343A Microwave Frequency Counter can be operated to 26.5 GHz. The 5343A will include Option 001 and 011.

1-24. Ordering Special 5344S Combinations

1-25. The 5342A and 5343A each have options available as listed in *Table 1-5*. Two of these options (Options 001 and 011) are standard equipment with the 5342A in the 5344S System. However, there may be a desire to have one or more of the other available options. For example, you may want to include Option 002 Amplitude Measurement with the 5342A in the system. To order a 5344S System with Options 002, 003, and/or 004 installed in the counter, order the 5344S Option 142. This deletes the counter (but still includes all the necessary interfacing hardware). Then order the desired counter with the options. Once the separate instruments are received, they must be connected as described in paragraph 2-19. In the case described above, you would order:

1. 5344S System Option 142 - Deletes the 5342A counter and:
2. 5342A Option 001, 002 and 011.

1-26. When ordering in this configuration, be sure to order Options 001 High Stability Oscillator, for the counter. Option 001 High Stability Oscillator is the key to the 5344S Source Synchronizer System's stability.

1-27. For complete remote control of the 5344S system, Option 011 HP-IB should be installed in the counter. HP-IB is required in the counter only for Frequency Offset Locking under remote control. If HP-IB is not installed in the counter, the offset must be entered manually. See paragraphs 3-56 and 3-80.

NOTE

The 5344A can automatically recognize the counter to which it is attached. Once this has been determined, the 5344A will limit the maximum frequency to 18 GHz for the 5342A and 26.5 GHz for the 5343A. If the 5342A has Option 005 (operation to 24 GHz), the 5344A will still limit the operation to 18 GHz. However, when the 5342A is not being used with the 5344A (Manual and Auto Lock off), the 5342A Option 005 will operate as normal to 24 GHz.

Table 1-5. 5342A/5343A Table of Options

5342A	5343A	Description
001	001	High Stability Oscillator 10544A
002	N/A	Amplitude Measurement
003	N/A	Extended Dynamic Range
004	004	Digital-to-Analog Converter
005	N/A	Operates to 24 GHz
006	006	Microwave Limiter
011	011	Hewlett-Packard Interface Bus (IEEE 488-1978)

See the appropriate counter manual for specifications and operating details for these options.
N/A Not Available

1-28. Operation of Counter Options with the 5344A

1-29. Certain options for the 5342A and 5343A Microwave Frequency Counters reduce the input sensitivity. *Table 1-6* lists the options and the sensitivity levels for those options.

Table 1-6. 5342A/5343A Options Sensitivity

Option	5342A	5343A
002 and 003		
.5 - 12.4 GHz	-19 dBm	———
12.4 - 18 GHz	-14 dBm	———
006		
.5 - 12.4 GHz	-18 dBm	-27 dBm
12.4 - 18 GHz	-14 dBm	-21 dBm
18 - 26.5 GHz	———	-15 dBm

1-30. Options 002 Amplitude Measurement (5342A only) and 004 Digital-to-Analog Converter (5342A/5343A) will be automatically turned off whenever the 5344S is placed into Manual or Auto Lock mode. They will be re-activated when Manual or Auto Lock is turned off again. Option 011 HP-IB Interface for either counter is locked out whenever the 5344A is in Remote mode and Manual Lock or Auto Lock is on (but the 5344S is not necessarily Locked.) Any offset entered into the counter through the HP-IB will remain active. See paragraph 3-171, Remote Frequency Offset Locking.

1-31. RECOMMENDED TEST EQUIPMENT

1-32. The test equipment listed in *Table 1-7* is recommended for use during performance tests, adjustments, and troubleshooting. Substitute test equipment may be used if it meets the required characteristics listed in the table.

Table 1-7. Recommended Test Equipment

Instrument	Critical Specs	Model	Use
Spectrum Analyzer	500 MHz-18 GHz	HP 8565A	O,P
Microwave Counter	500 MHz-26.5 GHz	HP 5343A	O,P
Controller	IEEE 488-1978	HP 85A*	O,P
Sweep Mainframe	5344S Compatible	HP 8350A	O,P
8350A/8620A/B/C Plug-ins	500 MHz-26.5 GHz	HP 86595A	O,P
uP Exerciser	For use with M6800	HP 5001A	T
Signature Multimeter	Signature analysis, multimeter functions	HP 5005A/B	T
Oscilloscope	100 MHz bandwidth	HP 1740A	O,P,T
Oscilloscope	275 MHz bandwidth	HP 1725A	T
Power Splitter	DC-18 GHz	HP 11667A	O,P
Directional Coupler	7 - 18 GHz	HP 11691D	O,P
Crystal Detector	.5 - 18 GHz	HP 8476A	O,P
Digital Multimeter	20V Range	HP 3465A	A
Spectrum Analyzer	20 Hz - 300 kHz Input	HP 141T/8556A/ 8552A	A,T
Service Accessory Kit	Complete Kit	10842A	T
10842A contains: (Only required boards are listed)	2 × 10 pin	05342-60030	T
	2 × 12 pin	05342-60031	T
	2 × 15 pin	05342-60032	T
	2 × 18 pin (2)	05342-60033	T
	2 × 22 pin (2)	05342-60034	T
	2 × 24 pin	05342-60035	T
	A14 Extender 5342A/43A	05342-60036	T
	†A9 Polarized Extender	05344-60014	T

A = Adjustments
O = Operational Verification
P = Performance Test
T = Troubleshooting

* The HP 85A requires the 00085-15003 I/O ROM (installed in the 82936A ROM Drawer), the 82903A 16K Memory Module, and the 82937A HP-IB Interface. An HP 85F may be substituted for the HP 85A and accessories.

† The 05344-60014 has been added to the 10842A Extender board kit. Earlier kits may not have this extender board. It should be obtained and added to the kit.

SECTION II
INSTALLATION

2-1. INTRODUCTION

2-2. This section contains information for unpacking, inspection, storage, installation, and connection to the Hewlett-Packard Interface Bus.

2-3. UNPACKING AND INSPECTION

2-4. If the shipping carton is damaged, inspect the instrument for visible damage (scratches, dents, etc.). If the instrument is damaged, notify the carrier and the nearest Hewlett-Packard Sales and Support Office immediately (the offices are listed at the back of this manual). Keep the shipping carton and packaging material for the carrier's inspection. The Hewlett-Packard Sales and Support Office will arrange for repair or replacement of your instrument without waiting for the claim against the carrier to be settled.

2-5. PREPARATIONS FOR USE

2-6. Power Requirements

2-7. The HP 5344A requires a power source of 100-, 120-, 220-, or 240-volt ac, +5%, -10%, 48 to 66 Hz single phase. The power consumption is approximately 125 VA. See Section I, Specifications for description.

2-8. Line Voltage Selection

CAUTION

Before connecting the instrument to ac power lines, be sure that the voltage selector is properly positioned as described in the following paragraph.

2-9. The 5344A is equipped with a power connector module that has a plug-in printed-circuit card line voltage selector to choose 100-, 120-, 220-, or 240-volt ac operation (see *Figure 2-1*). Before applying power, the selector card must be set to the correct position and the correct fuse must be installed as described in paragraph 2-13.

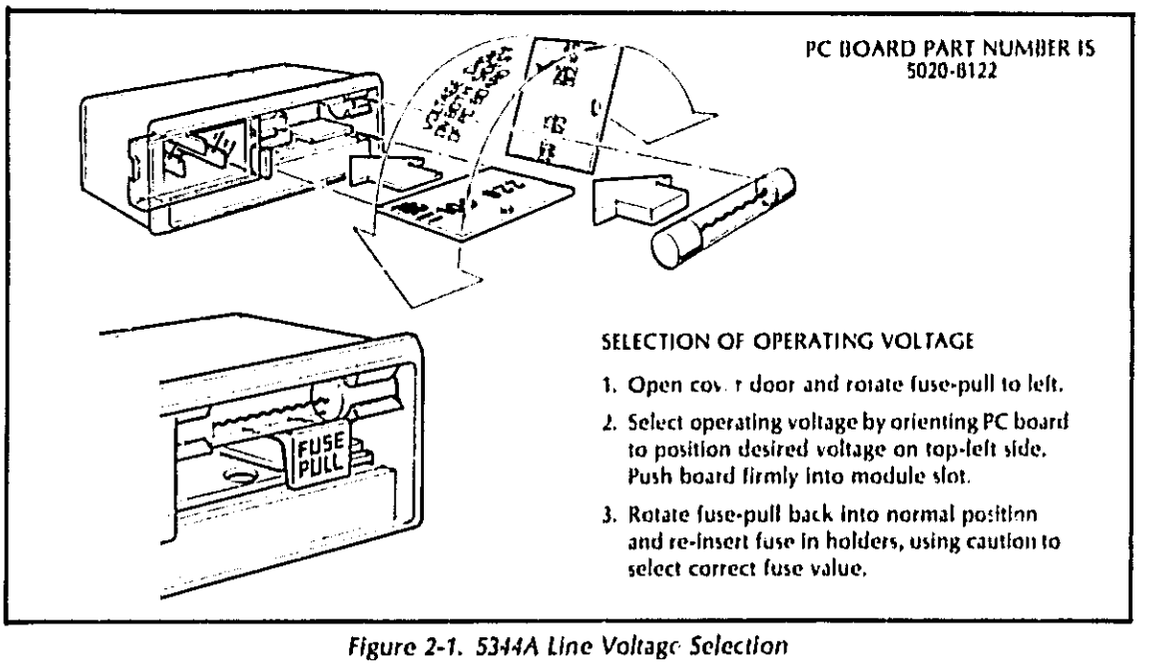


Figure 2-1. 5344A Line Voltage Selection

2-10. Power line connections are selected by the position of the plug-in card in the module. When the card is plugged into the module, the only visible markings on the card indicate the line voltage to be used. The correct value of line fuse, with a 250-volt rating, must be installed after the card is inserted.

2-11. To convert from one line voltage to another, the power cord must be disconnected from the power module before the sliding window covering the fuse and card compartment can be moved to expose the fuse and circuit card.

2-12. Pull on the fuse lever and then pull the card out of the module. The fuse lever must be held to one side to remove and insert the card. Insert the card so the marking that agrees with the line voltage to be used is visible.

2-13. Return the fuse lever to normal position, insert the correct fuse, slide the plastic window over the compartment, and connect the power cord to complete the conversion.

NOTE

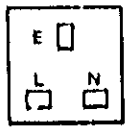
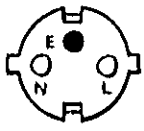
For operation from 100V ac or 120V ac use a 1.25A slo-blo fuse (2110-0305). For 220V ac or 240V ac operation use a .75A slo-blo fuse (2110-0360).

2-14. Power Cable

WARNING

BEFORE CONNECTING ELECTRICAL POWER TO THIS INSTRUMENT, THE PROTECTIVE EARTH TERMINALS OF THIS INSTRUMENT MUST BE CONNECTED TO THE PROTECTIVE CONDUCTOR OF THE POWER CORD (MAINS). THE MAIN PLUG SHALL ONLY BE INSERTED IN A SOCKET OUTLET PROVIDED WITH A PROTECTIVE EARTH CONTACT. THE PROTECTIVE ACTION MUST NOT BE DEFEATED BY THE USE OF AN EXTENSION CORD (POWER CABLE) WITHOUT A PROTECTIVE CONDUCTOR (GROUNDING).

2-15. The 5344A is shipped with a three wire power cable. When the cable is connected to an appropriate ac power source, this cable connects the chassis to the earth ground. The type of power cable plug shipped with each instrument depends on the country of destination. Refer to *Figure 2-2* for the part numbers of the power cables and plug configurations available.

Plug Type	Cable HP Part No.	CD	Plug Description	Cable Length (Inches)	Cable Color	For Use In Country
250V 	8120-1351 8120-1703	0 6	Straight **BS1363A 90°	90 90	Mint Gray Mint Gray	United Kingdom, Cyprus, Nigeria, Rhodesia, Singapore
250V 	8120-1369 8120-0696	0 4	Straight **NZSS198/ASC112 90°	79 87	Gray Gray	Australia, New Zealand
250V 	8120-1689 8120-1692	7 2	Straight **CEE7-Y11 90°	79 79	Mint Gray Mint Gray	East and West Europe, Saudi Arabia, Egypt, So. Africa, India (unpolarized in many nations)
125V 	8120-1348 8120-1398 8120-1754 8120-1378 8120-1521 8120-1676	5 5 7 1 6 2	Straight **NEMA5-15P 90° Straight **NEMA5-15P Straight **NEMA5-15P 90° Straight **NEMA5-15P	80 80 36 80 80 30	Black Black Black Jade Gray Jade Gray Jade Gray	United States, Canada, Japan (100V or 200V), Mexico, Philippines, Taiwan
250V 	8120-2104	3	Straight **SEV1011 1959-24507 Type 12	79	Gray	Switzerland
250V 	8120-0698	6	Straight **NEMA6-15P			United States, Canada
220V 	8120-2956 8120-2957	2 3	Straight **DHCK 107 90°	79 79	Gray Gray	Denmark

*CD = Check Digit (refer to Section VI).

** Part number shown for plug is industry identifier for plug only. Number shown for cable is HP Part Number for complete cable including plug.

E = Earth Ground; L = Line; N = Neutral

Figure 2-2. AC Power Cables Available

2-16. Operating Environment

2-17. TEMPERATURE. The 5344A may be operated in temperatures from 0°C to 50°C.

2-18. ALTITUDE. The 5344A may be operated at altitudes up to 4,600 metres (15,000 feet).

2-19. Mating Counter to 5344A

2-20. If the 5344A and the 5342A (or 5343A) counter are ordered together (as the 53445), they will be received as one unit connected together mechanically and electrically. However, if the 5344A is ordered separately and is to be connected to an existing counter, the following procedure should be performed. Refer to *Figure 2-3*.

a. Unpack the 5344A and locate the mating hardware and cables listed below:
   1. Interface cable shield (aluminum plate with four square holes.)
   2. Four link locks.
   3. Four 6-32 × 3/8" flat head pozidriv screws (for link locks).
   4. Four 6-32 × 7/16" pan head pozidriv screws.
   5. Four flat washers (for 6-32 × 7/16" screws).
   6. Counter to 5344A processor interface cable (ribbon type).
   7. Two 18" BNC-BNC cables.
   8. 8350A Sweeper Interface Cable.
   9. IF OUT modification cable and tie-wraps.

b. Remove any handles or rack flanges from the counter.

c. Using a 6-32 × 3/8" flat-head screw, attach two of the link locks to the right-hand side of the counter. Orient the locks so they are open to the rear of the counter. Attach the locks to the top and bottom screw holes.

d. Using the remaining two 6-32 × 3/8" flat head screws, attach the remaining link locks to the left-side of the 5344A. Orient the locks so they are open to the front of the 5344A.

e. Slide the counter and the 5344A together at the front frames. The link locks will mate together. Bring the rear frames together so the instruments are parallel.

f. Looking at the rear of the two instruments, insert the processor interface cable, with the red stripe up, into the Processor Interface connectors.

g. Orient the interface cable shield to align the square hole of the cover with the square mounts on the instrument's rear chassis frames.

h. Secure the processor shield with the four 6-32 × 7/16" pan-head pozidriv screws and flat washers.

i. Using the two BNC-BNC cables, connect the counter FREQ STD OUT to the 5344A 10 MHz, and the counter IF OUT to the 5344A IF IN.

j. Attach the handles and/or rack flanges to the 53445.

k. This completes the mating procedure. Additional connections will be made to the instruments as applications are described.

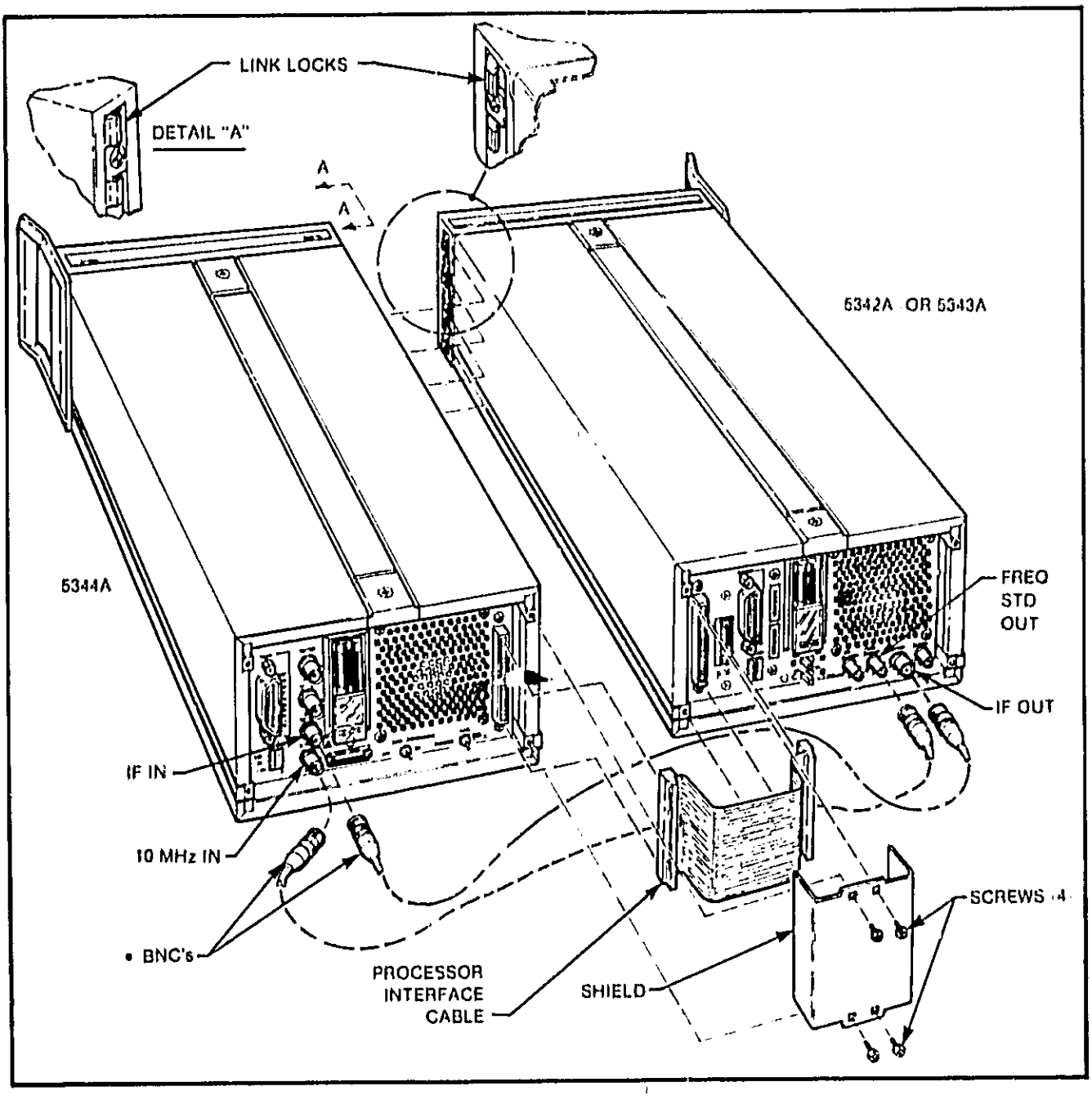


Figure 2-3. Connecting 5344A to the 5342A (or 5343A)

2-21. Compatibility with 5342A/43A Counters

2-22. The 5344A is compatible with all standard 5342A and 5343A Microwave Frequency Counters. However, certain serial number counters require a simple modification as described in the following paragraph.

2-23. Required Modifications for Earlier Version 5342A/43A Counters

2-24. Earlier models of 5342A and 5343A counters require a modification to the IF OUT BNC (J4) on the rear panel. This requires adding a brass shield to BNC connector J4 (IF OUT). This is required on 5342A with serial numbers 2142A05040 and below and for 5343A serial numbers 2201A00625 and below. The following procedure describes this modification.

NOTE

This change is not required on counters received as part of a 5344S system or on counters with serial numbers higher than those listed in paragraph 2-24. Refer to *Figure 2-4* for IF OUT modification part numbers for required parts.

1. Remove all power from the 5342A/5343A counter.
2. Remove all four feet from the counters bottom cover.
3. Remove the top cover by removing the screw in the rear strap cap (securing the rear of the strap handle). Remove the cap and then slide the top cover toward the rear until it can be freely removed.
4. Using a large Pozidriv screwdriver rotate the screw located in the rear of the bottom cover counter-clockwise. As the screw is rotated, the cover will begin to slide backwards away from the instrument. Grasp the cover and assist its movement until it can be freely removed. The screw will remain attached to the rear cover.
5. Using a large Pozidriv screwdriver, remove the four screws securing the rear frame casting to the main frame struts.
6. Separate the rear frame casting, tilting the top forward to allow access to the IF OUT BNC connector J4.
7. Unsolder the IF OUT shielded cable from J4. Disconnect the opposite end of the cable from A27J2 located at the front of the instrument. Cut the three grey tie-wraps securing the cable bundle. Remove the cable.
8. Replace the IF OUT cable with the new cable supplied (05344-60114). Connect the new cable to A27J2 and route it to the rear panel just as the original cable. Resecure the cable bundle with the three supplied tie-wraps (1400-0249).
9. Remove the rear panel IF OUT BNC and replace it with the supplied BNC. Secure the BNC firmly.
10. Slide the brass barrel (1), nylon spacer (2), and a brass sleeve (3), onto the IF OUT shielded cable as shown in *Figure 2-4*.

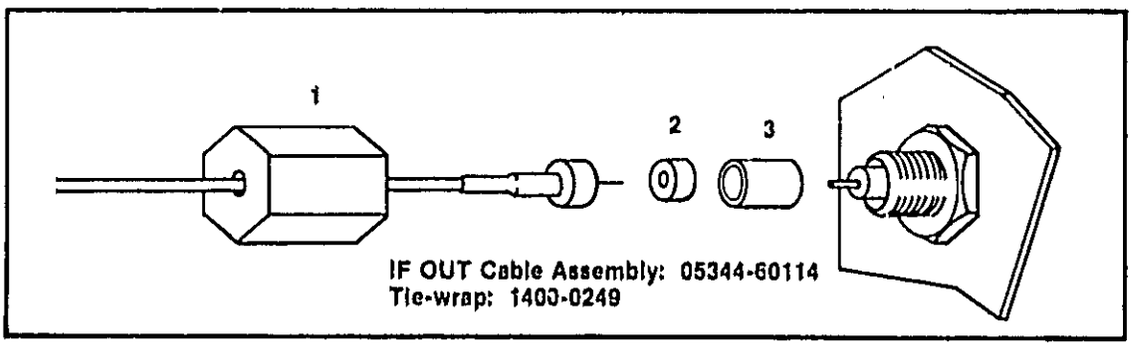


Figure 2-4. IF OUT Modification

11. Insert the exposed wire into the center conductor of the BNC. While holding the cable in position, thread the BNC barrel onto the BNC. Pulling the rear panel back should provide enough room to thread the barrel.
12. Tighten the barrel firmly.
13. Re-assemble the counter by performing steps 2 through 6 in reverse order.
14. This completes the modification.

2-25. HP-IB Interconnections

2-26. HEWLETT-PACKARD INTERFACE BUS. Interconnection data concerning the rear panel HP-IB connector is provided in *Figure 2-5*. This connector is compatible with the HP 10833A/B/C/D cables. (See *Table 2-1* for cable descriptions.) The HP-IB system allows interconnection of up to 15 (including the controller) HP-IB compatible instruments. The HP-IB cables have identical "piggy-back" connectors on both ends so that several cables can be connected to a single source without special adapters or switch boxes. System components and devices may be connected in virtually any configuration desired. There must, of course, be a path from the calculator (or other controller) to every device operating on the bus. As a practical matter, avoid stacking more than three or four cables on any one connector. If the stack gets too large, the force on the stack produces great leverage which can damage the connector mounting. Be sure each connector is firmly (finger tight) screwed in place to keep it from working loose during use.

Table 2-1. HP-IB Cable Descriptions

10833A	1 metre (3.3 ft.)
10833B	2 metre (6.6 ft.)
10833C	4 metre (13.2 ft.)
10833D	0.5 metre (1.6 ft.)

DESIGNED FOR HP-IB SYSTEMS

The above symbol when located in the upper corner of a page indicates HP-IB information is contained on that page. This information may be operation, performance, adjustment, or service related.

2-27. CABLE LENGTH RESTRICTIONS. To achieve design performance with the HP-IB, the proper voltage levels and timing relationships must be maintained. If the system cable is too long the lines cannot be drive properly, and the system will fail to perform properly. Therefore, when interconnecting an HP-IB system, it is important to observe the following rules:

a. The total cable length for the system must be less than or equal to 20 meters (65 feet).

b. The total cable length for the system must be less than or equal to 2 meters (6.6 feet) times the total number of devices connected to the bus.

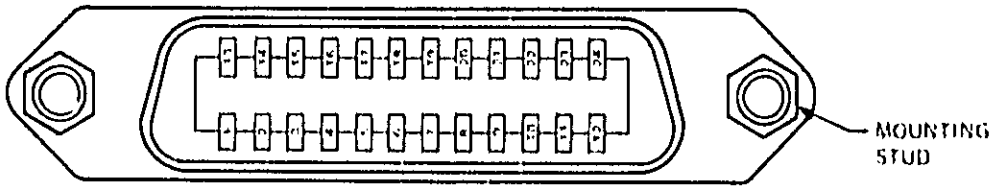
c. The total number of instruments connected to the bus must not exceed 15.

2-28. 5344A Listen/Talk Address

2-29. The 5344A contains a rear panel HP-IB instrument address selection switch. There are five switches designated (A5, A4, A3, A2, A1) which are used to select the address. Instructions for setting and changing the address are provided in Section III of this manual along with the programming codes.

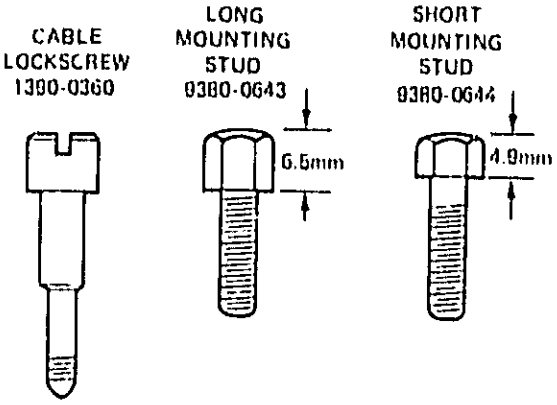
2-30. HP-IB Descriptions

2-31. A description of the HP-IB is provided in Section III of this manual. A study of this information is necessary if the user is not familiar with the HP-IB concept. Additional information concerning the design criteria and operation of the bus is available in IEEE Standard 488-1978, titled "IEEE Standard Digital Interface for Programmable Instrumentation." See *Figure 2-5*.



PIN	LINE	
1	DIO1	
2	DIO2	
3	DIO3	
4	DIO4	
13	DIO5	
14	DIO6	
15	DIO7	
16	DIO8	
5	EOI	
17	REN	
6	DAV	
7	NRFD	
8	NDAC	
9	IFC	
10	SRQ	
11	ATN	
12	SHIELD-CHASSIS GROUND	
18	P/O TWISTED PAIR WITH PIN 6	THESE PINS ARE INTERNALLY GROUNDED
19	P/O TWISTED PAIR WITH PIN 7	
20	P/O TWISTED PAIR WITH PIN 8	
21	P/O TWISTED PAIR WITH PIN 9	
22	P/O TWISTED PAIR WITH PIN 10	
23	P/O TWISTED PAIR WITH PIN 11	
24	ISOLATED DIGITAL GROUND	

The 5344A contains metric threaded HP-IB cable mounting studs as opposed to English threads. Metric threaded HP 10833A, B, C, or D HP-IB cable lockscrews must be used to secure the cable to the instrument. Identification of the two types of mounting studs and lockscrews is made by their color. English threaded fasteners are colored silver and metric threaded fasteners are colored black. DO NOT mate silver and black fasteners to each other or the threads of either or both will be destroyed. Metric threaded HP-IB cable hardware illustrations and part numbers follow.



Logic Levels

The Hewlett-Packard Interface Bus logic levels are TTL compatible, i.e., the true (1) state is 0.0V dc to 0.4V dc and the false (0) state is +2.5V dc to +4.0V dc.

Programming

Refer to Section III, Operation

Mating Connector

HP 1251-0293; Amphenol 57-30240.

Mating Cables Available

HP 10833A, 1 metre (3.28 ft.)
HP 10833B, 2 metres (6.56 ft.)
HP 10833C, 4 metres (13.12 ft.)
HP 10833D, 0.5 metre (1.64 ft.)

Cabling Restrictions for Standard System

1. A Hewlett-Packard Interface Bus System may contain no more than 1.8 metres (6 ft.) of connecting cable per instrument.
2. The maximum accumulative length of connecting cable for any Hewlett-Packard Interface Bus System is 20.0 metres (65.6 ft.).

Figure 2-5. Hewlett-Packard Interface Bus Connections

2-32. Operational Check

2-33. To determine if the instrument is operating properly, refer to the operational verification in Section IV. Contact your nearest HP Sales and Support Office (see manual back cover) for information concerning warranty claims.

2-34. PACKAGING FOR RESHIPMENT

2-35. Original Packaging

2-36. The same containers and materials used in factory packing can be obtained through the Hewlett-Packard Sales and Support Office listed at the rear of this manual.

2-37. Since the 5342A/5343A Microwave Frequency Counter is an integral part of the 53445 System, the counter should be returned with the 5344A when service is required.

2-38. If the instrument is being returned to Hewlett-Packard for service, attach a tag indicating the type of service required, return address, model number, and full serial number. Mark the container FRAGILE to assure careful handling.

2-39. In any correspondence, refer to the instruments by model numbers and full serial numbers.

2-40. Other Packaging Methods

2-41. If it becomes necessary to re-ship an instrument, good commercial packing should be used. Contract packaging companies in many cities can provide dependable custom packaging on short notice. The following general instructions should be followed when repackaging with commercially available materials.

a. If shipping to a Hewlett-Packard Office or Center, attach a tag indicating the type of required, return address, model number, and full serial number.

b. Wrap the instrument in heavy paper or plastic.

c. Use a strong shipping container. A double-wall carton made of 350-pound test material is adequate.

d. Use enough shock-absorbing material (3- to 4-inch layer) around all sides of the instrument to provide a firm cushion and prevent movement inside the container. Protect the front panel with cardboard.

e. Seal the shipping container securely.

f. Mark the shipping container FRAGILE to assure careful handling.

2-42. STORAGE

2-43. If the instrument is to be stored for an extended period of time, it should be enclosed in a clean, sealed container.

SECTION III
OPERATION AND PROGRAMMING

3-1. INTRODUCTION

3-2. This section contains descriptions of operating characteristics and modes, operating procedures, descriptions of the front and rear panel controls and indicators, and Hewlett-Packard Interface Bus (HP-IB) programming information.

3-3. The 5344A is a companion instrument for the 5342A or 5343A Microwave Frequency Counter. The operation of the 5342A/5343A Counter should be understood before attempting to operate the 5344S system. For complete information on the 5342A or 5343A Microwave Frequency Counters, refer to the Operating and Service Manuals for these instruments. When appropriate, the 5344A/S operating information is supplemented with 5342A/5343A operating information where necessary for clarity.

3-4. The 5344A Source Synchronizer in combination with either a 5342A or 5343A Microwave Frequency Counter allows phase locking of a signal source to any frequency (1 Hz resolution) in the high operating range of the counter used. The desired lock frequency is selected via the 5344A keyboard and the signal source must be set within the specified capture range of that frequency in order for the 5344A to achieve lock. This can be automatically achieved if the source is an HP 8350A or an HP 8620C with Option 011.

3-5. The counter is fed a sample of the source signal to be locked. The 5344A generates a correction signal for the signal source by comparing the phase of the down converted signal in the counter with an internal crystal controlled synthesizer. The synthesizer may be swept over narrow ranges (40 MHz maximum), and the signal source will follow remaining phase-locked. For wider sweeps with an 8620C or 8350A, the source may be locked at the start of the sweep and the correction voltage held constant throughout the rest of the sweep (Lock and Roll mode).

3-6. User interaction with the system is through the 5344A front panel, which contains a keyboard, 11-digit scratchpad display, and RPG (rotary-pulse-generator) knob. All 5344S functions except Auto Lock may be controlled remotely via HP-IB.

3-7. The 5344A is attached mechanically to the 5342A or 5343A counter and electrically to the counter's microprocessor bus, IF and 10 MHz outputs.

3-8. MODES OF OPERATION

3-9. The 5344S has four modes of operation. They are CW, CF/ΔF, Start/Stop, and Lock/Roll. Each mode can be used in Manual Lock or Auto Lock, as described in the following paragraph.

3-10. MANUAL LOCK MODES

3-11. Manual Lock requires the signal source to be manually tuned to within capture range of the selected frequency. If the 5344S is used with an 8350A or 8620C with Option 011, the 5344S can automatically tune the sweeper to the selected frequency (Auto Lock.)

3-12. CW in Manual Lock

3-13. The 5344S attempts to lock the signal source to the selected Continuous Wave (CW) frequency. If the signal source is too far from the desired frequency for the 5344S to bring it into lock, the FREQ HI or FREQ LO annunciator is turned on, and the signal source must be manually tuned (as indicated). When lock is achieved, the LOCKED annunciator lights. If lock is lost, the 5344A turns off the LOCKED annunciator and again indicates FREQ HI or FREQ LO.

3-14. CF/ΔF in Manual Lock

3-15. The 5344S attempts to achieve a locked sweep of the signal source from:

$$\text{Center Freq} - \frac{\Delta\ \text{Freq}}{2} \quad \text{to} \quad \text{Center Freq} + \frac{\Delta\ \text{Freq}}{2}$$

using the SWEEP TIME selected by the user. If the signal source is too far from the desired frequency range, it must be manually tuned (as in CW mode). When lock is achieved, the LOCKED annunciator is lit. If lock is lost, the 5344S turns off the LOCKED annunciator, and the signal source must be manually tuned to regain lock. The sweep must not cross 500 MHz, 650 MHz, or 800 MHz, as described in paragraph 3-50.

NOTE

If ΔF = 0, CF/ΔF operates the same as the CW mode since the sweep width (ΔF) = 0.

3-16. In CF/ΔF the 5344S can generate 4 separate markers over the sweep range. Discussion of markers begins in paragraph 3-43.

3-17. Start/Stop in Manual Lock

3-18. The 5344S attempts to achieve a locked sweep of the signal source from the selected START frequency to the selected STOP frequency using the SWEEP TIME selected by the user. If the STOP frequency is less than START, or STOP-START is too large, an error indication is given, and the locking process is restarted. If the signal source is too far from the desired frequency range, the signal source must be tuned (as in CW mode). The capture range, however, is reduced by 1/2. When lock is achieved, the LOCKED annunciator is lit. If lock is lost, the 5344S turns off the LOCKED annunciator, and the signal source must be manually tuned to regain lock. The sweep must not cross 500 MHz, 650 MHz, or 800 MHz, as described in paragraph 3-50.

NOTE

If START = STOP, START/STOP operates the same as the CW mode since the sweep width = 0.

3-19. In Start/Stop, the 5344S can generate 4 separate markers over the sweep range. Discussion of markers begins in paragraph 3-43.

3-20. Lock/Roll in Manual Lock

3-21. In the Lock/Roll mode, the 5344S has the ability to provide a highly accurate locked starting frequency and then uses the sweeper's ability to sweep wide frequency ranges. This combination gives significantly better accuracy for broad sweeps than a sweeper alone.

3-22. The 5344S attempts to lock the signal source to the selected Lock/Roll Start frequency in the same manner as for CW Manual Lock operation. If successful, the 5344S holds the FM correction signal constant and sends a sweep trigger signal to the sweeper to start the sweep. It then waits for an end-of-sweep signal (derived from the sweeper's SWEEP OUT-10 volt ramp) and repeats the lock/trigger/wait cycle. The sweeper controls must be set properly to achieve the desired sweep from the locked starting frequency. In Lock/Roll mode, the LOCKED light is lit continuously even though the signal is only locked at the start of each sweep.

3-23. AUTO LOCK MODES (SYSTEM CONTROLLER)

3-24. The 5344A contains a portion of the HP-IB code set for the 8350A and 8620C Sweep Oscillators. This gives the 5344S the ability to program many of these sweeper functions as if it were a controller (by IEEE 488-1978 terminology the 5344S is a System Controller). For instance if the CW frequency selected on the 5344A front panel is 10 GHz, the 5344A would automatically program the sweeper to a CW frequency of 10 GHz, provided the sweeper's RF Plug-in has that range. Paragraph 3-177, System Controller Mode, gives the IEEE 488-1978 details concerning this feature. The following paragraphs describe the basic operation of Auto Lock.

NOTE

Since the 8620C cannot be programmed for specific frequencies in the Start/Stop mode, the 8620C cannot be used in Auto Lock/Roll.

3-25. CW in Auto Lock

3-26. The 5344S attempts to lock the signal source to the selected CW frequency. If the signal source is too far from the desired frequency, the 5344S tunes the sweeper via HP-IB to bring it into lock. When lock is achieved, the LOCKED annunciator is turned on. If lock is lost, or cannot be achieved, the 5344S turns off the LOCKED annunciator and attempts to adjust the signal source via HP-IB to regain lock. If the signal source cannot attain the desired frequency, an error indication is displayed on the 5344A.

3-27. CF/ΔF in Auto Lock

3-28. The 5344S attempts to achieve a locked sweep of the signal source from the selected CF - ΔF/2 to CF + ΔF/2 using the SWEEP TIME selected by the user. If the signal source is too far from the desired frequency range, the 5344S tunes it via HP-IB (as in CW mode). When lock is achieved, the LOCKED annunciator is turned on. If lock is lost, the 5344S turns off the LOCKED annunciator and attempts to adjust the signal source via HP-IB to regain lock. If the signal source cannot attain the desired frequency, an error indication is displayed on the 5344A. The sweep must not cross 500 MHz, 650 MHz, or 800 MHz, as described in paragraph 3-50.

3-29. A marker signal is generated for any 5344S marker frequencies selected as described in paragraph 3-45.

3-30. Start/Stop in Auto Lock

3-31. The 5344S attempts to achieve a locked sweep of the signal source from the selected START to the selected STOP frequency using SWEEP TIME selected by the user. If the STOP frequency is less than START, or STOP - START is too large, an error indication is displayed on the 5344A. If the signal source is too far from the desired frequency range, the 5344S tunes it via HP-IB (as in CW mode). When lock is achieved, the LOCKED annunciator is turned on. If lock is lost, the 5344S turns off the LOCKED annunciator and attempts to adjust the signal source via HP-IB to regain lock. If the signal source cannot attain the desired frequency, an error indication is displayed on the 5344A. The sweep must not cross 500 MHz, 650 MHz, or 800 MHz, as described in paragraph 3-50.

3-32. A marker signal is generated for any 5344S marker frequencies selected as described in paragraph 3-45.

3-33. Lock/Roll in Auto Lock

3-34. The 5344S attempts to lock the signal source to the selected Lock/Roll Start frequency in the same manner as for CW Auto Lock. If successful, the 5344A holds the FM correction signal constant and sends a sweep trigger signal to the sweeper to start the sweep. It then waits for an end-of-sweep signal (derived from the sweeper's SWEEP OUT-10V RAMP) and repeats the lock/trigger/wait cycle. The sweeper controls must be properly set to achieve the desired sweep from the locked starting frequency. The 5344S only sets the sweeper close to the desired starting frequency via HP-IB in this mode.

3-35. Auto Lock/Roll will operate only with the 8350A Sweep Oscillator.

3-36. In Lock/Roll, the signal is locked only briefly at the start of each sweep. It is possible for the sweeper settings to be changed during the unlocked portion of the sweep such that the starting frequency is changed by some near multiple of the selected 5342A/43A local oscillator frequency. This would result in lock being regained at the end of the selected sweep, even though the frequency is nowhere near that desired (pressing Reset causes the 5344S to re-lock to the desired frequency). In Lock/Roll, the LOCKED light is normally lit continuously even though the signal is only locked at the start of each sweep.

3-37. LOCKED SWEEPS CF/ΔF and START/STOP

3-38. Sweep Time for Locked Sweeps

3-39. Sweep time can be selected for the two Locked Sweep modes, CF/ΔF and Start/Stop. The sweep time range is 10 ms to 100 s. The sweep mode may be Single or Continuous as determined by the ACQUIRE key (refer to under Front Panel Features, paragraph 3-102).

3-40. Sweep Increment

3-41. During locked sweeps (CF/ΔF and START/STOP modes) the 5344S is actually stepping the signal source to a new locked CW frequency every 10 microseconds in phase continuous steps. Normally the step increment is so small that the sweep appears to be continuous. The actual increment is given by the following formula (for START/STOP mode use START-STOP in place of ΔF):

$$\text{INCR} = \frac{\Delta F}{\text{SWEEP TIME}/10\ \mu\text{s}}$$

3-42. For example, if ΔF = 40 MHz and SWEEP TIME = 10 ms, INCR = 40 KHz. A fixed increment of 80 KHz is used for locked sweep retrace.

3-43. MARKERS

3-44. The 5344A has the ability to generate 4 separate markers. The markers are settable across the swept band. The following paragraphs describe the use of these markers.

3-45. Markers are generated by the 5344S only in CF/ΔF and START/STOP modes. A marker signal is then generated for desired 5344S marker frequencies in the swept range. The markers can be disabled by setting them to 0, as described in Front Panel Features, paragraph 3-102. Setting any Marker below 500 MHz causes that marker to default to 500 MHz. Setting any marker above 18 GHz (5342A)or above 26.5 GHz (5343A) causes that marker to default to 18 GHz or 26.5 GHz. If the 5344S is in Subharmonic Mode or Frequency Offset Locking, the limits are 10 MHz to 99.999999999 GHz.

3-46. Markers cannot be arbitrarily close to each other or to the Start or Stop frequencies of the sweep. The determining factor is time, so, for slower sweeps, the markers can be closer in frequency. The minimum separation of the first marker and the start frequency is given by:

$$\frac{(40\ \mu s)\ (STOP - START)}{SWEEP\ TIME}$$

3-47. The minimum marker spacing or the spacing between the last marker and the stop frequency is given by:

$$\frac{(1.4\ \mu s)\ (STOP - START)}{SWEEP\ TIME}$$

3-48. If markers are entered that are too close to each other or the stop frequency, the 5344A displays an error message while sweeping and ignores the offending marker(s). If the first marker is too close to the start frequency, the marker is ignored, but no error message is displayed.

3-49. The marker output is a -5V rectangular pulse at the Z AXIS OUT connector on the front panel.

3-50. Frequency Restrictions of Locked Sweeps

3-51. Due to IF bandwidth restrictions, locked sweeps (CF/ΔF and START/STOP modes) cannot cross the frequencies of 500, 650 or 800 MHz. An error message is displayed if such a sweep is attempted.

3-52. SUBHARMONIC LOCKING AND FREQUENCY OFFSET LOCKING MODES

3-53. Subharmonic Locking Mode Overview

3-54. Subharmonic Locking Mode provides several benefits. They are:

1. Allows the front panel RF OUT to be used at its full power capabilities. No power splitters or directional couplers are necessary.
2. The ability to operate the 5344S beyond the limits of 18 GHz (5342A) or 26.5 GHz (5343A). In this mode the maximum frequency is 99.999999999 GHz.
3. The RF OUT signal may be amplitude modulated (as required for network analyzers) without affecting the performance of the 5344S.

3-55. These benefits are described in more detail beginning in paragraph 3-74.

3-56. Frequency Offset Locking Overview

3-57. Frequency Offset Locking mode is similar to Subharmonic Locking mode in that the 5344S phaselocks at a frequency that is offset from the entered frequency (instead of at a sub-harmonic of the input frequency). The lower limit for this mode is 10 MHz. Frequency Offset Locking mode is active whenever a frequency offset is entered in the 5342A/43A, and the 5344S is in Subharmonic Locking mode, as described in *Figure 3-18*. The offset used by the 5344S is the negative of that entered in the counter and is applied to all frequencies entered into the 5344S except ΔF and STEP SIZE.

3-58. To understand the operation of these modes, a basic description of the 83500 and 86200 series plug-ins is provided in the following paragraphs.

3-59. HEWLETT-PACKARD RF PLUG-INS

3-60. Most Hewlett-Packard 86200 and 83500 series sweeper plug-ins use one of the following techniques to generate the output signal.

1. Yttrium-Iron-Garnet (YIG) Tuned Oscillator (YTO)
2. YTO and fixed frequency Cavity Oscillator
3. YTO and a GaAs FET Doubler
4. YTO and a YIG Tuned Multiplier (YTM)
5. A combination of the above

3-61. The following paragraphs provide descriptions of typical plug-ins, and describe basic block diagrams. The blocks indicate specific plug-ins that use a technique, but certain sections of the block are deleted.

3-62. Basic YTO

3-63. The basic YTO plug-in, as shown in *Figure 3-1*, generates frequencies over a single band. The YTO is voltage controlled over (for example), the range of 5.9 GHz to 12.4 GHz. The YTO output is fed to the front panel of the plug-in, possibly through an amplifier, as the RF OUT. An FM input on the rear panel allows external voltages to be used to vary the YTO frequency over a small range.

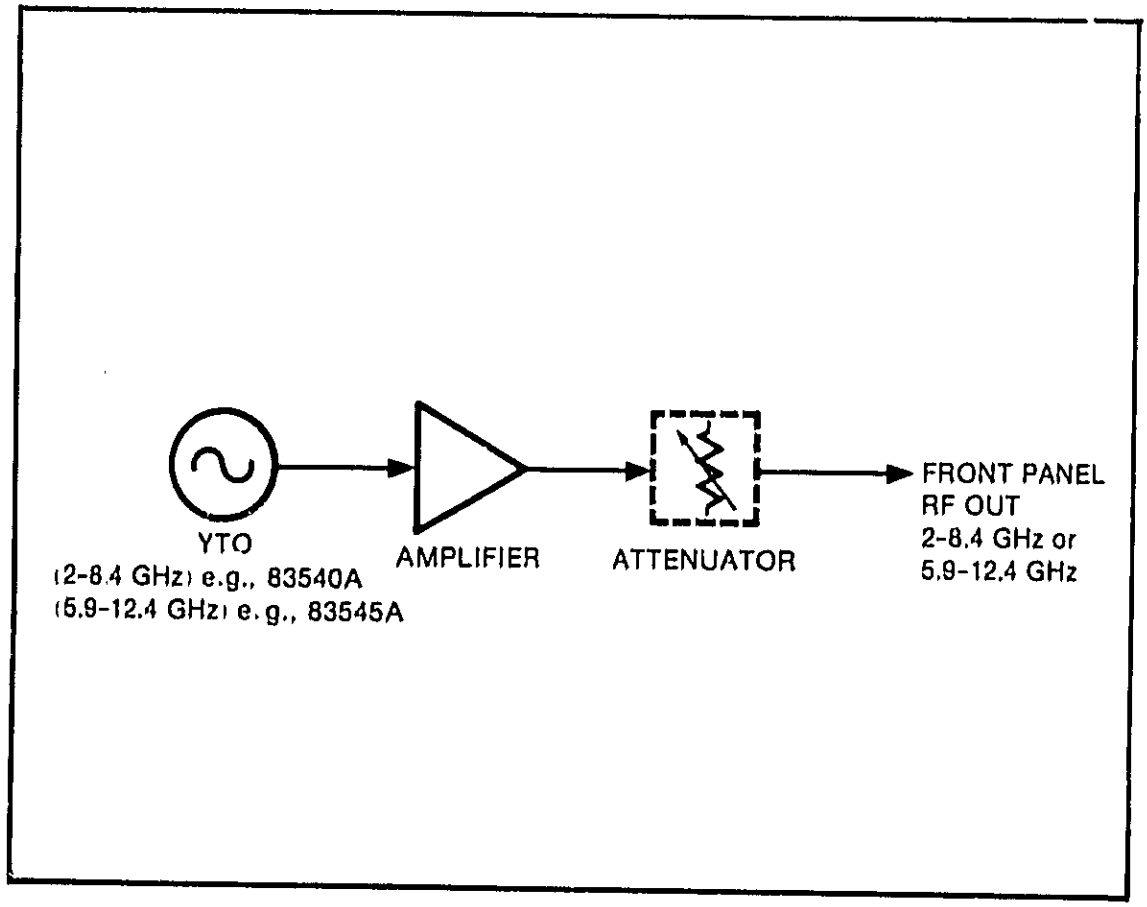


Figure 3-1. Basic YIG Tuned Oscillator

3-64. Basic YTO and Fixed Frequency Cavity Oscillator

3-65. To generate frequencies below the YTO's frequency range, the output of the YTO is mixed with a fixed frequency Cavity Oscillator, as shown in *Figure* 3-2. The difference frequency between the YTO and the Cavity Oscillator is fed to the front panel as the RF OUT. For example, the Cavity Oscillator is fixed at 3.8 GHz, and the YTO is tunable from 3.81 GHz to 6.2 GHz. When the YTO frequency is varied over its 3.81 GHz to 6.2 GHz range, the difference frequency moves from 10 MHz (3.81 GHz - 3.8 GHz) to 2.4 GHz (6.2 GHz - 3.8 GHz). The YTO output is fed to the rear panel as the AUX OUT. This plug-in would be specified with an output range of .01 GHz to 2.4 GHz even though the 3.81 GHz to 6.2 GHz signal is available at the rear panel AUX OUT. The front panel RF OUT is offset from the rear panel AUX OUT by a constant 3.8 GHz. Also located on the rear panel is an FM input to allow the YTO frequency to be varied over a small range. The stability and accuracy of this technique is limited by the stability of the YTO. However, when this plug-in is locked by the 53445, the Cavity Oscillator becomes the limit of the stability and accuracy.

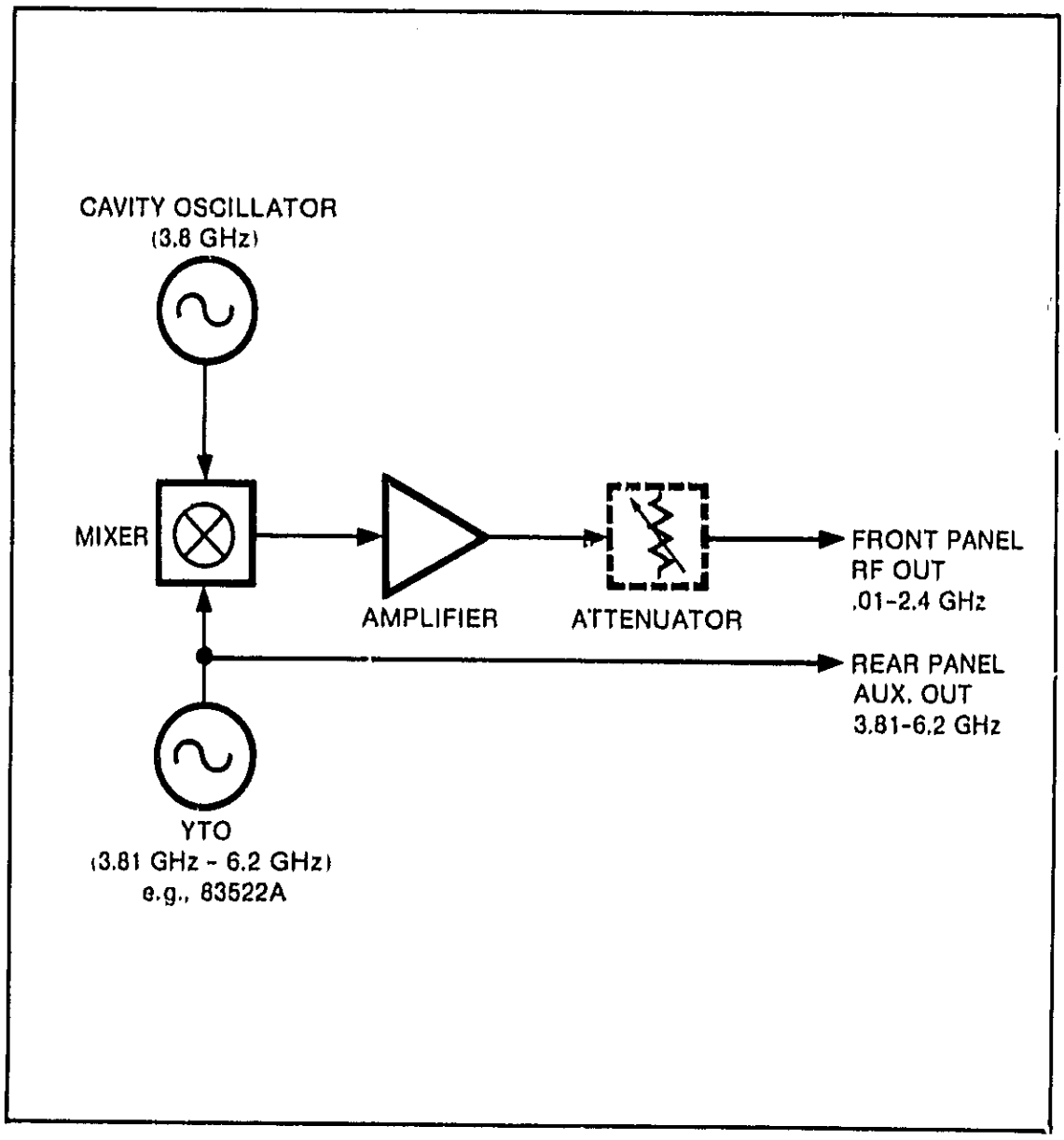


Figure 3-2. Basic YTO and Fixed Frequency Cavity Oscillator

3-66. YTO and GaAs FET Doubler

3-67. A simple way of generating frequencies above the YTO frequency range is to apply the YTO output (9- 13.25 GHz) to a GaAs FET Doubler, as shown in *Figure* 3-3. As implied by its name, the doubler multiplies the YTO frequency by a factor of 2. By varying the YTO frequency, a range of 18 GHz to 26.5 GHz can be generated. The doubled signal is fed to the front panel as the RF OUT. The YTO signal is fed to the rear panel as the AUX OUT. The AUX OUT signal is always 1/2 of the YTO frequency. The rear panel FM input allows the YTO frequency to be varied over a small range. The stability of this technique is limited by the stability of the YTO.

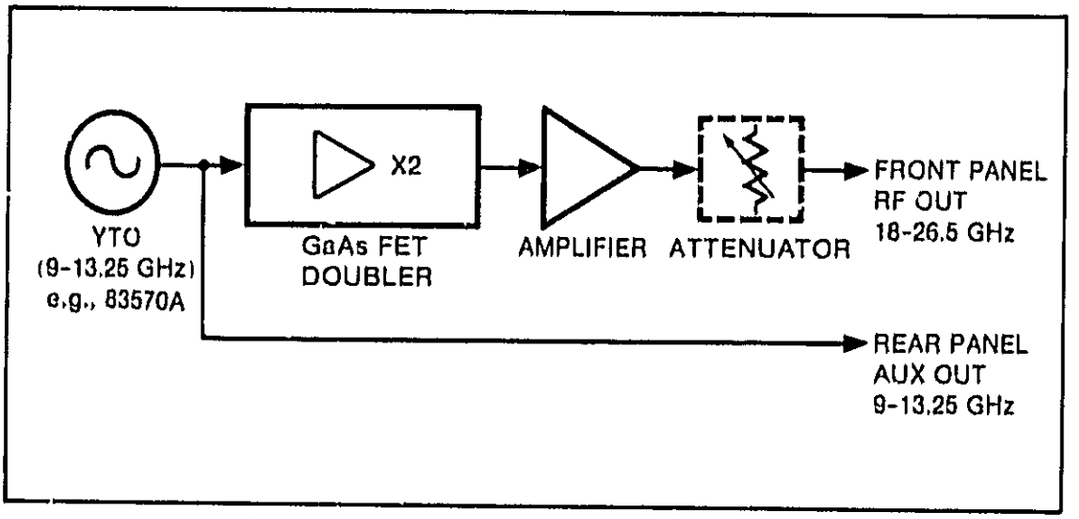


Figure 3-3. YIG Tuned Oscillator and GaAs FET Doubler

3-68. YTO and YTM

3-69. To generate frequencies above the YTO's frequency range, the output of the YTO is applied to a YIG Tuned Multiplier, as shown in *Figure 3-4*. The YTM multiplies the YTO output in integer steps (2 & 3). By varying the YTO frequency and the YTM value, a range of 2 GHz to 18.6 GHz can be generated. The multiplier output from the YTM is fed to the front panel as RF OUT. The YTO is fed to the rear panel as the AUX OUT. Also located on the rear panel is an FM input to allow the YTO frequency to be varied over a small range. The rear panel AUX OUT (YTO) is always a subharmonic of the front panel RF OUT (except when generating the 2 GHz to 6.2 GHz range. In this case the RF OUT and AUX OUT frequencies are equal). The stability of the technique is limited by the stability of the YTO.

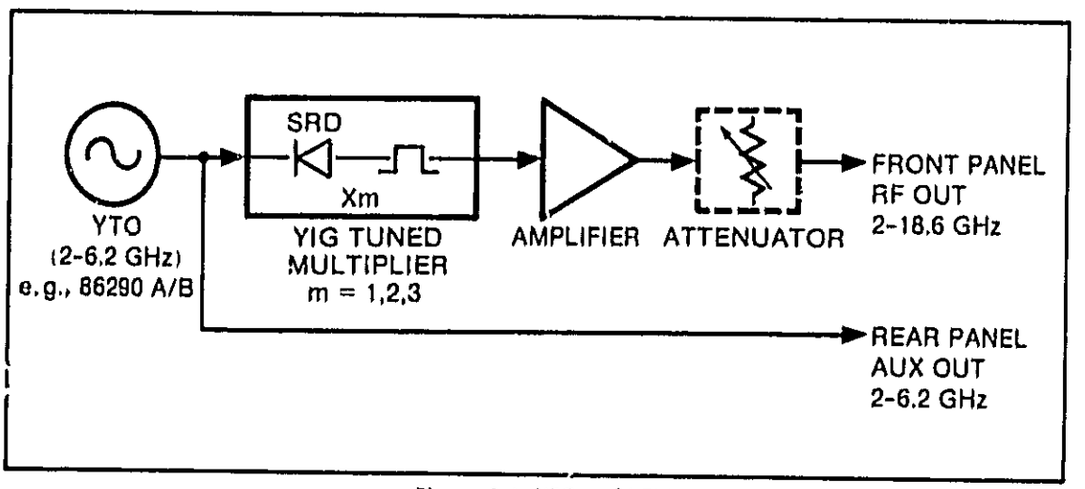


Figure 3-4. YTO and YTM

3-70. Wide Band Plug-Ins

3-71. To generate wide-band frequencies, for example, .01 to 20.0 GHz, all of the previous techniques can be combined in one unit as shown in *Figure 3-5*. To generate frequencies below the YTO range, it is mixed with a fixed frequency Cavity Oscillator. To generate frequencies above the YTO range, it may be multiplied by a YTM.

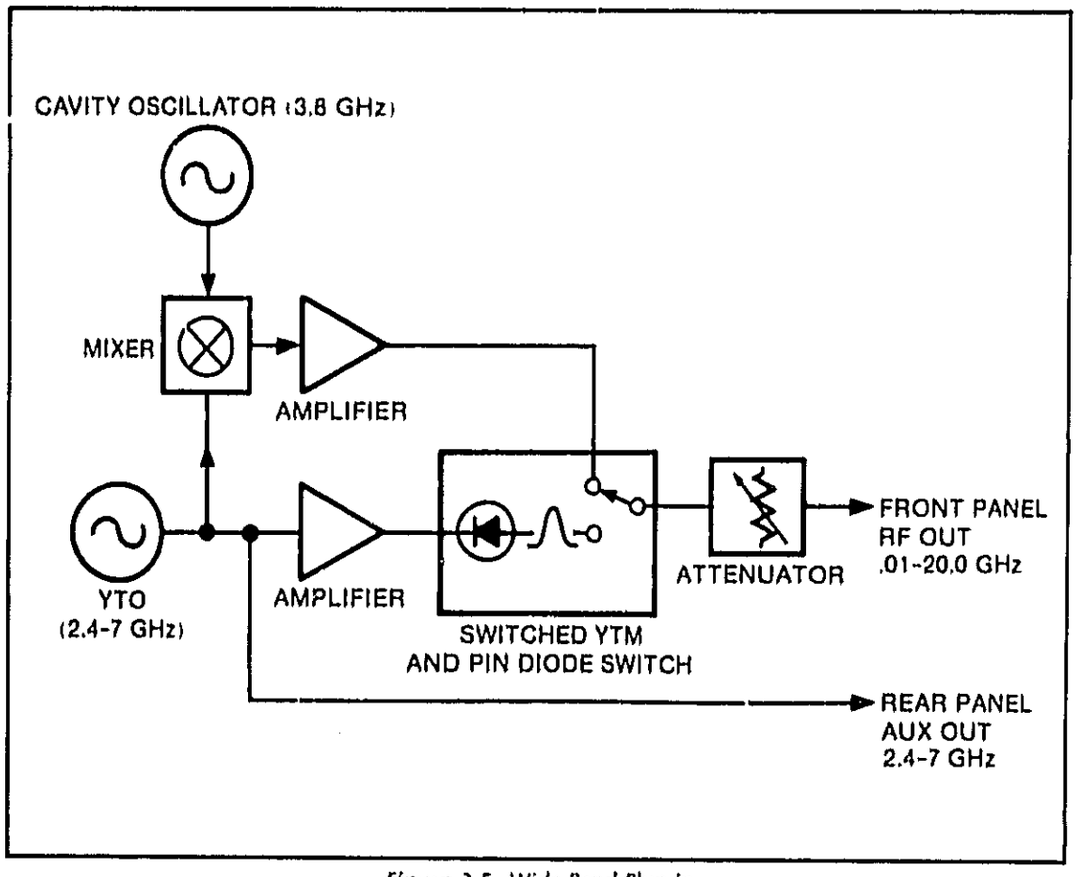


Figure 3-5. Wide Band Plug-In

3-72. Further investigation of the particular plug-in in use is suggested to help realize the full potential of the 5344S. Keep in mind the relationship between the RF OUT and the AUX OUT.

3-73. Subharmonic Locking and Frequency Offset Locking utilize these functions to expand the 5344S's capabilities.

3-74. Detailed Description of Subharmonic Locking Mode

3-75. Subharmonic mode provides a way to control sweeper plug-ins without having to place a power splitter or directional coupler in the signal path, which lowers the total available power and reduces flatness of the frequency response. Subharmonic Locking Mode also provides a way to control sweeper plug-ins that can generate frequencies beyond the 5344S's range.

3-76. In Subharmonic Locking Mode, instead of counting the front panel sweeper RF OUT to determine the necessary correction voltage, the 5344S counts the rear panel AUX OUT (YIG output). This AUX OUT is directly related to the front panel RF OUT, being either a subharmonic or offset by a specific value. This allows the front panel RF OUT to be used at its full power capabilities. Subharmonic Locking Mode cannot be used if the YIG output signal is not available before any multiplication, heterodyning, or modulation.

3-77. In Subharmonic Locking Mode, the AUX OUT (YIG fundamental) is applied to the counter input. Then the rear panel SUB HMNC/NORM switch is placed in the SUB HMNC position. This performs two functions: (1) enables the use of a Frequency Multiplier number, and (2) extends the 5344A's upper and lower numeric input limits. Frequencies not equal to the front RF OUT (but harmonically related) and frequencies above 18 GHz (5342A) or 26.5 GHz (5343A) can be entered. The 5344S compares the entered frequency on the 5344A to the frequency being applied to the counter, and determines the Frequency Multiplier number required, provided this number is within the range of 1 to 4. If the Frequency Multiplier number required is greater than 4, it must be entered manually. The highest allowable value is 99. See Frequency Multiplier, paragraph 3-89.

3-78. For example, the YIG is tuned to 5.0 GHz (at AUX OUT), but 20 GHz has been selected on the 5344A front panel. The 5344A determines the Frequency Multiplier number to be 4. The 5.0 GHz signal being applied to the 5342A is well within the 18 GHz limit.

3-79. However, if the selected value on the 5344A is 25 GHz, the 5344A will display Err 09, since the multiplier is 5, and the 5344A cannot automatically determine this. The multiplier of 5 must be manually entered. See Frequency Multiplier, paragraph 3-89.

3-80. Detailed Frequency Offset Locking

3-81. Frequency Offset Locking allows the 5344S to operate with sweeper plug-ins that can generate signals below the 5344S's lower limit of 500 MHz. In this mode, the 5344S can control plug-ins down to 10 MHz. In the following example, the range of the plug-in is 10 MHz to 2.4 GHz. This range is generated using the YTO and Fixed Frequency Oscillator (Cavity Oscillator) described in paragraph 3-64.

3-82. Instead of applying the front panel RF output of the plug-in to the 5344S's counter input, the rear panel AUX OUT (YTO) is used. The AUX OUT is always 3.8 GHz higher (offset) than the front panel RF OUT. The YTO range is from 3.81 to 6.2 GHz. As can be seen, this range is above the counter's 500 MHz lower limit. Since the offset is constant, the 3.8 GHz can be subtracted from the counter's display. The display will now always be equal to the plug-in's front panel RF OUT.

3-83. The 5344S controls the plug-in over the range of 3.81 to 6.2 GHz. The YTO is being mixed with the Cavity Oscillator to generate a lower frequency. The Cavity Oscillator frequency (3.8 GHz) being subtracted from the counter's display is for user convenience only. This ensures the 5344S display and the counter's display are consistent.

3-84. The offset is not subtracted from the counter's display under the following conditions:

1. Manual or Auto Lock is off.
2. Manual or Auto Lock is on but the 5344S is out of lock.

3-85. Under these conditions, the counter will display the actual rear panel AUX OUT (YTO) frequency.

3-86. The rear panel MODE switch must be in the SUB HMNC position.

3-87. Since the Cavity Oscillator is not being controlled, any variation in the Cavity Oscillator's frequency is directly reflected in the plug-in's front panel RF OUT.

3-88. Some plug-ins, such as those described in paragraph 3-70, combined several techniques to generate signals over a wide range. The plug-in changes techniques at some frequency, for example, above 2.4 GHz. If the 5344S is being used in Frequency Offset Mode and a frequency is entered above the frequency where the Cavity Oscillator technique is used, the relationship between the AUX OUT and the RF OUT will no longer be an offset, but instead could be equal or a subharmonic. The offset entered into the counter is no longer needed. The offset will cause tuning to be very difficult, if not impossible.

3-89. Frequency Multiplier

3-90. If a Frequency Multiplier of "1" has been entered and Subharmonic Locking mode is enabled, the 5344S calculates an internal subharmonic integer by dividing the entered locking frequency by the selected signal source frequency as measured by the 5342A/43A. If this result is close to an integer (typically 10%), the 5344A rounds it and uses it as the Frequency Multiplier. If the 5344A determines the Frequency Multiplier to be greater than "4", it will display Err 09 indicating that it cannot determine the multiplier and the correct value must be manually entered.

3-91. To manually enter a Frequency Multiplier, Marker 9 is selected and then the multiplier is entered and terminated by pressing any one of the unit keys (GHz/s, MHz/ms).

3-92. The Frequency Multiplier number is applied to all frequencies entered into the 5344A except for ΔF and Step Size.

3-93. MODE Switch (NORM/SUBHMNC on Rear Panel)

3-94. Since there is a possibility of locking to the wrong frequency if the sweeper is mistuned, a switch is provided to disable the Subharmonic Locking mode. The switch should be set to NORM if:

1. The plug-in does not use frequency multiplication.

2. The plug-in uses frequency multiplication, but the 5342A/43A is connected to the panel RF output.

3. There is a desire to utilize the subharmonic signal, but you prefer to enter the sub-harmonic frequency on the 5344A rather than the actual sweeper output frequency.

3-95. The position of the MODE switch is indicated by the rightmost decimal point of the numeric display. It is lit when subharmonic locking is in effect (SUB HMNC position) of MODE switch.

3-96. Since the 5342A/43A counter display is produced by multiplying the counted subharmonic signal (1 Hz resolution) by the harmonic number N, its resolution is only N • Hz. The 5344S synthesizer's resolution is .01 Hz, so the actual locked sweeper output frequency resolution is still 1 Hz, regardless of harmonic number.

3-97. When in REMOTE (HP-IB) operation, the 5344A LOOP BANDWIDTH and Subharmonic Locking MODE switches are ignored. These functions are controlled via HP-IB commands until REMOTE mode is terminated. See paragraph 3-138.

3-98. PARAMETER LIMITS

3-99. *Table 3-1* lists the absolute parameter limits for the 5344S.

Table 3-1. Parameter Limits

Mode	Parameter Limit	
	5342A	5343A
CW	500 MHz - 18 GHz	500 MHz - 26.5 GHz
CF ΔF	500 MHz - 18 GHz 0 MHz - 40 MHz	500 MHz - 26.5 GHz 0 MHz - 40 MHz
START STOP	500 MHz - 18 GHz 500 MHz - 18 GHz	500 MHz - 26.5 GHz 500 MHz - 26.5 GHz
L/R (Start)	500 MHz - 18 GHz	500 MHz - 26.5 GHz
MARKERS	500 MHz - 18 GHz Setting any Marker to 0 turns that Marker off	500 MHz - 26.5 GHz
SWEEP TIME	10 ms - 100 s	
STEP SIZE	0 Hz - 18 GHz	0 Hz - 26.5 GHz
FREQ. MULT.	1 - 99	

3-100. LOCKED MODE RESTRICTIONS

3-101. When LOCK mode is entered, the conditions listed in *Tables 3-2* and *3-3* must be met:

Table 3-2. Manual Lock Mode Restrictions

Mode	Manual Lock Mode Restrictions	
	5342A	5343A
CW	None	None
CF/ΔF	CF-ΔF/2 ≥ 500 MHz	CF-ΔF/2 ≥ 500 MHz
START/STOP	START ≤ STOP STOP-START ≤ 40 MHz	START ≤ STOP STOP-START ≤ 40 MHz
LK/R	None	None
MARKERS	None	None
SWEEP TIME	None	None

Table 3-3. Auto Lock Mode Restrictions

Mode	Auto Lock Restrictions	
	5342A	5343A
CW	Frequency in Signal Source Range	
CF/ΔF	CF-ΔF/2 ≥ 500 MHz CF-ΔF/2 and CF+ΔF/2 in Signal Source Range	CF-ΔF/2 ≥ 500 MHz
START/STOP	START ≤ STOP STOP-START ≤ 40 MHz START and STOP in Signal Source Range	START ≤ STOP STOP-START ≤ 40 MHz
LK/R	LOCK/ROLL START Frequency in Signal Source Range	
MARKERS	None	None
SWEEP TIME	None	None

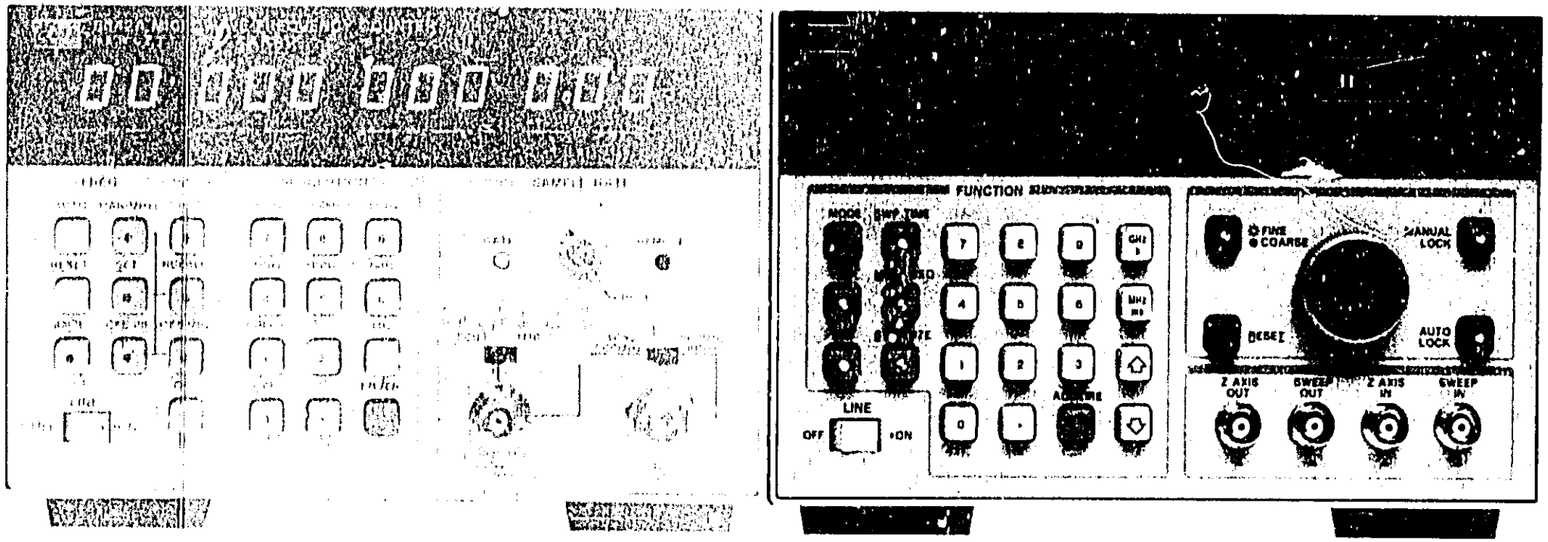


Figure 3-6a. Front Panel Features

3-102. FRONT PANEL FEATURES

3-103. *Figure 3-6a* illustrates the 5344A front panel features. The function of each indicator and control is described as follows:

INDICATORS

Annunciators

CW

Indicates that the 5344S is in the CW (Continuous Wave) mode (single frequency; no sweep). The CW frequency is displayed and may be changed when the F1 key is lit.

CF/ΔF

Indicates that the 5344S is in CF/ΔF mode (frequency is swept from CF−ΔF/2 to CF + ΔF/2). The center frequency is displayed and may be changed when the F1 key is lit. The sweep width is displayed and may be changed when the F2 key is lit.

STRT STOP

Indicates that the 5344S is in START/STOP mode (frequency swept from START to STOP). The start frequency is displayed and may be changed when the F1 key is lit. The stop frequency is displayed and may be changed when the F2 key is lit.

LK/R

Indicates that the 5344S is in LOCK/ROLL mode (frequency locked at L/R START, then released to allow sweeper to control sweep). The starting lock frequency is displayed and may be changed when the F1 key is lit.

NOTE

The MODE key "scrolls" through the four modes listed above. When the MODE key is pressed, the mode changes from CW to CF/ΔF, CF/ΔF to START/STOP, START/STOP to LOCK/ROLL, LOCK/ROLL to CW. See MODE KEY.

As the mode changes, the previous frequency parameters are carried into the new mode:

$$CF = CW \qquad \Delta F = STOP - START$$
$$START = CF - \Delta F/2 \qquad STOP = CF + \Delta F/2$$
$$L/R\ START = START$$
$$CW = L/R\ START + (STOP - START)/2$$

Display Digits

The 5344A display contains 11 digit positions. The display is used to show the value of the currently selected 5344S parameter. It is also used to indicate any error conditions arising during operation. The rightmost decimal point is used to indicate the position of the rear panel Mode switch. See paragraph 3-74. When the SWEEP TIME is selected, the characters S.S. appear on the display. See Sweep Time, paragraph 3-38.

GHz/MHz/S/ms

Indicates the units of the displayed value (gigahertz, megahertz, seconds, milliseconds).

Bar Meter

The meter (10 segment, center scale bar graph) indicates the frequency correction signal being applied to the signal source. It shows how close the source's uncorrected frequency is to that desired. The two center bars are dimly lit when the correction signal is near zero. As the signal moves from zero, the appropriate one of the two center bars switches to full intensity. As the signal continues to deviate from zero, successive bars light until full scale is reached. The direction the bar graph moves proportional to the voltage control FM input of the sweeper.

NOTE

The LOCKED, FREQ HI and FREQ LO indicators and the meter are not active unless the 5344S is in either MANUAL or AUTO LOCK mode. The METER is not active unless the 5344S is LOCKED and the LOCKED lamp is on.

FREQ HI/FREQ LO

When the input signal is not locked, these indicators show its position relative to the desired frequency. This information should be used to tune the signal source to achieve Manual Lock (see Manual Lock Mode Restrictions *Table 3-2*).

LOCKED

Indicates that the input signal of the 5342A/43A counter is locked to the frequency (CW or swept) entered on the 5344A keyboard.

RMT

When lit, shows that the 5344A has been selected for HP-IB programming. See Remote Programming Via the HP-IB, paragraph 3-13B.

TALK/LSN

These indicators show the selected 5344A HP-IB status. The TALK light indicates that the 5344A is the selected Talker on the HP-IB. This occurs only during Auto Lock and serial polls when the 5344A is being accessed remotely. The LSN light indicates that the 5344A is currently addressed to listen on the HP-IB. This never occurs in Auto Lock mode.

CONT

The CONT light indicates that the 5344S in the SYSTEM CONTROLLER mode (rear panel switch is in the SYS CONT position). With the switch in the SYS CONT position, the Auto Lock mode of the 5344S is enabled (See Auto Lock Key). No other HP-IB system controller can be on the bus when the 5344S is in this mode.

CONTROLS

FUNCTION KEYS

MODE

MODE cycles (scrolls) through the mode selection (CW, CF/ΔF, START/STOP, LOCK/ROLL). Each time the MODE key is pressed, the mode advances one function. The appropriate mode indicator is turned on, and the F1 key is lit. The 5344A parameter associated with F1 for the newly selected mode is displayed.

F1

Selects the first mode parameter (CW, CF, START, LOCK/ROLL START) for display/change.

F2

Selects the second mode parameter (ΔF, STOP) for display change. F2 is ignored in CW mode and in LOCK/ROLL is used only to invoke a special diagnostics mode. See *Table 8-9* for diagnostics.

SWP TIME

Selects the SWEEP TIME parameter for display/change. When SWEEP TIME is selected, it may also be used to toggle the sweep mode between SINGLE and CONTINUOUS by pressing the ACQUIRE key. In CONTINUOUS sweep, the 5344S initiates a new sweep immediately after the previous sweep ends. In SINGLE sweep, the 5344S waits for RESET to be pressed or a change in any sweep parameter before initiating a sweep. SINGLE sweep sub-mode is indicated by S.S. being displayed in the two leftmost digit positions of the 5344A display whenever SWEEP TIME is selected.

NOTE

If the SWEEP TIME is greater than 50 seconds and ΔF (or STOP-START) equals 1 Hz, the resultant sweep will be invalid.

MKR FREQ

Selects the marker frequency parameters or the frequency multiplier for display/change. The next key pressed should be 1, 2, 3 or 4, specifying which of the four markers is to be selected; 0, specifying that all four markers are to be set to zero (disabled); or 9, specifying that the Frequency Multiplier is to be entered. The display is cleared when the MKR FREQ key is pressed and remains blank until a valid digit (0, 1-4, or 9) is entered. The MKR FREQ light (in the key) also flashes until a valid digit is entered.

When MKR FREQ 0 is entered, all four marker frequencies are immediately set to zero, thus disabling them. MKR FREQ 1 is then selected as the parameter.

Entering MKR FREQ 9 displays the selected frequency multiplier. A new multiplier may then be entered with the numeric digit keys. Entry of the multiplier is completed by pressing either units key (GHz/s or MHz/ms). The frequency multiplier must be an integer between 1 and 99. Any entered fraction will be truncated.

STEP SIZE

Selects the STEP SIZE parameter for display/change.

Numeric Entry Keys (0-9, ., GHz/s, MHz/ms)

One means of changing the currently selected parameter is to enter a new value with the numeric entry keys. The general sequence of keystrokes is as follows:

First digit or decimals (.) - Pressing the first numeric entry key results in clearing the 5344S display of the selected value of the selected parameter and entering the value of the new first digit or the decimal point in the most significant position (leftmost).

Subsequent digits or decimals (.) - Subsequent depression of a digit key results in the new digit being displayed on the right of the value entered previously. Pressing the decimal point key results in the decimal point appearing in the rightmost digit position of the value entered. Only one decimal point may be entered. Any others after the first are ignored. Also, only 11 digits may be entered. Additional digits will be ignored.

GHz/s, MHz/ms - One of the units keys must be pressed following entry of the numeric value. If the currently selected parameter is a frequency, the "GHz" or "MHz" light will be turned on. If the parameter is SWEEP TIME, the "s" or "ms" light will be turned on. If the parameter is FREQUENCY MULTIPLIER, neither light will be turned on.

The value of the selected parameter is updated, and if the 5344S is in LOCK mode (MANUAL or AUTO), the new parameter is immediately reflected in the lock operation.

NOTE

Depending on the parameter changed and the magnitude of the change during LOCK mode, the 5344S may or may not be able to regain lock. It will, however, remain in LOCK mode waiting for the user to adjust the signal source (MANUAL LOCK) or tune it via HP-IB (AUTO LOCK).

Also note that once numeric entry has begun (i.e. once the first digit or decimal point key has been pressed), the increment/decrement keys, the tuning knob, the ACQUIRE key, and the MANUAL and AUTO LOCK keys are ignored until the entry is complete or terminated. Numeric entry may be terminated without affecting the value of the currently selected parameter by pressing any function key (including the one currently lit).

ACQUIRE Key:

5344S frequency parameters may be changed by acquiring them from the 5342A/43A counter. This is accomplished by pressing ACQUIRE following the selection of the desired parameter. If the 5344S is not locked, an automatic measurement is performed on the 5342A/43A and the result entered in the 5344S display and used to update the selected parameter. If the 5344S is locked, the value of the F1 parameter of the selected mode is taken as the new parameter and is immediately reflected in the lock operation. Note that SWEEP TIME, ΔF, and FREQUENCY MULTIPLIER may not be acquired. (When SWEEP TIME is selected, the ACQUIRE key is used to toggle the state of the sweep submode from CONTINUOUS to SINGLE or vice versa.)

Increment/Decrement Keys: (Up arrow ⇧, Down arrow ⇩)

Pressing the increment (or decrement) key results in the selected STEP SIZE being added to (or subtracted from) the currently selected parameter. The 5344S display is updated, and if the 5344S is in LOCK mode, the new parameter is immediately reflected in the lock operation. The increment and decrement keys may not be used to change SWEEP TIME or FREQUENCY MULTIPLIER.

Tuning Knob (RPG):

The tuning knob may also be used to adjust all 5344S parameters except FREQUENCY MULTIPLIER. Turning the knob clockwise increases the value of the parameter, and turning the knob counter-clockwise decreases the value. The 5344S display is updated, and, if the 5344S is in LOCK mode, the new value of the parameter is reflected immediately in the lock operation. The rate of change in the value being adjusted with the tuning knob is affected by the selected state of the FINE/COARSE key and the rate at which the knob is being turned.

FINE/COARSE Key

Pressing the FINE/COARSE key toggles the state of the FINE/COARSE indicator light (in the key). When the light is turned off, tuning knob adjustments are relatively coarse, allowing rapid changes in parameter values. When the light is on, adjustments are slower, allowing easier fine-tuning. The FINE/COARSE key is operational at any time except when the 5344S is in REMOTE HP-IB operation.

RESET Key:

The RESET key has three effects:

1. If the 5344S is in REMOTE HP-IB operation, the RESET key returns the 5344S to LOCAL mode, restoring control to the front panel. (Note that the RESET key is ignored if a "LOCAL LOCKOUT" HP-IB command has been received by the 5344A).

2. If the 5344S is in LOCK mode but not in REMOTE HP-IB operation, RESET restarts the locking algorithm.

3. If the 5344S is LOCKED, in a sweep mode (CF/ΔF, START/STOP, LOCK/ROLL), and the single sweep sub-mode has been selected, pressing RESET initiates a new sweep.

MANUAL LOCK Key:

Pressing the MANUAL LOCK key when its light is off, places the 5344S in LOCK mode (or keeps it in LOCK mode if AUTO LOCK is already in effect) and indicates that the signal source may need to be tuned to achieve lock. Pressing the MANUAL LOCK key when its light is already on disables LOCK mode and turns off the MANUAL LOCK indicator light.

AUTO LOCK Key:

Pressing the AUTO LOCK key when its light is off, places the 5344S in LOCK mode (or keeps it in LOCK mode if MANUAL LOCK is already in effect) and indicates that the signal source will be tuned automatically by the 5344S via HP-IB as necessary to achieve lock. Pressing the AUTO LOCK key when its light is already on disables LOCK mode and turns off the AUTO LOCK light.

The "SYSTEM CONTROLLER" switch on the 5344S rear panel HP-IB address switch must be in the "SYS CONT." position when AUTO LOCK is pressed. Otherwise, an error indication will be given.

NOTE

If no valid frequency has been entered when LOCK mode is initiated for the first time, a measurement will be made on the 5342A/43A and the resulting frequency used by the 5344S for the selected mode's F1 parameter (CW, CF, START, LOCK/ROLL START).

CONNECTORS

Z AXIS OUT

This connector provides a Z-axis modulation signal for display devices (oscilloscope, X-Y recorder). Provides a rectangular -5V pulse for selected marker frequencies. At all other times Z AXIS OUT is tied directly to Z AXIS IN. Z Axis Out is generated by the 5344S when locked in either locked sweep mode (CF/ΔF or START/STOP).

SWEEP OUT

This connector provides a linear ramp voltage from zero to 10 volts synchronous with the RF sweep signal. Sweep Out is generated by the 5344S when locked in either locked sweep mode. At all other times, SWEEP OUT is tied directly to SWEEP IN.

NOTE

Z AXIS OUT and SWEEP OUT are not generated by the 5344S in CF/ΔF mode if ΔF = 0 or in START/STOP mode if START = STOP.

Z AXIS IN

This connector accepts the Z-axis modulation signal from the sweeper. It is tied directly to Z AXIS OUT within the 5344S except when the 5344S is locked in a locked sweep mode. Then Z AXIS IN has no effect.

SWEEP IN

This connector accepts the SWEEP OUT signal from the sweeper. It is required in LOCK/ROLL mode to allow end-of-sweep detection and is then tied directly to SWEEP OUT within the 5344A. SWEEP IN is also tied to SWEEP OUT at all other times except when the 5344S is locked in a locked sweep mode (such as CW mode). Then SWEEP IN has no effect.

POWER

LINE OFF/ON

This switch applies power to the 5344A. If the 5342A (or 5243A) is already on, the counter will go through its power-up routine following the 5344A power-up routine.

3-104. REAR PANEL FEATURES

3-105. *Figure 3-6b* illustrates the 5344A rear panel features. The function of each control is described as follows:

HP-IB Connector

Used to convey data and programming information. IEEE-1978 Compatible. See paragraph 3-138.

HP-IB ADDRESS Switches

The HP-IB address switch has seven individual switches, six of which are actually used. The top switch determines if the 5344S's AUTO LOCK mode may be invoked from the front panel. With the switch in the SYS CONT. position, the 5344S will act as an HP-IB system controller to set sweeper parameters via HP-IB when AUTO LOCK is pressed. No other system controller may be in a powered-up state on the bus if SYS CONT. is selected. When the top switch is not in the SYS CONT. position, the 5344S may be programmed remotely val HP-IB by any bus controller.

The bottom five switches are used to set an HP-IB address in binary (bottom switch is the LSB). HP-IB addresses must be in the range 0-30 (binary 0000 11110). If all of the address switches are in the "1" position, the 5344S will use address 30. If system controller mode is selected (top switch in SYS CONT. position), the HP-IB address switches should be set to the address of the sweeper to be controlled in AUTO LOCK. If system controller mode is disabled, the HP-IB address switches determine the address by which the 5344S is accessed on the bus by a remote controller. The unmarked switch is not used. Refer to paragraph 3-151. HP-IB Address Selection for more details.

FM OUT

This connector provides the frequency correction signal (FM) needed to maintain the locked frequency output of the signal source. It must be connected to the FM input of the signal source or locked operation.

SWP TRIG

This connector provides the signal necessary to control the sweeper in LOCK/ROLL mode. It must be connected to the EXT TRIGGER connector on the sweeper (or, optionally, STOP SWEEP on the 8350A).

IF IN

This connector must be connected to the IF OUT signal provided on the rear panel of the 5342A/43A.

10 MHz IN

This connector must be connected to the FREQ STD OUT (10 MHz) signal provided on the rear panel of the 5342A/43A.

Input Power Module

AC input power module permits operation from 100-, 120-, 220-, 240- volts ac. The number visible in the module window indicates nominal line voltage to which the instrument must be connected (see *Figure 2-1*). The protective grounding conductor connects to the instrument through this module.

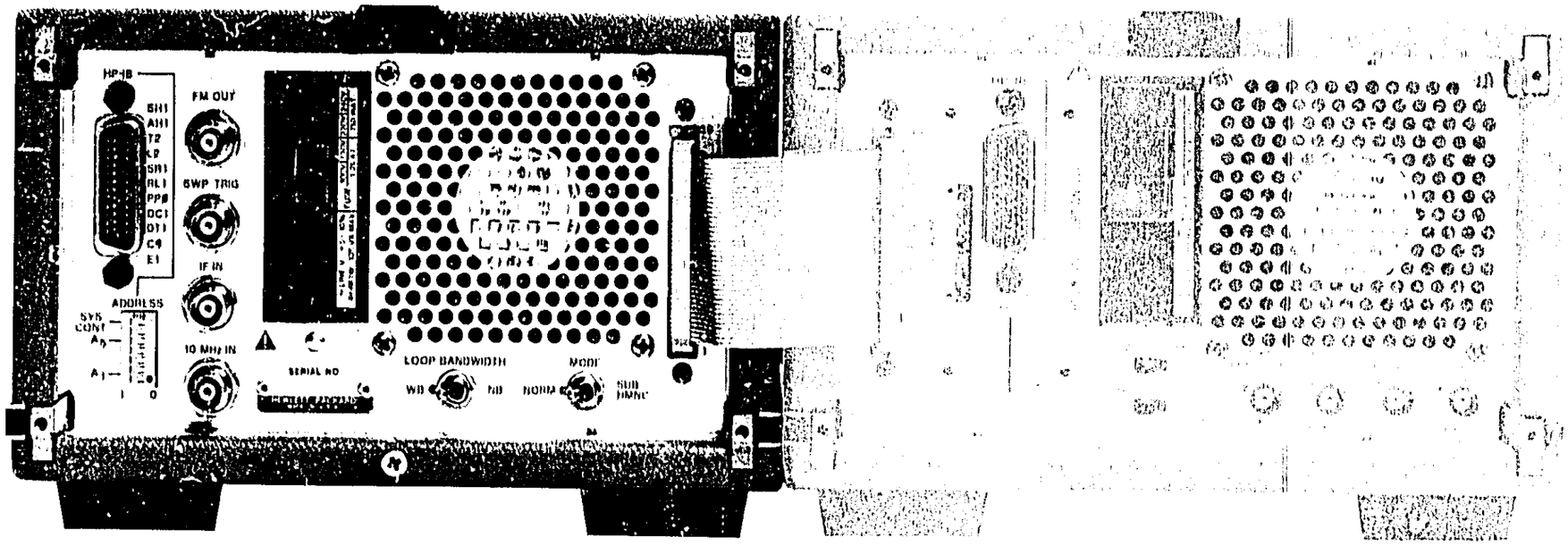


Figure 3-6b
REAR PANEL FEATURES

(See Page 3-21)

LOOP BANDWIDTH-WB/NB (WIDE BAND/NARROW BAND)

This switch sets locking loop bandwidth to about 100 kHz (WB), recommended for sweepers, or to about 20 kHz (NB), recommended for signal generators in CW mode only. The NB mode often yields better phase noise performance, but the WB mode is recommended to lock noisier sources (like sweepers) or any source when sweeping.

The position of the LOOP BANDWIDTH switch is indicated by the MANUAL or AUTO LOCK key light when in LOCK mode. If the switch is in the wideband (WB) position, the LOCK light is always on. In narrowband (NB), the light flashes slowly.

SUBHMNC/NORM (SUBHARMONIC/NORMAL) MODE Switch

This switch, when in the SUBHMC position, defeats the upper and lower frequency limits, and enables the use of a Frequency Multiplier. See paragraph 3-89.

PROCESSOR INTERFACE Connector

Provides the electrical connections for the interface cable between the 5344A and the counter.

WARNING

ANY INTERRUPTION OF THE PROTECTIVE (GROUNDING) CONDUCTOR INSIDE OR OUTSIDE OF THE INSTRUMENT OR OR DISCONNECTING OF THE PROTECTIVE EARTH TERMINAL IS LIKELY TO MAKE THE INSTRUMENT DANGEROUS. (See paragraph 2-14.)

3-106. Function Key Operation

3-107. Pressing any FUNCTION key *(Figure 3-6)* results in termination of any other parameter display or change in progress. The indicator light in the previously selected function key is turned off. The light associated with the newly selected parameter is turned on, and the selected value of that parameter is displayed (except as mentioned for marker frequencies and the Frequency Multiplier, which require that a digit key also be pressed before the value can be displayed). Once the parameter is displayed, it can be changed via the Numeric Entry Keys (all parameters), Increment/Decrement keys (frequency parameters only except STEP SIZE), or the Tuning Knob (all parameters except FREQUENCY MULTIPLIER).

3-108. 5344A Display While Locked

3-109. In LOCK mode, the 5342A/43A front panel displays the following as listed in *Table 3-4:*

Table 3-4. 5344A Display While Locked

Mode	5342/5343A Display
CW	CW Frequency
CF/ΔF	CF Frequency
START/STOP	Start Frequency
LOCK/ROLL	LOCK/ROLL START Frequency

3-110. In CW mode the 5342A/43A is actually counting the input frequency and updating the display. In CF/ΔF and START/STOP modes the display is static. In LOCK/ROLL mode the display is also normally static, but if the counter being used with the 5344S is a 5343A and the signal source is an HP 8350A sweeper, the Counter Trigger mode may be invoked on the 8350A to momentarily stop the sweep and signal the 5344S to measure a desired frequency (stop or marker). The 8350A's CNTR TRIG output must be connected to the 5343A's SWP INTFC A input. The sweeper's STOP SWEEP input must be connected to the 5344A's SWEEP TRIGGER output or to the 5343A's SWP INTFC B. Then selecting a frequency parameter on the 8350A front panel and pressing the SHIFT and M2 keys enables Counter Trigger mode. See *Figure 3-11* Lock/Roll In Manual or *Figure 3-15*, Lock/Roll In Auto Lock for a descriptive procedure.

3-111. OPERATOR'S CHECKS

3-112. 5342A/5343A Stand-Alone Operation

3-113. The 5344A and the 5342A/43A each have power switches that must be set to the ON position. The order in which they are turned-on doesn't matter. The 5342A (or 5343A) may be operated alone by applying power only to the counter. However,since the 5344A uses the counter's microprocessor, if both instruments are ON and the 5344A is switched OFF, the 5342A must be switched OFF, then ON, to return complete control to the 5342A. This is not required with the 5343A.

3-114. Power-Up Self Check

3-115. On power-up, the 5344S performs its self-test routine. If all tests pass, the 5344S performs its initialization and then passes control to the 5342A/43A which performs its own self-test and proceeds to free-run mode (5342A/43A counting; 5344A idle).

3-116. The power-up values for 5344S parameters are as shown in *Table 3-5:*

Table 3-5. 5344S Power-Up Parameters

MODE = CW
CW = STOP = START = 0
ΔF = 0
MARKERS = 0
SWEEP TIME = 10 ms
STEP SIZE = 0
FREQUENCY MULTIPLIER = 1
LOCK = OFF
RPG KNOB = COARSE
HP-IB: LOCAL
RM = 0

3-117. If during the power-up self-test a failure is detected, an error code will be displayed on the 5344A as follows:

Err 13 ..... Ux ROM Failure
Err 14 ..... RAM Failure

where x is the reference designation of the defective ROM located on the A11 Main ROM Buffer Assembly.

3-118. If one of these errors is displayed, refer to Section VIII, Service for further instructions.

3-119. ERRORS AND END OF SWEEP (----EOS----) MESSAGES

3-120. When an operational error is detected by the 5344S, such as an incorrect parameter, an error message is displayed on the 5344A front panel. The error message consists of "Err" followed by a two-digit error number. *Table 3-6* describes each error condition and the probable causes for it.

Table 3-6. ERROR Messages

Err 01. Invalid frequency measurement on 5344S.

a. Signal source output not connected to counter input.

b. Source power level too low.

c. Source RF OUT turned off.

d. Source RF BLANKING turned on when using Lock/Roll mode on 5344S.

e. Signal source frequency < 500 MHz or > 18 GHz (5342A) or 26.5 GHz (5343A).

f. Signal source sweeping or being manually tuned too fast.

g. Signal source internal square-wave modulation turned on.

h. Cables are defective or not usable over desired frequency range.

Err. 02. Markers too close to each other or to the STOP frequency.

Solution: Move markers or increase sweep time.

Err. 03. STOP frequency less than START frequency.

Err 04. STOP frequency - START frequency greater than 40 MHz.

Solution: Reduce sweep span.

Err 05. Signal source FM sensitivity less than 1 MHz/volt.

a. Sensitivity really is less than 1 MHz/volt.

b. 5344A FM OUT not connected to signal source FM INPUT.

c. For HP 86200 plug-ins; PL-NORM-FM switch in NORM position. (Should be in PL position).

d. For HP 83500 plug-ins: CW filter enabled.

e. 5344A A6 (Main Loop Board) fuse blown.

Err 06. Signal source FM sensitivity greater than 100 MHz/volt.

Err 07. Sweep too wide for signal source sensitivity.

Solution: Reduce sweep width.
Increase source FM sensitivity.

Err 08. Sweep cannot cross the frequencies of 500, 650 or 800 MHz.

Solution: Change sweep parameters.

Err 09. Invalid value calculated for Frequency Multiplier in Subharmonic Locking Mode.

a. Sweeper is not tuned close enough to desired frequency to allow reliable automatic determination of harmonic number.

Solution: Tune source closer to correct frequency.
Use AUTO LOCK (System Controller).

b. The 5344S has determined the harmonic number to be greater than four.

Solution: Enter the Frequency Multiplier manually.

Table 3-6. ERROR Messages (Continued)

Err 10. System controller switch not set to SYS CONT for AUTO LOCK. (ADDRESS switch on rear panel.)

Solution: Set switch to SYS. CONT.
Use Manual Lock.

Err 11. Signal source cannot be tuned close enough via HP-IB.

a. Signal source HP-IB port not connected to 5344A.

b. 5344A HP-IB address switch not set to address of signal source.

c. Signal source is not HP 8620C or HP 8350A.

d. Desired frequency is not within range of installed plug-in.

e. 8620C has plug-in installed that is not supported for Auto Lock, (86210A, 86220A, 8621A/B).

Err 12. AUTO LOCK cannot be achieved.

a. AUTO LOCK attempted in LOCK/ROLL mode with 8620A/B/C sweeper.

Solution: Use Manual Lock.

b. HP-IB address of sweeper and 5344A are not the same.

Err 13. Checksum error in power-up ROM test. Bad ROM number (U1, U4, U6, U8) also displayed.

Err 14. RAM failure during power-up self-test.

Err 15. Actual locking frequency out of range (500 MHz to 18 GHz for 5342A, or 500 MHz to 26.5 GHz for 5343A) in Subharmonic or Offset Locking mode.

3-121. End-of-Sweep (EOS) Message

3-122. The 5344A will display ----EOS---- when LOCK mode is entered or RESET is pressed, while waiting for the present sweep to be completed so that a locking sequence may be started. EOS is also displayed when the 5344S has triggered a sweep and is waiting for the sweeper to respond.

3-123. There are several possible causes for the EOS message to remain on the display of the 5344A:

a. The sweeper is set for long sweep times, and the present sweep has not yet been completed.

b. The SWEEP IN of the 5344A is not connected to the sweep ramp of the source.

c. The sweeper is not sweeping.

d. The sweeper's RF output is turned off for any length of time.

e. The sweeper is tuned out of the capture range of the 5344S.

f. The SWEEP TRIGGER out of the 5344S is not connected to the source.

3-124. SIGNAL SOURCE REQUIREMENTS

3-125. Signal sources to be used with 5344S must meet the following specifications:

1. Frequency and output power which meet the 5344S specifications of *Table 1-1.*

2. An FM port with a sensitivity between 1 and 50 MHz/volt and bandwidth of dc to at least 2 MHz in wideband mode, or dc to at least 200 KHz in narrowband mode. If the input impedance of the FM port is less than 5 Kohms, the sensitivity will be reduced by the output impedance of the 5344S FM OUT signal (250 ohms). The minimum sensitivity must then be $(R_{in} + 250)/R_{in}$ MHz/Volt, with R_{in} in ohms. The FM input bandwidth must also meet the minimum values with this 250 ohms in series with it. This is significant only if the input capacitance is large.

3-126. HP Signal Sources Used With the 5344S

3-127. The HP sweeper mainframes listed in *Table 3-7* meet the requirements listed in paragraph 3-125 over at least part of their range.

CAUTION

SEE PARAGRAPH 3-131 BEFORE CONNECTING THE 5344S TO THE 8640A/B. DAMAGE TO THE 8640A/B MAY RESULT IF A DIRECT CONNECTION IS MADE.

Table 3-7. HP Sweeper Mainframe/5344A Compatibility

Sweeper Mainframe	Compatibility
8350A Sweeper	MANUAL and full AUTO LOCK
8620A/B Sweeper	MANUAL LOCK only
8620C Sweeper (without Option 011)	MANUAL LOCK only
8620C Sweeper (with Option 011) except for AUTO LOCK/ROLL	MANUAL and AUTO LOCK
8640A/B Signal Generator	MANUAL LOCK only
8683A/B Signal Generator 8684A/B Signal Generator	Limited Capture Range and Sweep Width

3-128. HP Sweeper Plug-In/5344S Compatibility

3-129. *Table 3-8* lists the compatibility of the various HP sweeper plug-ins for the 8350A and 8620A/B/C.

Table 3-8. HP Sweeper Plug-In/5344A Compatibility

Plug-In	Sweeper 8620	Sweeper 8350	*Restrictions/Comments
83522A		X	1
83525A		X	1
83540A		X	1
83545A		X	1
83570A		X	1
83590A		X	1
83592A		X	1
83594A		X	1
83595A		X	1
8621A/B	X		2
86222A/B	X	X	5
86222A/B-H80	X	X	3; MLA
86230A/B	X	X	5
86235A	X	X	5
86235A-008	X	X	3; MLA
86240A/B	X	X	5
86240C	X	X	3; MLA
86241A	X	X	5
86242A/C/D	X	X	5
86242D-008	X	X	3; MLA
86245A	X	X	5
86245A-008	X	X	3; MLA
86250A/C/D	X	X	5
86250D-008	X	X	3; MLA
86260A	X	X	5
86260A-H82	X	X	3; MLA
86260B/C	X	X	5
86290A/B/C	X	X	5
86290A/B-H08	X	X	4,5

MLA-Microwave Link Analyzer

NOTES FOR RESTRICTIONS/COMMENTS:

1. The plug-in's "CW FILTER" switch must be turned off.
2. The "FM" position of the "FM-NORM-PL" switch must be used. ("PL" may operate, depending upon sensitivity). AUTO LOCK is not supported.
3. The "NORM" position of the "MLA-NORM" switch must be used. Capture range is limited.
4. AUTO LOCK with subharmonic locking (AUX OUT) will not operate with the 8620C Option 011 and this plug-in.
5. The "PL" or "FM" position of the "FM-NORM-PL" switch must be used.
6. The 86210A, 86220A, and 8690 series will not operate with the 5344S.

3-130. Throughout this manual, the 8350A Sweep Oscillator and an 83592A (.01 to 20.0 GHz) plug-in are used for examples and discussion. Since an 8620 series Sweep Oscillator may also be used, *Table 3-9* cross references the connectors (input/output) of the sweeper mainframe. Refer to *Table 3-7* for compatibility of the 8620 series mainframes with the 5344S.

Table 3-9. 8350A/8620 Series Connector Cross Reference

8350A	8620A/B/C	Function
SWEEP OUT/IN (Front/rear panel)	SWEEP OUT (Front panel)	0 to +10V ramp concurrent with sweep. Used to detect end of sweep.
EXT TRIGGER (pin 9 of the Programming Connector) SWEEP OUT/IN (Front-rear panel)	EXT TRIGGER (Rear panel)	Initiates a sweep.
CNTR TRG (Rear panel)	None	Output to externally trigger 5343A Counter
STOP SWEEP (Rear panel)	None	Input to stop progress of a forward sweep. For use with a 5343A Counter.
FM INPUT* (Rear panel)	None* (Located at rear of plug-in)	Frequency Modulation input

*Note: The FM input for 83500 series plug-ins is located on the rear panel of the 8350A mainframe. If an 86000 series plug-in is used with the 11869A RF Plug-in Adapter in the 8350A, the 86000 series FM input is routed to the 8350A rear panel FM INPUT. The 86200 series FM INPUT is not available at the rear of the plug-in.

3-131. Using the 5344S With an 8640A/B Signal Generator

3-132. The 8640A/B Signal Generator cannot safely handle the -10 Volt signal that the 5344S can apply to its FM input port. The circuit shown in *Figure 3-7* installed between the 5344S FM OUT and the 8640 FM INPUT will protect the 8640 from excessive voltage and does not degrade specified performance.

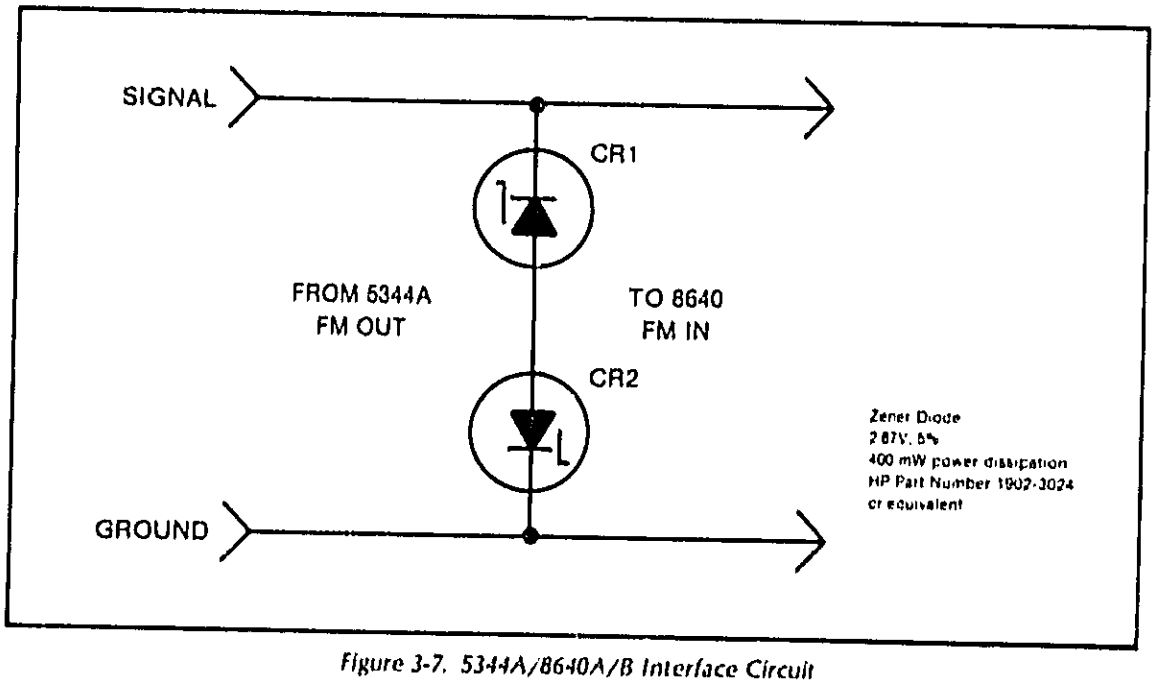


Figure 3-7. 5344A/8640A/B Interface Circuit

3-133. DETAILED OPERATING MODES

3-134. *Figures 3-8* through *3-16* detail the four modes of operation in Manual Lock and in Auto Lock mode. These figures include all required interconnections and operating procedures. This assumes the 5344A and 5342A/43A have been connected per paragraph 2-19. These examples use the HP 8350A Sweep Oscillator and an 83592A (.01 to 20.0 GHz). Change the parameters of the examples to fit your sweeper's frequency range.

3-135. The signal level at the input of the counter should be as specified in *Table 1-1*, Specifications. Power splitters and directional couplers attenuate the signal level, so be sure there is sufficient signal for the counter input. When placing an attenuating device in series with the signal would cause the level to drop below the required level, a feature called Subharmonic Locking is provided. This allows the signal source's output to be used without any attenuating devices. *Figure 3-17* details the Subharmonic Locking and *Figure 3-18* details the Frequency Offset Locking mode.

3-136. Common Control Problems

3-137. Most sweep oscillators have controls and functions that, if inadvertently turned-on, may cause problems when the 5344S tries to lock. For instance, if the square-wave modulation is on, the 5344S will not be able to follow the signal and lock will not be achieved. The following *Table* lists some of the common controls that may create problems.

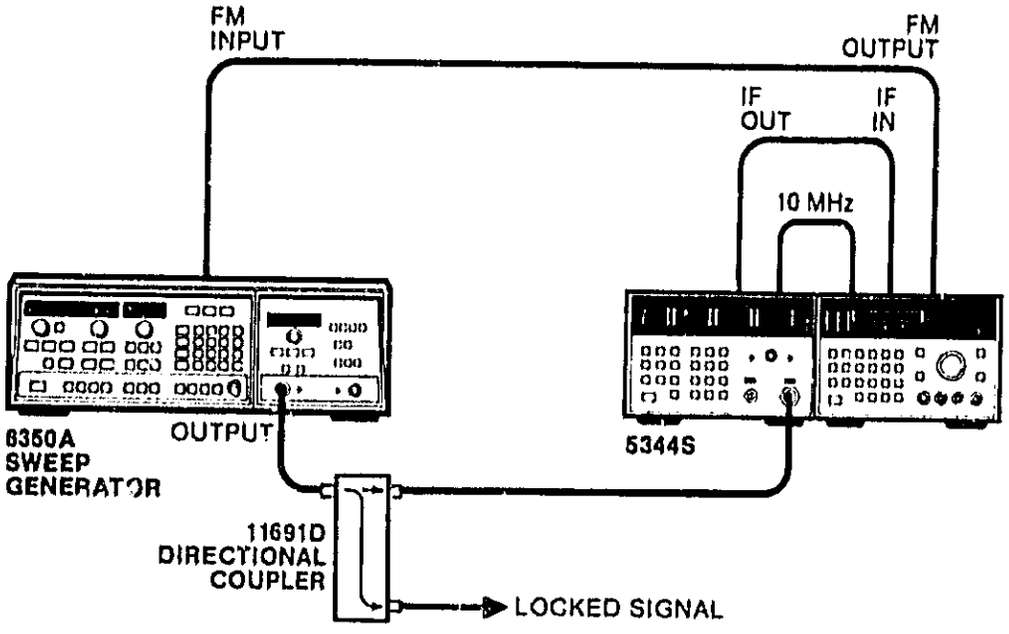
Table 3-10. Common Control Problems

1. Square-wave modulation turned-on or the signal being applied to the counter is being modulated in some form.
2. Sweeper's Amplitude Markers are turned-on.
3. CW filter is on.
4. RF Blanking is on during LOCK/ROLL.

Description:

The 5344S locks the signal source to the specified CW frequency. The signal source must be manually adjusted to within 25 MHz of the desired CW frequency.

Connections:



Example:

CW locked frequency at 2.000000000 GHz.

1. Set MANUAL LOCK and AUTO LOCK off (lamp off). If AUTO LOCK is turned on, the 5344A will display error code Err 10.
2. Select CW mode on the 8350A. If the plug-in has a CW filter, turn it OFF. Verify the counter SAMPLE RATE is not in HOLD.
3. Using the 8350A DATA ENTRY keys, press:

   [2] [GHz s]

   The 8350A should display 2.000 GHz and the 5342A should display approximately 2 GHz.
4. Using the 5344A Function keys, press:
   a. MODE until the CW annunciator lights. The MODE key will scroll through the four modes of operation. If you pass CW, continue pressing MODE until you return to CW.
5. Using the 5344A Numeric Entry keys, press:

   [2] [GHz s]

   The 5344A should display:

   2.000000000 GHz

   The 5344S always assumes that the remaining unentered digits are zero. Thus 1 Hz resolution always occurs.

Figure 3-8. CW in Manual

6. Press the 5344A MANUAL LOCK key.

   The LOCKED annunciator should light.

7. If the FREQ LO annunciator lights, manually raise the frequency of the 8350A until the 5342A displays 2 GHz ± 25 MHz. The 5344S will automatically tune the 8350A to the desired frequency.

8. If the FREQ HI annunciator lights, manually lower the frequency of the 8350A until the 5342A displays 2 GHz ± 25 MHz. The 5344S will automatically tune the 8350A to the desired frequency.

9. Notice that when either the FREQ HI or FREQ LO annunciators are on, indicating that tuning is required, the resolution on the counter decreases to 1 KHz. This allows a very fast update of the counter display making tuning quicker and easier.

NOTE

The 5344S will display error code Err 01 if the frequency of the sweeper is changing too fast for the 5344S to follow. This may occur for the following reasons:

a. The sweeper is sweeping,

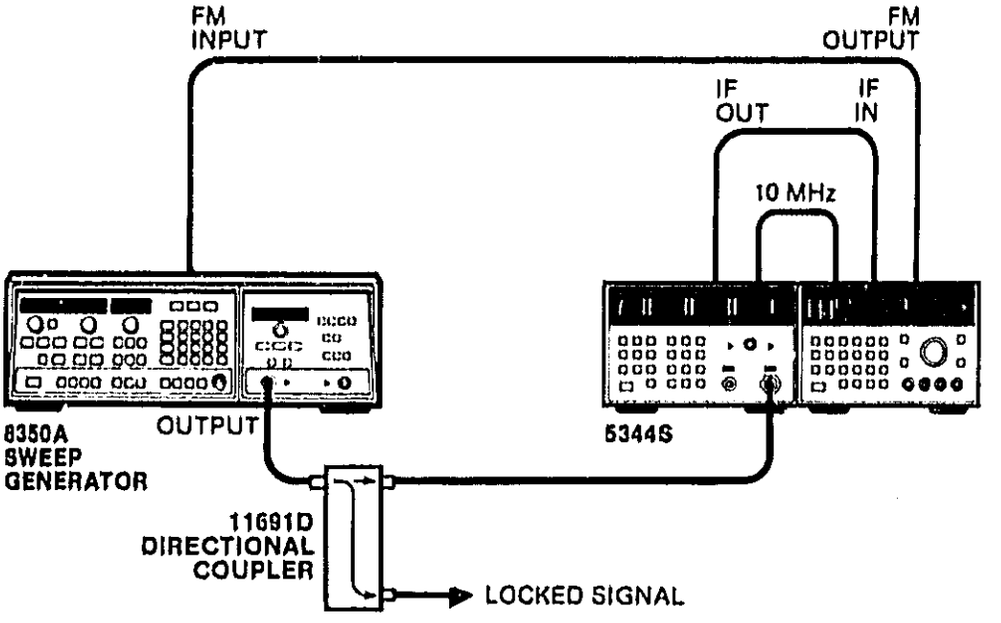
b. or when manually tuning the sweeper, it is being tuned too quickly.

Figure 3-8. CW in Manual (Continued)

Description:

The 5344S will lock the sweeper to the specified Center Frequency, and then sweep in a range around the CF as specified by the ΔF (sweep width), by the Sweep Time specified on the 5344A.

Connections:



Example:

Center Frequency (CF) of 2 GHz and a sweep width (ΔF) of 20 MHz. The 5344S will sweep the source from CF-(ΔF/2) to CF+(ΔF/2) or 1.990 GHz to 2.010 GHz.

1. Set MANUAL LOCK and AUTO LOCK off (lamp off). If AUTO LOCK is turned on, the 5344A will display error code Err 10.
2. Select CW mode on the 8350A. If the plug-in has a CW filter, turn it OFF.
3. Using the 8350A DATA ENTRY keys, press:

   [2] [GHz s]

   the 8350A should display 2.000 GHz and the 5342A should display approximately 2 GHz.
4. Using the 5344A Function keys, press:
   a. MODE until the CF/ΔF annunciator lights. The MODE key will scroll through the four modes of operation. If you pass CF/ΔF, continue pressing MODE until you return to CF/ΔF.
5. Using the 5344A Numeric Entry keys, press:

   [2] [GHz s]

   The 5344A should display:

   2.000000000 GHz

   The 5344S always assumes that the remaining unentered digits are zero. Thus, 1 Hz resolution always occurs.
6. Press the F2 key on the 5344A. The LED inside the key will light to indicate that it is waiting for data to be entered and the entered value will be shown on the display.

Figure 3-9. CF/ΔF in Manual

7. Using the 5344A Numeric Entry keys, press:

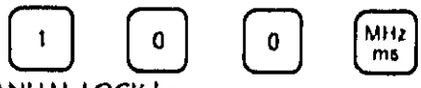
The 5344A should display:

20.000000 MHz

To see the Center Frequency value, press key F1. Unless Numeric Entry keys are pressed, the value will remain unchanged. If an invalid value is entered, the previous value will remain unchanged. If a value outside of the limits is entered, the value will default to the closest limit.

8. Press the 5344A SWP TIME key. The LED inside of the key will light to indicate that it is waiting for data to be entered.

9. Using the 5344A Numeric Entry keys, press:



10. Press the 5344A MANUAL LOCK key.

The LOCKED annunciator should light.

11. If the FREQ LO annunciator lights, manually raise the frequency of the 8350A until the 5342A displays 2 GHz (±15 MHz). The 5344S will automatically tune the 8350A to the desired frequency.

12. If the FREQ HI annunciator lights, manually lower the frequency of the 8350A until the 5342A displays 2 GHz (±15 MHz). The 5344S will automatically tune the 8350A to the desired frequency.

13. Notice that when either the FREQ HI or FREQ LO annunciators are on, indicating that tuning is required, the resolution on the counter decreases to 1 KHz. This allows a very fast update of the counter display making tuning quicker and easier. The sweep is also halted until Lock is achieved.

NOTE

The 5344S will display error code Err 01 if the frequency of the sweeper is changing too fast for the 5344S to follow. This may occur for the following reasons:

a. The 8350A is in SWEEP mode (vs. CW) and is sweeping, or

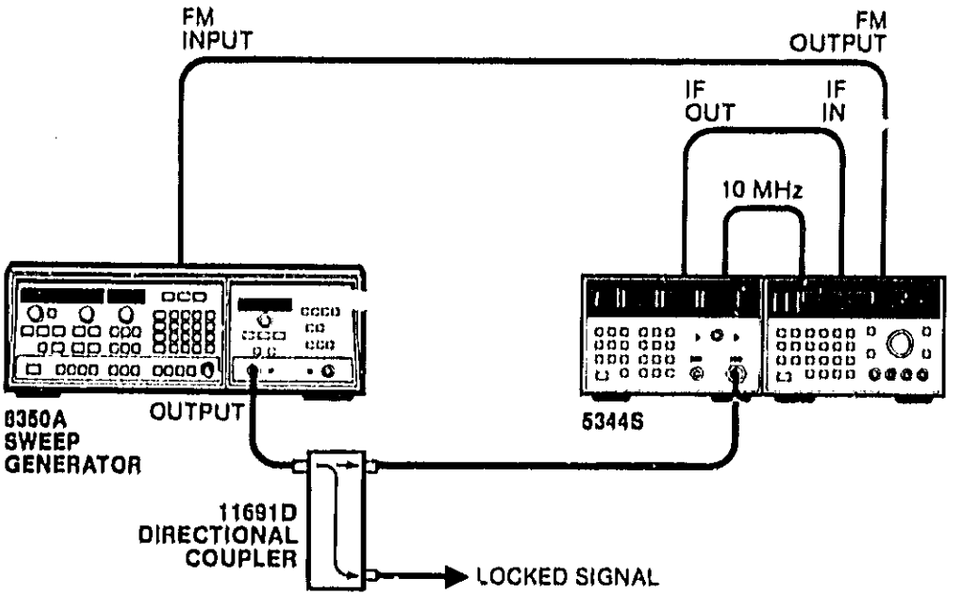
b. When manually tuning the 8350A to within 15 MHz, it is being tuned too quickly.

Figure 3-9. CF/ΔF in Manual (Continued)

Description:

The 5344S will lock the sweeper to the specified Start Frequency and then sweep from the specified Start Frequency to the specified Stop Frequency by the specified Sweep Time. The difference between the Start and Stop frequency must be less than 40 MHz. The Sweep Time range is 10 ms-100 s.

Connections:



Example:

Start Frequency (STRT) of 2 GHz and a Stop Frequency Stop (STOP) of 2.040 GHz.

1. Set MANUAL LOCK and AUTO LOCK off (lamp off). If AUTO LOCK is turned on the 5344A will display error code Err 10.
2. Select CW mode on the 8350A. If the plug-in has a CW filter, turn it OFF.
3. Using the 8350A DATA ENTRY keys, press:

   [2] [.] [0] [2] [GHz]

   The 8350A should display 2.020 GHz and the 5342A should display approximately 2.02 GHz.
4. Using the 5344A Function keys, press:
   a. MODE until STRT/STOP annunciators lights. The F1 key will light indicating the 5344A is waiting for a START frequency value. The MODE key will scroll through the four modes of operation. If you pass STRT/STOP, continue pressing MODE until you return to STRT/STOP.
5. Using the 5344A Numeric Entry keys, press:

   [2] [GHz]

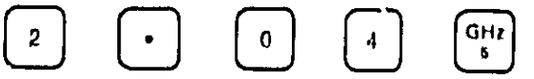
   The 5344A should display:

   2.000000000 GHz

   The 5344S always assumes that the remaining unentered digits are zero. Thus 1 Hz resolution always occurs.

Figure 3-10. Start/Stop in Manual

6. Press the F2 key on the 5344A. The LED inside the key will light to indicate that it is waiting for a STOP frequency to be entered and the entered value will be shown on the display.
7. Using the 5344A Numeric Entry keys, press:



the 5344A should display:

2.040000000 GHz

To see the START Frequency value, press key F1. Unless Numeric Entry keys are pressed, the value will remain unchanged. If an invalid value is entered, the previous value will remained unchanged. If a value outside of the limits is entered, the value will default to the closest limit.

SWP TIME

8. Press the 5344A  key.

   The LED inside the key will light to indicate that the 5344A is waiting for Sweep Time value to be entered.

9. Using the 5344A Numeric Entry keys press:

   the 5344A will display:

   100 ms

10. Press the 5344A MANUAL LOCK key.

    The LOCKED annunciator should light.

11. If the FREQ LO annunciator lights, manually raise the frequency of the 8350A until the 5342A displays 2.02 GHz ±15 MHz. The 5344S will automatically tune the 8350A to the desired frequency.
12. If the FREQ HI annunciator lights, manually lower the frequency of the 8350A until the 5342A displays 2 GHz (±15 MHz). The 5344S will automatically tune the 8350A to the desired frequency.
13. Notice that when either the FREQ HI or FREQ LO annunciators are on indicating that tuning is required, the resolution on the counter decreases to 1 KHz. This allows a very fast update of the counter display making tuning quicker and easier. The sweep is also halted until Lock is achieved.

NOTE

The 5344S will display error code Err 01 if the frequency of the sweeper is changing too fast for the 5344S to follow. This may occur for the following reasons:

a. The 8350A is in SWEEP mode (vs. CW) and is sweeping, or
b. When manually tuning the 8350A to within 15 MHz it is being tuned too quickly.

Figure 3-10. Start/Stop in Manual (Continued)

Description:

The 5344S will lock the sweeper to the Start Frequency selected on the 5344A, and then sweep to the Stop Frequency selected on the 8350A by the Sweep Time also selected on the 8350A.

Connections:

There are two possible interconnections (listed below) for Lock and Roll. Use the one that is most convenient. The optional configuration is provided for applications requiring use of the programming connector that would make connection to the sweeper's EXT TRIGGER pin difficult.

Preferred:

Pin 9 of the 8350A Programming Connector to the 5344A rear panel SWP TRIG. Use the supplied adapter HP Part No. 8120-3545.

Settings:

8350A SWEEP mode in TIME.

8350A SWEEP TRIGGER in EXT.

Optional:

8350A rear panel STOP SWEEP to the 5344A SWP TRIG.

Settings:

8350A SWEEP mode to TIME.

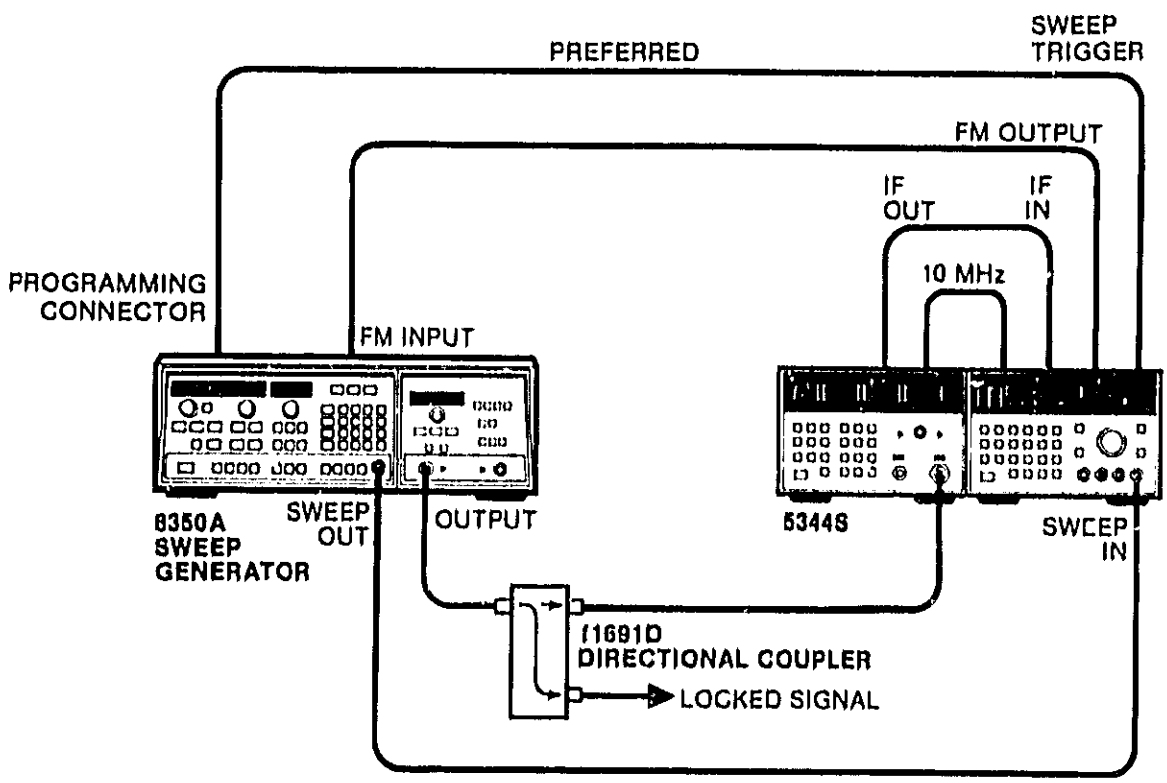


Figure 3-11. Lock and Roll in Manual

Example:

Start Frequency (F1) of 2 GHz and a Stop Frequency (F2) of 4 GHz with a Sweep Time of 100 ms.

1. Set MANUAL LOCK and AUTO LOCK off (lamp off.) If AUTO LOCK is turned on, the 5344A will display error code Err 10.
2. Select Start/Stop mode on the 8350A. If the plug-in has a CW filter, turn it OFF.
3. Using the 8350A DATA ENTRY keys, press:

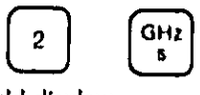
START	and then,	2		GHz	
STOP	and then,	4		GHz	
SWEEP TIME	and then,	1	0	0	ms

EXT trigger; If the SWEEP TRIGGER is connected to the 8350A EXT TRIG.

INT or LINE trigger if the SWEEP TRIG is connected to the 8350A STOP SWEEP.

The 8350A should display 2.000 GHz on the START display, 4.000 GHz on the STOP display, and 0.100 SEC on the Frequency/Time display.

4. Using the 5344A Function keys, press:
   a. MODE until the LK/R annunciator lights. The MODE key will scroll through the four modes of operation. If you pass LK/R, continue pressing MODE until you return to LK/R.
5. Using the 5344A Numeric Entry keys, press:



the 5344A should display:

2.000000000 GHz

The 5344S always assumes that the remaining unentered digits are zero. Thus, 1 Hz resolution always occurs.

6. Press the 5344A MANUAL LOCK key.

   The LOCKED annunciator should light.

7. If the FREQ LO annunciator lights, manually raise the frequency of the 8350A until the 5342A displays 2 GHz (±25 MHz). The 5344S will automatically tune the 8350A to the desired frequency.
8. If the FREQ HI annunciator lights, manually lower the frequency of the 8350A until the 5342A displays 2 GHz (±25 MHz). The 5344S will automatically tune the 8350A to the desired frequency.
9. Notice that when either the FREQ HI or FREQ LO annunciators are on indicating that tuning is required, the resolution on the counter decreases to 1 kHz. This allows a very fast update of the counter display making tuning quicker and easier. The sweep is also halted until Lock is achieved.

NOTE

In Lock/Roll, the signal source is locked only (briefly) at the start of each sweep. It is possible for the sweep settings to be changed during the unlocked portion of the sweep such that the starting frequency is changed by some near multiple of the current local oscillator frequency of the counter. This will result in lock being regained at the end of the current sweep, even though the frequency is nowhere near that desired. To avoid this situation, do not change any settings during a sweep. If you do get into this situation, press RESET to restart the locking algorithm.

Figure 3-11. Lock and Roll in Manual (Continued)

Due to the design of the 8350A sweeper, manually tuning it for LOCK/ROLL operation with the optional configuration is less convenient than when using the preferred method. For sweep times less than or equal to 100 ms, the 8350A waits until the end of a sweep before updating the output frequency to reflect the changes made at the front panel. Since the 5344A stops the sweep to allow tuning of the sweeper's start frequency, turning the 8350A's RPG or using its keyboard changes the sweeper's frequency display, but does not actually change the output. To change the start frequency, press EXT SWEEP TRIGGER on the 8350A front panel while tuning the LOCK/ROLL start frequency. This forces an immediate update to the output frequency. After the sweeper has been tuned and the 5344S locks, press EXT or LINE SWEEP TRIGGER to start the sweep. Alternatively, the 8350A's SWEEP TIME can be set greater than 100 ms for tuning, then returned to the actual desired value after lock is achieved.

Counting Sweeper Markers or Stop frequency:

If the counter being used with the 5344A is a 5343A, the markers of the 8350A or Stop frequency of the sweep can be counted during Lock and Roll (only the sweeper can generate markers during Lock and Roll). The following connections are required for this feature:

With the preferred method:

8350A CNTR TRIG to the 5343A rear panel SWP INTFC A

8350A STOP SWEEP to the 5343A rear panel SWP INTFC B

With the optional method:

8350A CNTR TRIG to the 5343A SWP INTFC A

After setting up the Lock/Roll sweep, you can count the markers or Stop frequency by:

1. Pressing STOP on the 8350A. This selects which parameter is to be measured by the 5343A.
2. Pressing:

[SHIFT] (blue key) [M2] on the 8350A.

This enables the counter interface function on the 8350A.

Whenever the 5344S Option 043 is locked in Lock/Roll, the sweeper interface function of the 5344S is automatically enabled. If the 5344S is not locked, simply press SWP MI on the 5343A to enable the sweeper interface.

If you wish to count one of the markers on the 8350A, the operation is quite similar, except that you would select the marker you wish to count in Step 1 above, rather than the sweeper STOP frequency.

To disable the sweeper/counter interface feature, press:

[SHIFT] (blue key) [M3] on the 8350A.

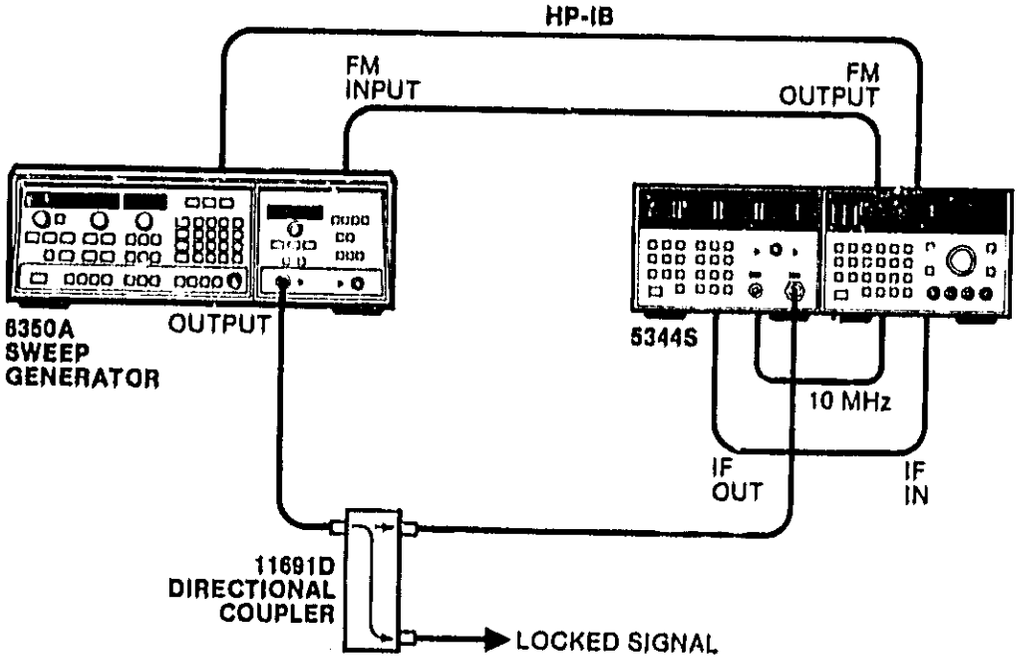
Figure 3-11. Lock and Roll in Manual (Continued)

Description:

The 5344S locks the signal source to the specified CW frequency. The signal source is automatically tuned by the 5344S. No manual tuning is required.

Connections:

1. The address of the 8350A Sweep Oscillator must be set to the same address as the 5344A. The top switch of the 5344A ADDRESS switches must be set to the SYS CONT position.



Example:

CW locked frequency at 2.000000000 GHz.

1. Set the 5344A HP-IB address to 00 by setting the bottom five switches to the right.
2. Set the 5344A to the System Controller mode by setting the top HP-IB switch to the left (SYS CONT.).
3. Set the 8350A address to 00 (equal to the 5344A) by pressing the following key sequence:

The HP-IB address will be shown on the Frequency/Time display of the 8350A.

4. Set MANUAL LOCK and AUTO LOCK off (lamp off) and verify the 5344A front panel CCUNT lamp is on. Also verify the plug-in's CW Filter is off.
5. Using the 5344A Function keys, press and release MODE until the CW annunciator lights. The MODE key will scroll through the four modes of operation. If you pass CW, continue pressing MODE until you return to CW.

Figure 3-12. CW in AUTO LOCK

6. Using the 5344A Numeric Entry keys press:

   [2] [GHz]

   The 5344A should display:

   2.000000000 GHz

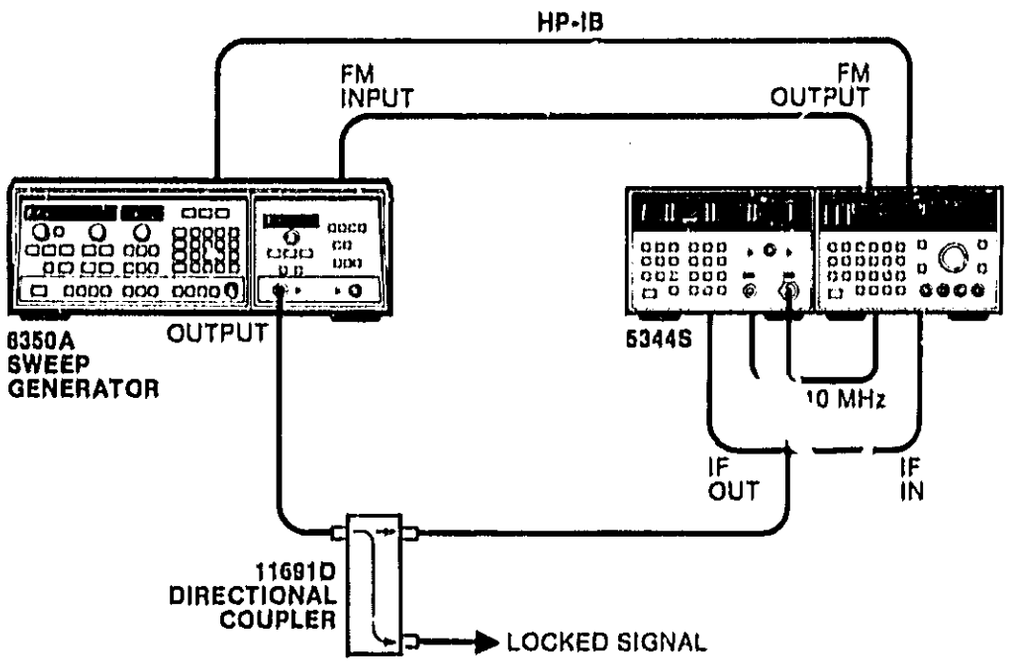
7. Press the 5344A AUTO LOCK key. The 5344A will now program the 8350A to the specified CW frequency. If the 8350A actual output frequency is not within the lock range of the 5344A, the 5344S will begin stepping the frequency in an attempt to bring it within range. If it is unsuccessful, Err 11 will be displayed. This is a possible indication that the 8350A and/or its plug-in is out of electrical alignment.

Figure 3-12. CW in AUTO LOCK (Continued)

Description:

The 5344S will lock the sweeper to the specified Center Frequency, and then sweep in a range around the CF as specified by the ΔF (sweep width) by the Sweep Time specified on the 5344A.

Connections:



Example:

Center Frequency (CF) of 2 GHz and a sweep width (ΔF) of 20 MHz. The 5344S will sweep the sweeper from CF-(ΔF/2) to CF+(ΔF/2) or 1.990 GHz to 2.010 GHz.

1. Set the 5344A HP-IB address to 00 by setting the bottom five switches to the right.
2. Set the 5344A to the System Controller mode by setting the top HP-IB switch to the left (SYS CONT.)
3. Set the 8350A address to 00 (equal to the 5344A) by pressing the following key sequence:

   [SHIFT] (blue key) [LCL] [0] [GHz 5]

   The HP-IB address will be shown on the Frequency/Time display of the 8350A.
4. Set MANUAL LOCK and AUTO LOCK off (lamp off) and verify the 5344A front panel CONT lamp is on. Also verify the plug-in's CW Filter is off.
5. Using the 5344A Function keys, press and release MODE until the CF/ΔF annunciator lights. The MODE key will scroll through the four modes of operation. If you pass CF/ΔF, continue pressing MODE until you return to CF/ΔF. The LED inside the F1 key will light.
6. Using the 5344A Numeric Entry keys press:

   [2] [GHz 5]

   The 5344A should display: 2.000000000 GHz

Figure 3-13. CF/ΔF in AUTO LOCK

7. Press the F2 key on the 5344A. The LED inside the key will light to indicate that it is waiting for data to be entered and the entered value will be shown on the display.
8. Using the 5344A Numeric Entry keys press:

The 5344A should display:

20.000000 MHz

If you want to see the Center Frequency value, press key F1. Unless Numeric Entry keys are pressed, the value will remain unchanged. If an invalid value is entered, the previous value will remain unchanged. If a value outside of the limits is entered, the value will default to the closest limit.

9. Press the 5344A SWP TIME key. The LED inside the key will light to indicate that the 5344A is waiting for a Sweep Time value to be entered.
10. Using the 5344A Numeric Entry keys, press:

the 5344A will display:

100 ms

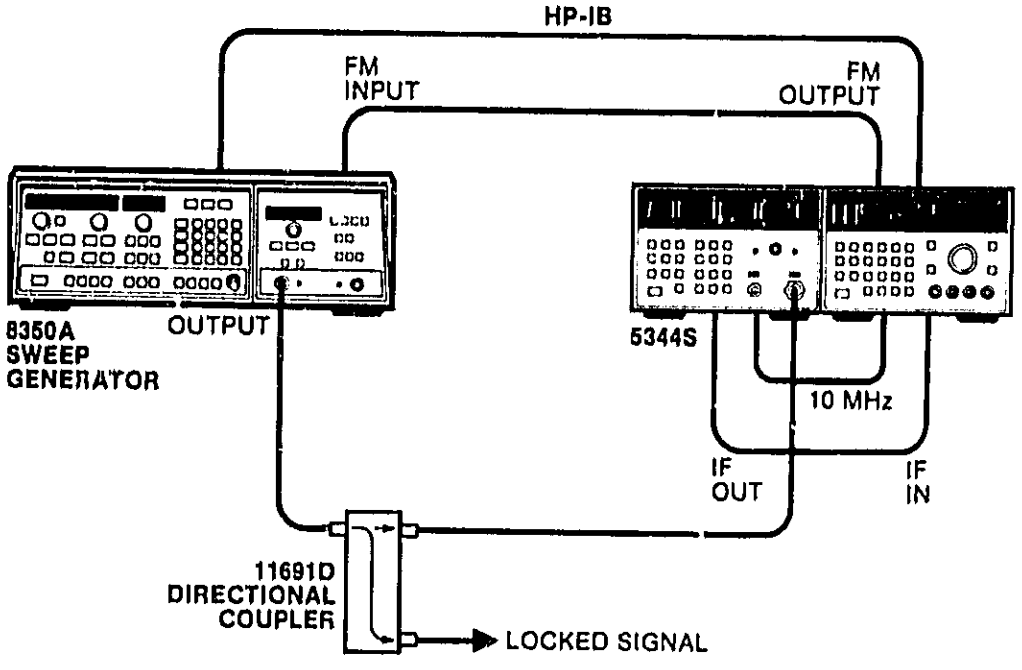
11. Press the 5344A AUTO LOCK key. The 5344A will now program the 8350A to the specified CF frequency, and then sweep over the specified ΔF range. The LOCKED annunciator should light. If the 8350A actual output frequency is not within the lock range of the 5344A, the 5344S will begin stepping the frequency in an attempt to bring it within range. If it is unsuccessful, Err 11 will be displayed. This is a possible indication that the 8350A and/or its plug-in is out of electrical alignment.

Figure 3-13. CF/ΔF in AUTO LOCK (Continued)

Description:

The 5344S will lock the sweeper to the specified Start Frequency, and then sweep from the specified Start Frequency to the specified Stop Frequency using the specified Sweep Time. The difference between the Start and Stop frequency must be less than or equal to 40 MHz. The Sweep time range is 10 ms-100 s.

Connections:



Example:

Start Frequency (STRT) of 2 GHz and a Stop Frequency Stop (STOP) of 2.040 GHz with a Sweep Time of 100 mS.

1. Set the 5344A HP-IB address to 00 by setting the bottom five switches to the right.
2. Set the 5344A to the System Controller mode by setting the top HP-IB switch to the left (SYS CONT.)
3. Set the 8350A address to 00 (equal to the 5344A) by pressing the following key sequence:

4. Set MANUAL LOCK and AUTO LOCK off (lamp off) and verify the 5344A front panel CONT lamp is on. Also verify the plug-in's CW Filter is off.
5. Using the 5344A Function keys, press and release MODE until the START/STOP annunciator lights. The F1 key will light indicating the 5344A is waiting for a START frequency value. The MODE key will scroll through the four modes of operation. If you pass STRT/STOP, continue pressing MODE until you return to STRT/STOP. The F1 key will light.

Figure 3-14. Start/Stop in AUTO LOCK

6. Using the 5344A Numeric Entry keys press:

The 5344A should display:

2.000000000 GHz

7. Press the F2 key on the 5344A. The LED inside the key will light to indicate that it is waiting for a STOP frequency to be entered and the entered value will be shown on the display.

8. Using the 5344A Numeric Entry keys press:

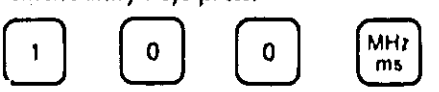
The 5344A should display:

2.040000000 GHz

If you want to see the START Frequency value, press key F1. Unless Numeric Entry keys are pressed, the value will remain unchanged. If an invalid value is entered, the previous value will remain unchanged.

9. Press the 5344A SWP TIME key. The LED inside the key will light to indicate that the 5344A is waiting for a Sweep Time value to be entered.

10. Using the 5344A Numeric Entry keys press:



The 5344A will display:

100 ms

11. Press the 5344A AUTO LOCK key. The 5344A will now program the 8350A to the center of the specified Start/Stop frequency range, and then sweep from Start to Stop. The LOCKED annunciator should light. If the 8350A actual output frequency is not within the lock range of the 5344A, the 5344A will begin stepping the frequency in an attempt to bring it within range. If it is unsuccessful, Err 11 will be displayed. This is a possible indication that the 8350A and/or its plug-in is out of electrical alignment.

Figure 3-14. Start/Stop in AUTO LOCK (Continued)

NOTE

Lock and Roll in Auto Lock will not operate with an 8620 series sweep oscillator.

Description:

The 5344S will lock the sweeper to the Start Frequency selected on the 5344A and then sweep to the Stop Frequency selected on the 8350A by the Sweep Time also selected on the 8350A.

Connections:

There are two possible interconnections for Lock and Roll. Use the one that is most convenient. The optional configuration is provided for applications requiring use of the programming connector that would make connection to the sweeper's EXT TRIGGER pin difficult.

Preferred:

Pin 9 of the 8350A Programming Connector to the 5344A rear panel SWP TRIG. Use the supplied adapter HP Part No. 8120-3545.

Settings:

8350A Sweep mode in TIME.
8350A Sweep Trigger in EXT.

Optional:

8350A rear panel STOP SWEEP to the 5344A SWP TRIG.

Settings:

8350A Sweep mode to TIME.
8350A Sweep Trigger to INT or LINE.

Connections:

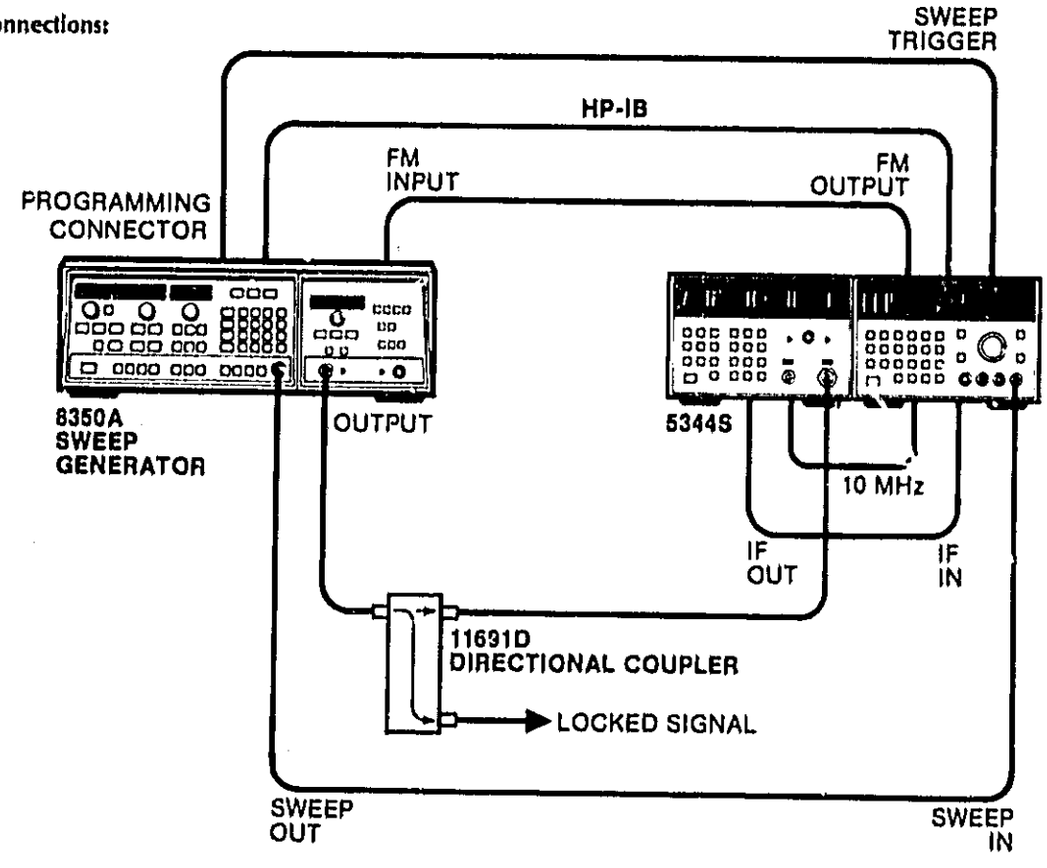


Figure 3-15. Lock and Roll in AUTO LOCK

Example:

Start Frequency of 2 GHz and a Stop Frequency of 5 GHz with a Sweep Time of 100 mS.

1. Set the 5344A HP-IB address to 00 by setting the bottom five switches to the right.
2. Set the 5344A to the System Controller mode by setting the top HP-IB switch to the left (SYS CONT.).
3. Set the 8350A address to 00 (equal to the 5344A) by pressing the following key sequence:

   [SHIFT] (blue key) [LCL] [0] [GHz s]

4. Set MANUAL LOCK and AUTO LOCK off (lamp off) and verify the 5344A front panel CONT lamp is on. Also verify the plug-in's CW Filter is off.
5. Using the 5344A Function ke; press and release MODE until the LK/R annunciator lights. The MODE key will scroll through the modes of operation. If you pass LK/R, continue pressing MODE until you return to LK/R.
6. Using the 5344A Numeric Entry keys, press:

   [2] [GHz s]

   The 5344A should display:

   2.000000000 GHz

7. Now enter the Stop frequency on the 8350A. Using the 8350A keys, press the following keys in sequence:

   [STOP] [5] [GHz s]

   The 8350A STOP display should be:

   5.00 GHz

8. Now enter the Sweep Time. Using the 8350A keys, press the following in sequence:

   [TIME] [1] [0] [0] [MHz ms]

   The 8350A TIME display should be:

   0.100 SEC

9. Press the 5344A AUTO LOCK key. The 5344A will now program the 8350A to the specified Start Frequency, and then sweep from Start to Stop. The LOCKED annunciator should light. If the 8350A actual output frequency is not within the lock range of the 5344A, the 5344A will begin stepping the frequency in an attempt to bring it within range. If it is unsuccessful, Err 11 will be displayed. This is a possible indication that the 8350A and/or its plug-in is out of electrical alignment.

Counting Markers or Stop frequency:

If the counter being used with the 5344A is a 5343A, the markers or Stop frequency of the sweep can be counted during Lock and Roll. The following connections are required for this feature:

With the preferred method:

8350A CNTR TRIG to the 5343A rear panel SWP INTFC A

8350A STOP SWEEP to the 5343A rear panel SWP INTFC B

Figure 3-15. Lock and Roll in AUTO LOCK (Continued)

With the optional method:

8350A CNTR TRIG to the 5343A SWP INTFC A

After setting up the Lock/Roll sweep, you can count the markers or Stop frequency by:

1. Pressing STOP on the 8350A. This selects which parameter is to be measured by the 5343A.
2. Pressing:

SHIFT (blue key) M2 on the 8350A.

This enables the counter interface function on the 8350A.

Whenever the 5344S Option 043 is locked in Lock/Roll, the sweeper interface function of the 5344S is automatically enabled. If the 5344S is not locked, simply press SWP M on the 5343A to enable the sweeper interface.

If you wish to count one of the markers on the 8350A, the operation is quite similar except that you would select the marker you wish to count in Step 1 above, rather than the sweeper STOP frequency.

To disable the sweeper/counter interface feature, press:

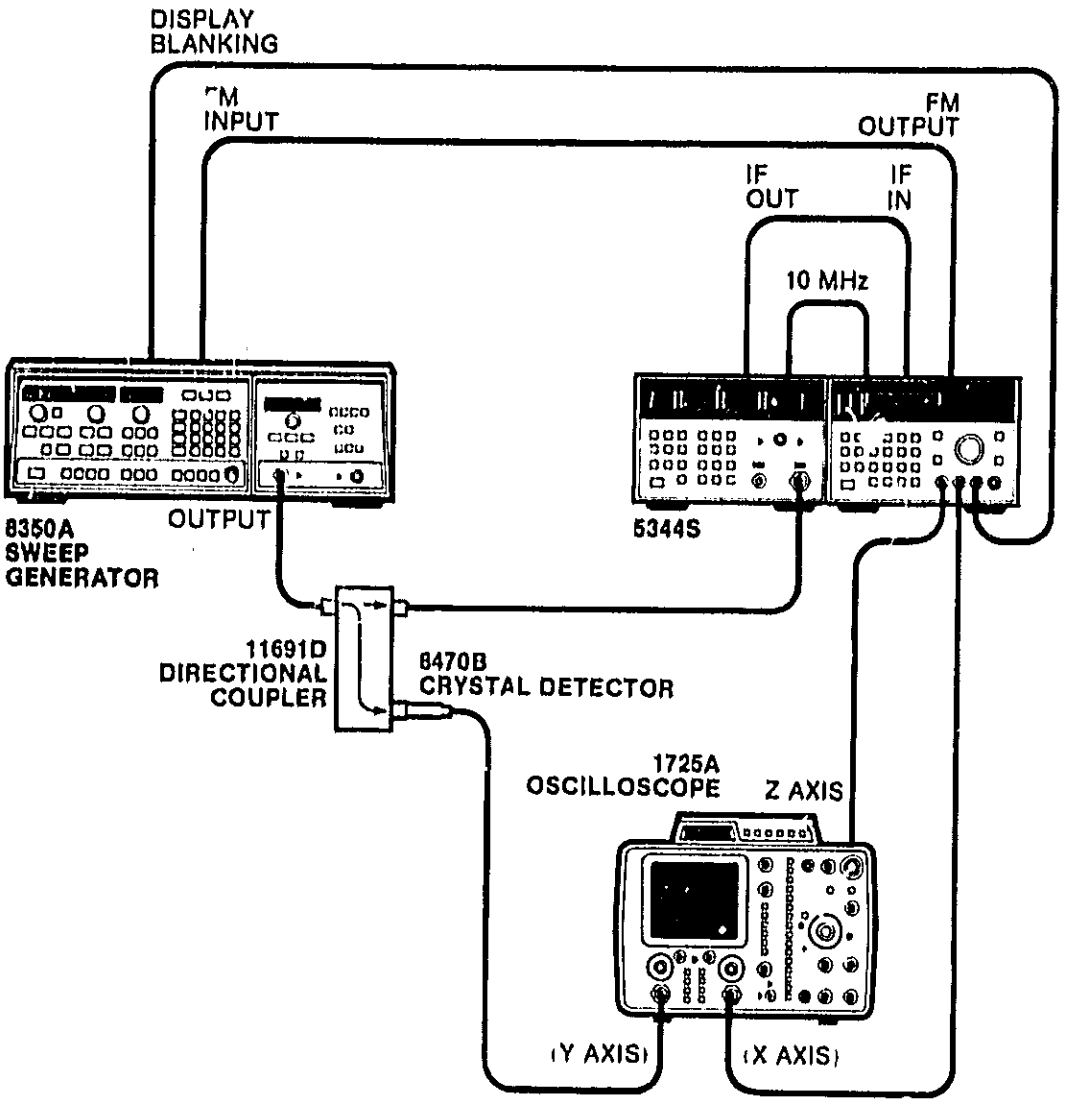
SHIFT (blue key) M3 on the 8350A.

Figure 3-15. Lock and Roll in AUTO LOCK (Continued)

Description:

The 5344S can generate 4 markers in CF/ΔF and Start/Stop mode.

Connections:



Example:

The 5344S will sweep from 2 GHz to 2.040 GHz generating one marker at the center of the sweep.

1. Set MANUAL LOCK and AUTO LOCK off (lamp off). If AUTO LOCK is turned on the 5344A will display error code Err 10.
2. Select CW mode on the 8350A. If the plug-in has a CW filter, turn it OFF.
3. Using the 8350A DATA ENTRY keys press:

The 8350A should display 2.020 GHz and the 5342A should display 2.02 GHz ±10 MHz.

Figure 3-16. Markers

4. Using the 5344A Function keys, press and release MODE until the START/STOP annunciator lights. The F1 key will light indicating the 5344A is waiting for a START frequency value. The MODE key will scroll through the four modes of operation. If you pass STRT/STOP, continue pressing MODE until you return to STRT/STOP.

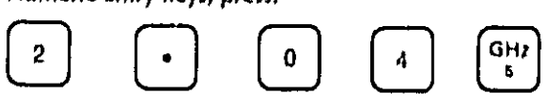
5. Using the 5344A Numeric Entry keys, press:

The 5344A should display:

2.000000000 GHz

6. Press the F2 key on the 5344A. The LED inside the key will light to indicate that it is waiting for a STOP frequency to be entered and the entered value will be shown on the display.

7. Using the 5344A Numeric Entry keys, press:



The 5344A should display:

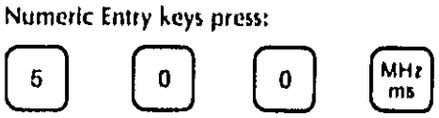
2.040000000 GHz

If you want to see the START Frequency value, press key F1. Unless Numeric Entry keys are pressed the value will remain unchanged. If an invalid value is entered the previous value will remain unchanged.

8. Press the 5344A SWP TIME key.

The LED inside the key will light to indicate that the 5344A is waiting for Sweep Time value to be entered.

9. Using the 5344A Numeric Entry keys press:



The 5344A will display:

500 ms

10. Press the 5344A MANUAL LOCK key.

The LOCKED annunciator should light.

11. Set the oscilloscope for an X-Y display. Adjust the Horizontal gain for a full width trace and center the trace with the vertical gain.

12. Press the 5344A MKR FREQ key. The lamp inside of the key will flash indicating the 5344A is waiting for one of the marker registers (1 through 4) to be selected.

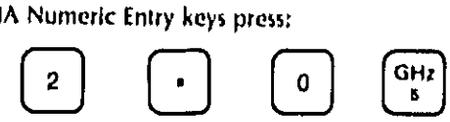
13. Using the 5344A Data Entry keys, select Marker one by pressing key 1.

14. Unless a marker has been previously entered, the 5344A should display:

0.000000 MHz

This indicates Marker 1 is OFF.

15. Using the 5344A Numeric Entry keys press:



The marker should now be seen on the oscilloscope screen as an intensified dot.

16. Now rotate the RPG knob clockwise and note the dot moves toward the right side of the sweep trace. The Marker 1 frequency is being increased toward the Stop frequency. When the marker frequency equals the Stop frequency, or it violates minimum marker spacing restrictions described in paragraph 3-47, Err 02 is displayed and the marker is ignored.

Figure 3-16. Markers (Continued)

17. Now rotate the RPG knob counter-clockwise. The marker will reappear on the trace. Move the marker towards the Start frequency. Again when the marker is too close to the Start frequency, or it violates the minimum separation restrictions described in paragraph 3-46, the marker will disappear. However, when the marker is too close to the Start frequency, no error is displayed.
18. Move marker 1 up to 2.01 GHz.
19. As described in steps 13 and 15, select Marker 2 and place it at 2.030 GHz.

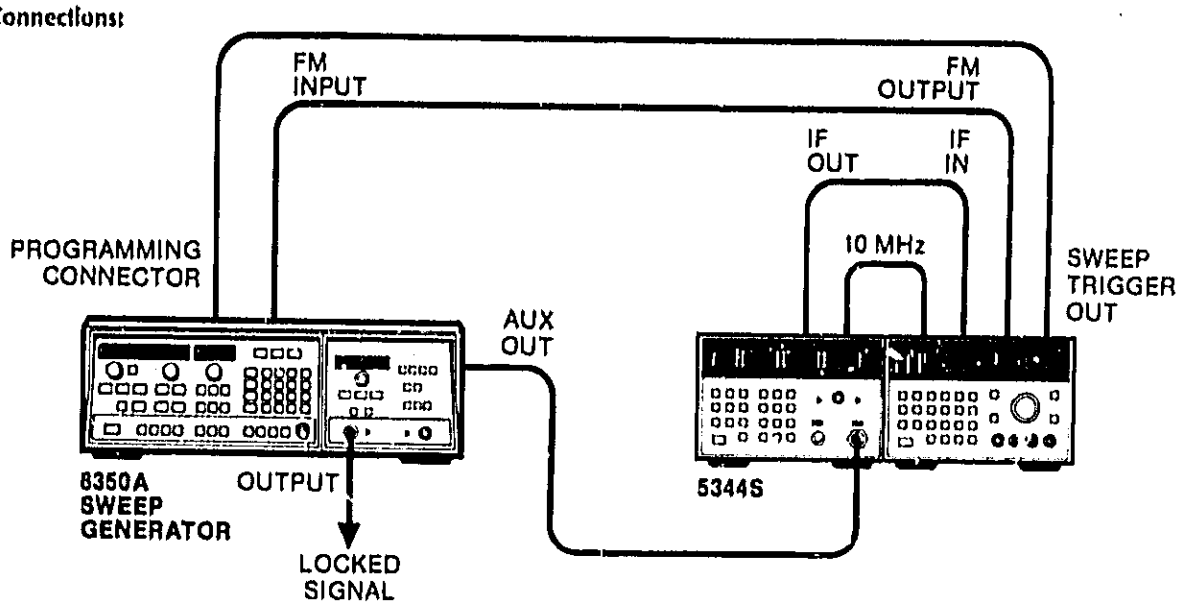
    You should now see two dots on the sweep trace.
20. Again using the RPG knob, move Marker 2 down towards Marker 1. Notice that when Marker 2 becomes too close to Marker 1, Marker 2 disappears. Whenever any two markers conflict, the higher frequency conflicting marker is ignored. The marker will always return once the spacing conflict is resolved.
21. Select Marker 3 and place it at 2.02 GHz.
22. Two more markers could be selected provided there is no conflict.

Figure 3-16. Markers (Continued)

Description:

This procedure will demonstrate Subharmonic Locking. The actual front panel output frequency will be 15 GHz. To avoid placing any attenuating devices in series with the output, the rear panel AUX OUT (YTO) will be used for the locking signal. The Frequency Multiplier will be set to 1 for automatic determination.

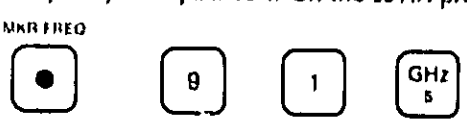
Connections:



Example:

The 5344S will be placed into CW mode. 15 GHz will be selected on the 5344A.

1. Set MANUAL LOCK and AUTO LOCK off (lamp off). If AUTO LOCK is turned on, the 5344A will display error code Err 10.
2. Set the 5344A rear panel Mode switch to the SUB HMNC position.
3. Set the 5344A Frequency Multiplier to 1. On the 5344A press:



4. Select CW mode on the 8350A. If the plug-in has a CW filter, turn it OFF.
5. Using the 8350A DATA ENTRY keys, press:

The 8350A should display 15.000 GHz.

6. Notice that the counter is not displaying 15 GHz, but the frequency the YTO is at before any multiplication. If you knew the multiplier value, the counter display would be of some use, but let's assume the value is unknown.
7. Using the 5344A Function keys, press and release MODE until the CW annunciator lights. The F1 key will light indicating the 5344A is wating for a CW frequency value.
8. Using the 5344A Numeric Entry keys press:

The 5344A should display:

15.000000000 GHz

Figure 3-17. Subharmonic Locking Mode

9. Press the MANUAL LOCK key.

   The LOCKED annunciator should light.

10. The 5344A will now divide the entered value of 15 GHz by the YTO frequency being displayed on the counter. The resulting value will be rounded to the nearest integer. The 5344A will determine the YTO frequency required to achieve lock. From this, the 5344A will turn on the FREQ HI or FREQ LO annunciator indicating the direction the YTO frequency must be tuned.

11. If the FREQ LO annunciator lights, manually raise the frequency of the 8350A until the 5344A locks.

12. If the FREQ HI annunciator lights, manually lower the frequency of the 8350A until the 5344A locks.

13. Notice that the counter is now displaying the actual output frequency of the plug-in even though it's counting the rear panel AUX OUT. The counter display is multiplied by the Frequency Multiplier value so the true output and the counter's display are the same. When the 5344S is not locked, or either MANUAL or AUTO LOCK are off, the counter will always display the true frequency it's counting. When Lock is achieved, the counter display will be multiplied so it displays the actual front panel output frequency.

NOTE

The 5344S has no way of determining the amount by which the YTO is being multiplied before being sent to the front panel of the plug-in. The 5344S is dependent upon the CW value entered on the 5344A. For example, if the YTO range is 2 to 5 GHz you could enter 20 GHz on the 5344A front panel and then press MANUAL LOCK. If the YTO was tuned close enough to a subharmonic of 20 GHz, lock could be achieved. The counter will display 20 GHz and nothing would appear wrong. But what if the 8350A was set to 10 GHz? The YTO would be at 5 GHz, the 5344S would determine the Frequency Multiplier to be 4×5 GHz = 20 GHz. The YTO would still be at 5 GHz. The 5344A and the counter would display 20 GHz, but the 8350A is really generating 10 GHz. The 5344S cannot detect that the 8350A is really at 10 GHz. The easiest way to avoid this situation is to set the 8350A as close as possible to the true desired output frequency. This way the YTO will require only a minor amount of tuning to achieve lock and the possibility of the 5344A determing the wrong multiplier is reduced. AUTO LOCK would also avoid this since the 5344A programs the 8350A to the desired frequency. A good practice is to compare the 5344A/counter and 8350A display when using MANUAL LOCK. The displays should be the same.

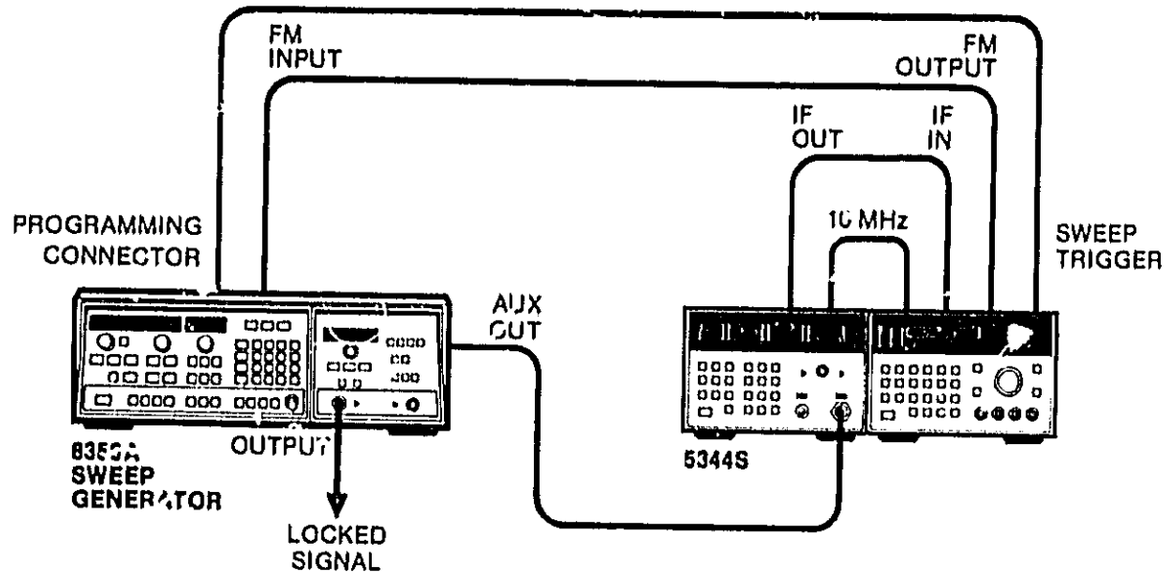
14. If AUTO LOCK had been used, the 5344A would have automatically programmed, the 8350A to 15 GHz.

Figure 3-17. Subharmonic Locking Mode (Continued)

Description:

This procedure will demonstrate Frequency Offset Locking. The actual front panel output frequency will be 10 MHz. The rear panel AUX OUT (YTO) will be used for the locking signal.

Connections:



Example:

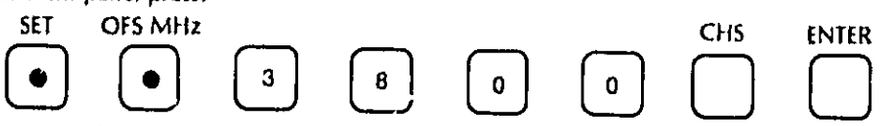
The 5344S will operate in CW mode and 10 MHz will be the locked frequency.

NOTE

Since there is no control over the Cavity Oscillator in the plug-in, the output signal is not phase locked.

1. First determine the frequency of the Cavity Oscillator in the plug-in. For the 83592A it is 3.8 GHz.
2. Now enter the Cavity Oscillator frequenc into the counter as an offset. Since the 5342A and 5343A adds all offsets, the value must be entered as negative.

   On the counter front panel press:

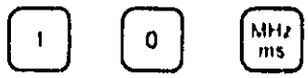
   Now 3.8 GHz will be subtracted from all frequencies applied to the counter.
3. Set the 5344A rear panel Mode switch to the SUB HMNC position.
4. Select CW mode on the 8350A. If the plug-in has a CW filter, turn it OFF.
5. Using the 8350A DATA ENTRY keys press:

   The 8350A should display 10.00 MHz.
6. Notice that the counter is not displaying 10 MHz, but the frequency of the YTO before being mixed with the Cavity Oscillator.
7. Using the 5344A Function keys, press and release MODE until the CW annunciators light. The F1 key will light indicating the 5344A is waiting for a CW frequency value.

Figure 3-18. Frequency Offset Locking

8. Using the 5344A Numeric Entry keys press:



The 5344A should display:

10.000000 MHz

9. Press the MANUAL LOCK key.

The LOCKED annunciator should light.

10. If the FREQ LO annunciator lights, manually raise the frequency of the 8350A until the 5344A locks.

11. If the FREQ HI annunciator lights, manually lower the frequency of the 8350A until the 5344A locks.

12. Notice that the counter is now displaying the actual output frequency of the plug-in although it's counting the rear panel AUX OUT. The counter display is offset by the Cavity Oscillator value so the true output and the counter's display are the same. When the 5344S is not locked, or either MANUAL LOCK or AUTO LOCK are off, the counter will always display the true frequency it is counting. When Lock is achieved, the counter display will be offset so it displays the actual front panel output frequency.

13. Above 2.4 GHz, the 83592A plug-in does not use the Cavity Oscillator, so frequency Offset Locking is limited to the range where the output of the plug-in is generated by mixing it with a fixed frequency oscillator.

14. If AUTO LOCK was being used, the 8350A would have been automatically programmed to 10 MHz.

NOTE

When performing Frequency Offset Locking procedures, if you know the true frequency of the Cavity Oscillator in the plug-in, enter that value. In this procedure, you entered 3.8 GHz as the offset. If the Cavity Oscillator is really at 3.7995xxxx GHz and this value is entered, the true output of the plug-in when Locked will be closer to the selected value. To determine the true frequency of the Cavity Oscillator, apply the locked signal to the input of another counter. If the sweeper is locked at 10 MHz the second counter probably isn't displaying exactly 10 MHz. This error is the amount the Cavity Oscillator is off from the value entered into the 5344S system's counter. As an offset into the second counter, enter the frequency to which the sweeper is locked. In this example, you would enter an offset of -10 MHz. Now the second counter is displaying the amount the Cavity Oscillator is off frequency. If the result is positive, lower the offset frequency by that amount. If the result is negative, increase the offset by that amount.

On the second counter, note the least significant digit that is stable. For example, the 1 KHz position is stable, but the 100 Hz position and below are not. When entering the true offset in the 5344S system's counter, limit the offset to the LSD that is stable.

Figure 3-18. Frequency Offset Locking (Continued)

3-138. REMOTE PROGRAMMING VIA THE HP-IB INTERFACE

3-139. Introduction

3-140. The 5344S Source Synchronizer is compatible with the Hewlett-Packard Interface Bus (HP-IB). Remote programming is installed as standard equipment and allows the 5344S to respond to remote control instructions as described in the following paragraphs. The 5344S also has the capability to act as a system controller for use with HP-IB compatible sweep oscillators, such as the 8350A Sweep Oscillator.

NOTE

HP-IB is Hewlett-Packard's implementation of IEEE Std. 488-1978, "Standard Digital Interface for Programmable Instrumentation".

3-141. The user must be familiar with the selected controller (9825A, 9826A, 9835A, 9845A, or 85A computers), the HP-IB, and the manual operation and functional capabilities of the 5344S.

3-142. HP-IB MODES OF OPERATION

3-143. There are two major modes of 5344S HP-IB operation:

1. Programmable — Where the 5344S is connected to a controller (and possibly other devices) via HP-IB and can be programmed remotely.
2. System Controller — Where the 5344S is connected only to a HP 8350A Sweep Oscillator via HP-IB and acts as a controller (this is called AUTO LOCK).

NOTE

The 5342A or 5343A counter used with the 5344A may also have HP-IB capability (Option 011 installed). In general, the counter's HP-IB interface is independent of the 5344A's, and may be accessed normally to control the counter. The only difference occurs when the 5344A is in Lock mode (MANUAL LOCK or AUTO LOCK button lit), then the counter's HP-IB interface is inactive. Attempting to send codes to, or read from the counter will cause all bus activity to stop.

3-144. When the 5344S is in the Programmable mode, the counter and 5344A would normally be on the same HP-IB bus, controlled by the same remote controller. In System Controller mode (Auto Lock), the 5344A is connected to the sweeper via the HP-IB, and the counter may be connected to a remote controller on a separate bus.

3-145. PROGRAMMABLE MODE

3-146. Interface Functions Subset

3-147. The capability of a device connected to the bus is specified by its interface function subset. These functions provide the means for a device to receive, process, and send messages over the bus. *Table 3-11* lists the 5344S interface functions using the terminology of the IEEE 488-1978 standard. These functions are also listed on the rear panel (adjacent to the HP-IB connector) as follows:

SH1, AH1, T2, L2, SR1, RL1, PP0, DC1, DT1, C0, E1

Table 3-11. HP-IB Interface Functions

Interface Function Subset Identifier	Interface Function Description
SH1	Complete Source Handshake Capability
AH1	Complete Acceptor Handshake Capability
T2	Talker (Basic Talker, Serial Poll, No Talk Only, Doesn't Unaddress If MLA)
L2	Listener (Basic Listener, No Listen Only, Doesn't Unaddress If MLA)
SR1	Complete Service Request Capability
RL1	Complete Remote/Local Capability
PP0	No Parallel Poll Capability
DC1	Complete Device Clear Capability
DT1	Complete Device Trigger Capability
C0	No System Controller Capability
E1	Open Collector Drivers

3-148. Bus Messages

3-149. Through bus messages, devices on the bus can exchange control and measurement information. There are 12 basic messages which can be sent over the interface. *Table 3-12* lists each bus message, giving a condensed description of the 5344S's response, and examples of various controller's implementation of these messages. Paragraph 3-150 provides a more detailed description of these messages.

Table 3-12. HP-IB Messages

HP-IB MESSAGE	DESCRIPTION/RESPONSE	SAMPLE HP 85A Address=20	IEEE 488 USAGE
DATA	Method for sending commands to the 5344A and receiving measurement data.	OUTPUT 720; "CW2GZLK1" ENTER 720;A	
TRIGGER	Used in LOCK/ROLL mode to initiate a sweep. Used in CF/ΔF and START/STOP to initiate a locked sweep.	TRIGGER 7 TRIGGER 720	GET LAG, GET
CLEAR	Aborts any partially entered HP-IB data message.	CLEAR 7 CLEAR 720	DCL LAG, SDC
REMOTE	5344S goes remote. All front panel controls are disabled (except RESET). All functions and modes remain the same as local unless changed by a DATA message.	REMOTE 7 REMOTE 720	REN REN, LAG
LOCAL	Returns 5344A to front panel control.	LOCAL 720	LAG, GTL
LOCAL LOCKOUT	Disables front panel reset key; only controller can return 5344A to local operation.	LOCAL LOCKOUT 7	LLO
GO TO LOCAL AND CLEAR LOCAL LOCKOUT	5344A returns to local operation. Local Lockout is cleared.	LOCAL 7	$\overline{\text{REN}}$

Table 3-12. HP-IB Messages (Continued)

HP-IB MESSAGE	DESCRIPTION/RESPONSE	SAMPLE HP 85A Address=20	IEEE 488 USAGE
SERVICE REQUEST	5344A will request service service when OUT OF LOCK condition exists, or when END OF SWEEP has been detected.	A=STATUS 7 IF BIT (A, 3)=1 Then SRQ is set	
STATUS BYTE	Presents status information.	STATUS 720	LAG, SPE, TAG, (accept status byte), LAG, SPD
PASSS CONTROL	Not applicable.		
ABORT	Terminates all HP-IB activity and returns control to the system controller.	ABORTIO 7	IFC

3-150. 5344S Bus Message Response

a. REMOTE: The 5344A goes Remote when it receives the REMOTE message on the HP-IB. All front panel controls except the RESET key are ignored. In REMOTE operation, the 5344S is programmed by the controller via messages sent over the bus. Until changed, the state of the 5344S remains as it was prior to receipt of the REMOTE message. Any partially entered keyboard sequence is aborted.

b. LOCAL: Returns the 5344S to front panel control. (HP-IB bus activity is ignored until another REMOTE message is sent). Otherwise, the state of the 5344S remains as it was prior to receipt of the LOCAL message, except for LOOP BANDWIDTH which defaults to Wide, and Subharmonic mode which defaults to NORM.

Any partially entered HP-IB data message is aborted.

NOTE

The 5344A does not respond to any messages other than REMOTE and serial polls (see STATUS BYTE) when in LOCAL operation.

c. LOCAL LOCKOUT: Disables the 5344A RESET key. The 5344A remains in remote operation until a LOCAL or CLEAR LOCKOUT & LOCAL message is received on the bus. The LOCAL LOCKOUT message can be used to maintain "absolute" programmatic control of the 5344S.

d. GO TO LOCAL AND CLEAR LOCAL LOCKOUT: Returns the 5344S to front panel control following a LOCAL LOCKOUT message. Otherwise, the state of the 5344S remains as it was prior to receipt of the CLEAR LOCKOUT & message. Any partially entered HP-IB data message is aborted.

e. ABORT: Terminates any HP-IB activity and returns control to the system controller. The 5344A HP-IB interface is reset to the state entered when remote operation is first enabled. 5344S parameters and lock state remain as they were before the ABORT message. Any partially entered HP-IB data message is aborted.

f. **CLEAR:** Aborts any partially entered HP-IB data message.

g. **TRIGGER:** Used in LOCK/ROLL mode to release lock and initiate a sweep, and in CF/ΔF and START/STOP modes to initiate a locked sweep. It is ignored in CW mode. (The HP-IB controller should check the STATUS byte to ensure that lock has been achieved and end-of-sweep is indicated before sending the trigger message). The "TR1" data message must have previously been sent to enable remote trigger operation.

h. **SERVICE REQUEST:** When in remote operation, the 5344S sends the SERVICE REQUEST message to the controller under the following conditions:

1. The 5344S is in Lock mode, but the input signal is not locked, and the OUT OF LOCK bit has been set in the SRQ mask register (see "RM" data message). Note that OUT OF LOCK does not generate the SERVICE REQUEST message in LOCK/ROLL mode during the actual sweep. It is only significant during the locked portion of the LOCK/ROLL sequence).
2. The 5344S is in a sweep mode (CF/ΔF, START/STOP, LOCK/ROLL), the end of the sweep is detected, and the END OF SWEEP bit has been set in the SRQ mask register (see "RM" data message). Note that if the "TR1" data message has not been sent to the 5344S, the SERVICE REQUEST message will be cleared as soon as the next sweep begins.

NOTE

If the 5344S Single Sweep mode is enabled at the time the REMOTE message is received on the bus, the 5344S will act as if it has also received a "TR1" data message. If the "TR1" data message is in effect when the 5344S returns to local operation, the Single Sweep mode will be enabled.

i. **STATUS BYTE:** The controller can read the 5344A STATUS BYTE at any time that the 5344A is in REMOTE operation to check selected operating conditions. This is especially useful in conjunction with the SERVICE REQUEST message. The controller can determine which event caused the service request. The bits of the STATUS BYTE have the following meanings:

7	6	5	4	3	2	1	0
—	RQS	EOS	OOL	FHI	FLO	—	LOK

RQS = 1 —— 5344S is sending a REQUEST SERVICE message.

EOS = 1 —— END OF SWEEP detected.

OOL = 1 —— OUT OF LOCK in LOCK mode.

NOTE

Bit 4 (Out of Lock) does not indicate error messages (see paragraph 3-119). Bit 4 (OOL) is also not valid until a period equal to the Lock time (see *Table 1-1*) after the Lock command (LK1) has been received.

FHI = 1 —— Input frequency too HIGH.

FLO = 1 —— Input frequency too LOW or insufficient signal level at counter input.

LOK = 1 —— 5344S is currently in LOCK mode, but not necessarily Locked (i.e., LK1 has been received).

NOTE

When LOK = 0, RQS = EOS = OOL = FHI = FLO = 0.

j. **STATUS BIT:** NOT USED

k. **PASS CONTROL:** NOT USED

3-151. Address Selection

3-152. To use the 5344S in an HP-IB system, you must set the rear panel ADDRESS switches to the desired address. The topmost switch sets the 5344S to either the ADDRESSABLE or the SYSTEM CONTROLLER mode. For use with a controller, the switch must be set to the ADDRESSABLE position. SYSTEM CONTROLLER is used when the 5344S is controlling an HP-IB programmable sweeper such as the HP 8350A. See System Controller Mode, paragraph 3-177 for more details.

3-153. The five bottom switches, A1 through A5, set the LISTEN/TALK addresses of the 5344S. *Table 3-13* shows all possible address settings of the corresponding ASCII codes for talk and listen. The 5344S is factory set to address 4 as shown in *Figure 3-19*.

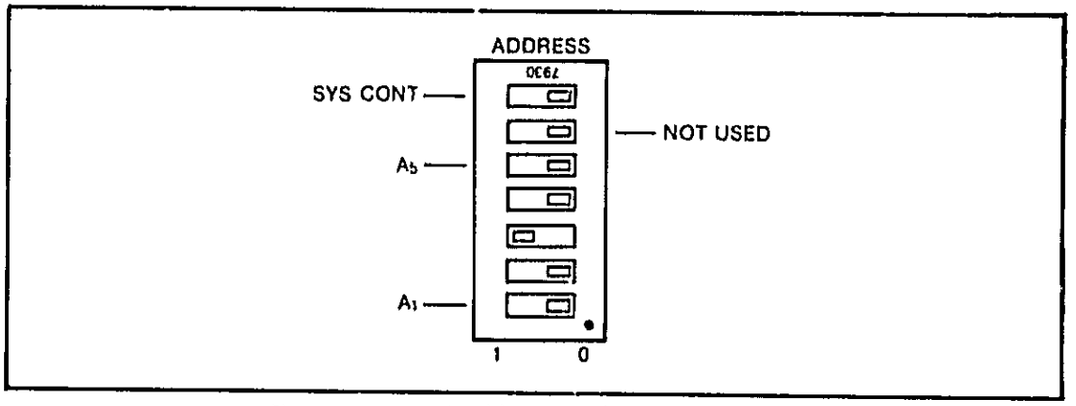


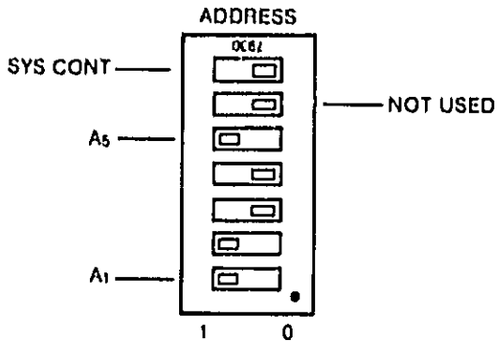
Figure 3-19. 5344S Address Switches Set to Address 4

3-154. Whenever you change the HP-IB address of the 5344A, turn the 5344A OFF, and then ON again.

3-155. Front Panel HP-IB Annunciators

3-156. The four HP-IB annunciators on the front panel indicate the status of the 5344S. The RMT annunciator lights to indicate that the 5344S is under remote control. The LSN annunciator indicates that the 5344S has been addressed to listen (receive commands.) The TALK annunciator indicates that the 5344S is addressed to talk. The CONT annunciator lights to indicate that the 5344S is in the System Controller mode (rear panel switch set to SYS CONT.).

Table 3-13. Address Selection



Address 19 Shown

NOTE

Select the listen address from the table below and set the address switches to the corresponding positions.

ASCII CODE CHARACTER	ADDRESS SWITCHES					5-BIT DECIMAL CODE
LISTEN	A_5	A_4	A_3	A_2	A_1	
SP	0	0	0	0	0	00
!	0	0	0	0	1	01
"	0	0	0	1	0	02
#	0	0	0	1	1	03
$	0	0	1	0	0	04
%	0	0	1	0	1	05
&	0	0	1	1	0	06
'	0	0	1	1	1	07
(	0	1	0	0	0	08
)	0	1	0	0	1	09
*	0	1	0	1	0	10
+	0	1	0	1	1	11
,	0	1	1	0	0	12
-	0	1	1	0	1	13
.	0	1	1	1	0	14
/	0	1	1	1	1	15
0	1	0	0	0	0	16
1	1	0	0	0	1	17
2	1	0	0	1	0	18
3	1	0	0	1	1	19
4	1	0	1	0	0	20
5	1	0	1	0	1	21
6	1	0	1	1	0	22
7	1	0	1	1	1	23
8	1	1	0	0	0	24
9	1	1	0	0	1	25
:	1	1	0	1	0	26
;	1	1	0	1	1	27
<	1	1	1	0	0	28
=	1	1	1	0	1	29
>	1	1	1	1	0	30

Address "21" is preset calculator address and cannot be used.

3-157. COMMAND CODES

3-158. All local functions are programmable via the HP-IB. All functions operate essentially the same as in local. The command codes described in the following paragraphs are listed in a condensed version in *Table 3-15.*

3-159. HP-IB Command Code Syntax Diagrams

3-160. Statement syntax is represented pictorially in the following paragraphs, to explain the format in which HP-IB programming commands should be sent to the instrument. All characters enclosed by a rounded envelope must be entered exactly as shown. Words enclosed by a rectangular box are names of items used in the statement and are described in the text following the diagram. Items contained within circles indicate required literals which must occur in the statement syntax exactly as shown.

NOTE

Spaces are not included in all instances where they may occur. Rather, they are included as (optional) additions to the command string in places where clarity is gained by their use.

3-161. Statement elements, connected by lines, can be followed in only one direction as indicated by the arrowhead at the end of the line. Any combination of statement elements that can be generated by following the lines in the proper direction is syntactically correct.

COMMAND CODES

INSTRUMENT PRESET

IP

Sets the 5344S to its power-up conditions as follows:

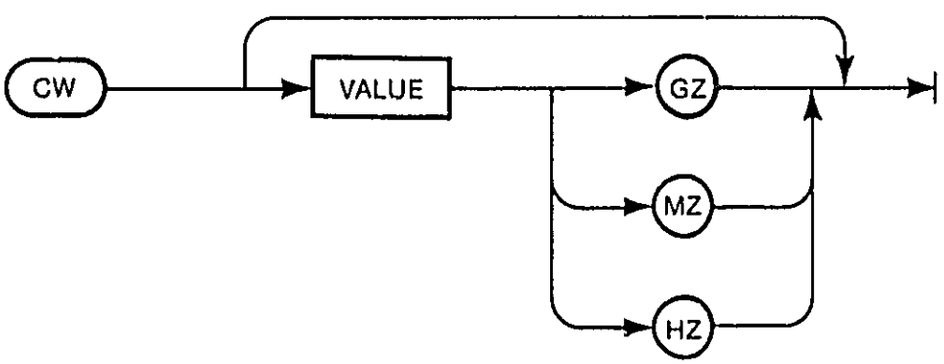
LOCAL
MODE = CW, CW Frequency = 0
MARKERS 1 through 4 = OFF, all Marker Frequencies = 0
SWEEP TIME = 10 ms
STEP SIZE = 0
FREQUENCY MULTIPLIER = 1
RM = 0

The IP command must not be followed by any other commands or data including carriage returns or line feeds until the power-up reset is complete. These commands will be ignored. The IP command should be placed on its own line.

CONTINUOUS WAVE

CW

Sets the 5344S to CW mode. The 5344S enters and displays the CW frequency.



VALUE:

The value may be a simple number such as 10, 25.98, 1010.25, etc. The value may also be a simple number plus an exponent, such as 10.79 E+9, 10 E-1, 26.5 E-2, etc. The exponent plus the multiplier must fall within the 5344S range, such as 75.92 E-1 GZ = 7.592 GHz.

Only the first 11 digits are significant. All others are ignored. Only the first decimal point is accepted as valid.

The CW frequency range is 500 MHz to 18 GHz for the 5342A and 500 MHz to 26.5 GHz for the 5343A. If the 5344S is placed in Subharmonic Locking mode, the limit extends from 10 MHz to 99.999999999 GHz for both counters.

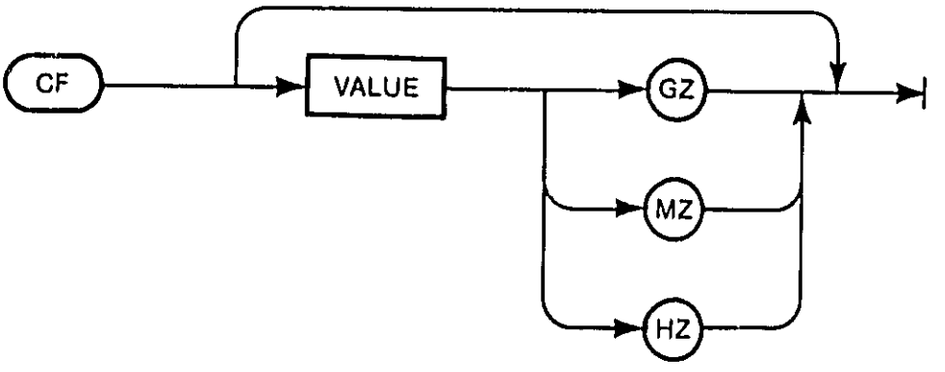
Entries outside of the limits default to the closest limit.

COMMAND CODES (Continued)

CENTER FREQUENCY

CF

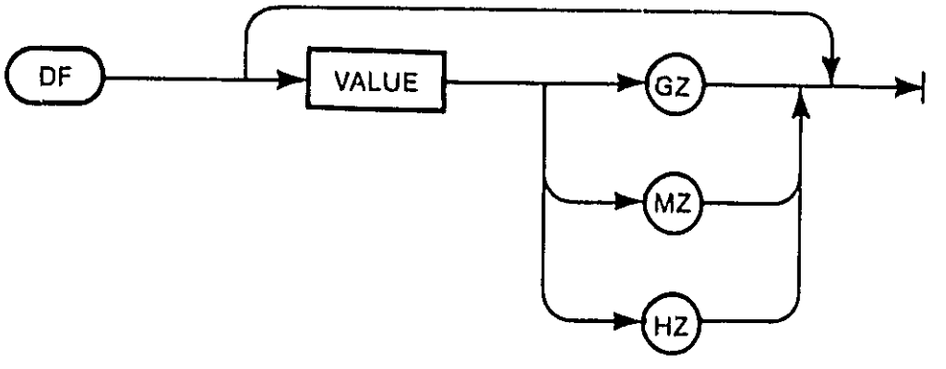
Sets the 5344S to CF/DF mode. The 5344A enters and displays the CF frequency.



DELTA FREQUENCY

DF

Sets the 5344S to CF/ΔF mode. The 5344A enters and displays the ΔF frequency.



VALUE:

The value for CF and DF may be a simple number such as 10, 25.98, 1010.25 etc. The value may also be a simple number plus an exponent, such as 10.79 E+9, 10 E-1, 26.5 E-2, etc. The exponent plus the multiplier must fall within the 5344S range, such as 75.92 E-1 GZ = 7.592 GHz.

The CF frequency range is 500 MHz to 18 GHz for the 5342A and 500 MHz to 26.5 GHz for the 5343A. If the 5344S is placed in Subharmonic Locking mode, the limit extends from 10 MHz to 99.999999999 GHz for both counters.

The DF frequency range is 0 MHz to 40 MHz. If the 5344S is placed in Subharmonic Locking mode, the limits remain 0 MHz to 40 MHz for both counters.

Only the first 11 digits are significant. All others are ignored. Only the first decimal point is accepted as valid.

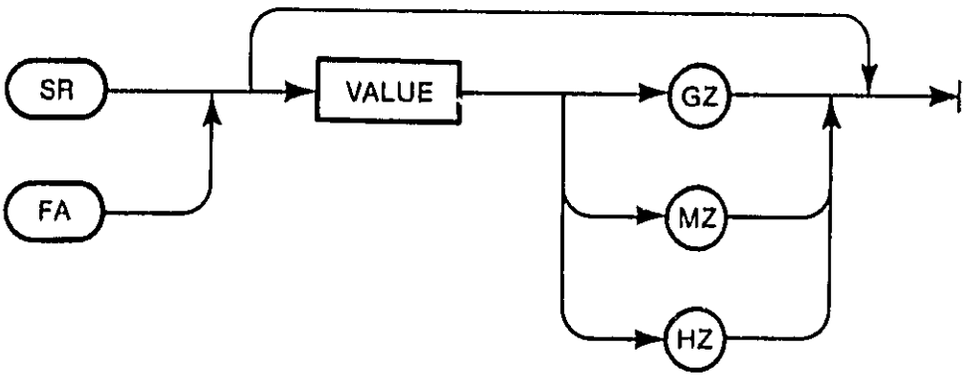
The CF and DF commands may be used together in one single command string or placed on separate lines. The 5344S will enter the CF/DF mode upon receipt of either CF or DF. Either command may be changed without affecting the unspecified commands. Sending any one of the commands without numerical values causes the 5344A to display that parameter. The parameter remains unchanged.

COMMAND CODES (Continued)

START

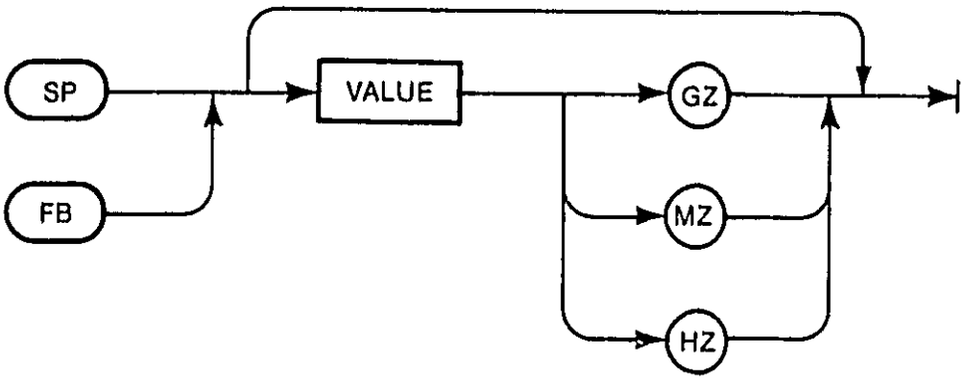
SR (FA)

Sets the 5344S to START/STOP mode. The 5344A enters and displays the START frequency. SR and FA are identical . FA is provided for conversion of 8350A programs.



STOP
SP (FB)

Sets the 5344S START/STOP mode. The 5344S enters and displays the STOP frequency. SP and FB are identical. FB is provided for conversion of 8350A programs.



VALUE:

The value for START and STOP may be a simple number such as 10, 25.98, 1010.25, etc. The value may also be a simple number plus an exponent, such as 10.79 E+9, 10 E-1, 26.5 E-2, etc. An exponent plus a multiplier must fall within the 5344S range, such as 75.92 E-1 GZ = 7.592 GHz.

The START and STOP frequency range is 500 MHz to 18 GHz for the 5342A and 500 MHz to 26.5 GHz for the 5343A. If the 5344S is placed in Subharmonic Locking mode, the limit extends from 10 MHz to 99.999999999 GHz for both counters.

Only the first 11 digits are significant. All others are ignored. Only the first decimal point is accepted as valid.

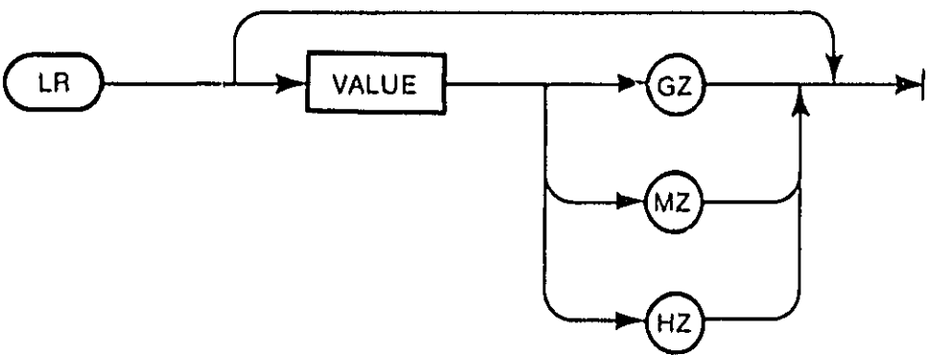
The SR (FA) and SP (FB) commands may be used together in one single command string or placed on separate lines. The 5344S will enter the START/STOP mode upon receipt of either SR (FA) or SP (FB). Either command may be changed without affecting the unspecified commands. Sending any one of the commands without numerical values causes the 5344A to display that parameter. The parameter remains unchanged.

COMMAND CODES (Continued)

LOCK/ROLL

LR

Sets the 53445 to LOCK/ROLL mode. The 5344A enters and displays LK/R START frequency. The STOP frequency and Sweep time are set on the sweep oscillator.



VALUE:

The value for LR may be a simple number such as 10, 25.98, 1010.25, etc. The value may also be a simple number plus an exponent, such as 10.79 E+9, 10 E-1, 26.5 E-2, etc. The exponent plus the multiplier must fall within the 53445 range, such as 75.92 E-1 GZ = 7.592 GHz.

The LR frequency range is 500 MHz to 18 GHz for the 5342A and 500 MHz to 26.5 GHz for the 5343A. If the 53445 is placed in Subharmonic Locking mode, the limit extends from 10 MHz to 99.999999999 GHz for both counters.

Only the first 11 digits are significant. All others are ignored. Only the first decimal point is accepted as valid.

Sending the LR command without a numerical values causes the 5344A to display that parameter. The parameter remains unchanged.

Entries outside of the limits default to the closest limit.

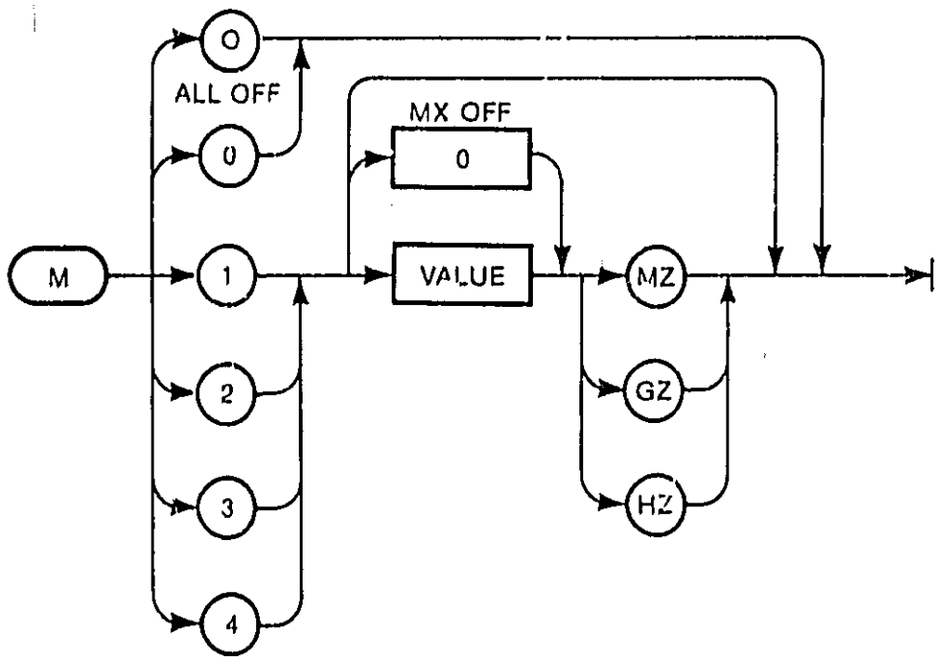
COMMAND CODES (Continued)

MARKERS

M0-M4

M0 or MO	Turns off all markers.
M1	The 5344A enters and displays MARKER 1 frequency.
M2	The 5344A enters and displays MARKER 2 frequency.
M3	The 5344A enters and displays MARKER 3 frequency.
M4	The 5344A enters and displays MARKER 4 frequency.

Setting any marker frequency to 0 turns OFF only that marker.



VALUE:

The value for MARKERS may be a simple number such as 10, 25.98, 1010.25, etc. The value may also be a simple number plus an exponent, such as 10.79 E+9, 10 E-1, 26.5 E-2, etc. An exponent plus a multiplier must fall within the 5344S range, such as 75.92 E-1 GZ = 7.592 GHz.

The MARKER frequency range is 500 MHz to 18 GHz for the 5342A and 500 MHz to 26.5 GHz for the 5343A. If the 5344S is placed in Subharmonic Locking mode, the limit extends from 10 MHz to 99.999999999 GHz for both counters.

Only the first 11 digits are significant. All others are ignored. Only the first decimal point is accepted as valid.

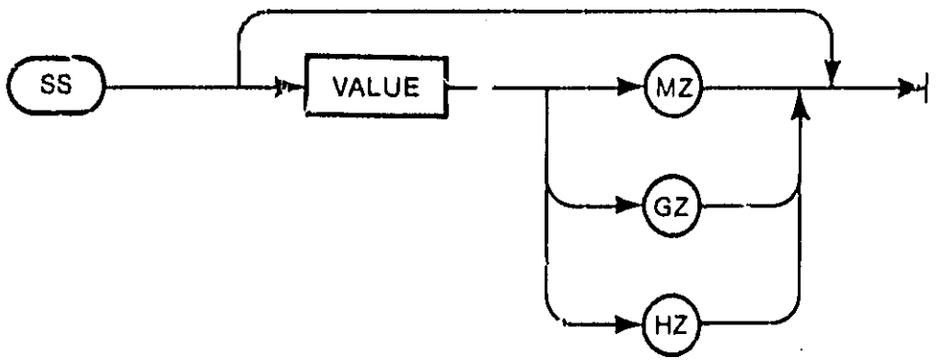
Sending any one of the commands without numerical values causes the 5344A to display that marker frequency. The marker frequency remains unchanged.

COMMAND CODES (Continued)

STEP SIZE

SS

The 5344A enters and displays the STEP SIZE frequency.



VALUE:

The value for SS may be a simple number such as 10, 25.98, 1010.25, etc. The value may also be a simple number plus an exponent, such as 10.79 E+9, 10 E-1, 26.5 E-2, etc. The exponent plus the multiplier must fall within the 5344S range, such as 75.92 E-1 GZ = 7.592 GHz.

The SS frequency range is 500 MHz to 18 GHz for the 5342A and 500 MHz to 26.5 GHz for the 5343A. If the 5344S is placed in Subharmonic Locking mode, the limit extends from 10 MHz to 99.999999999 GHz for both counters.

Only the first 11 digits are significant. All others are ignored. Only the first decimal point is accepted as valid.

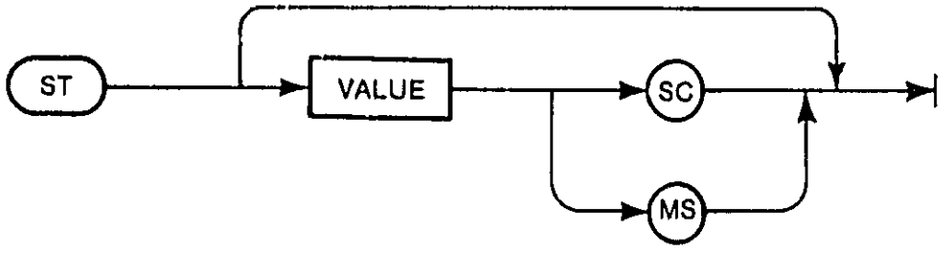
Sending the SS command without a numerical value causes the 5344A to display the current Step Size. The Step Size remains unchanged.

Entries outside of the limits default to the closest limit.

SWEEP TIME

ST

The 5344S enters and displays the Sweep Time.



VALUE:

The value for ST may be a simple number such as 10, 25.9, .101, etc. The value may also be a simple number plus an exponent, such as 9.79 E+1, 10 E-1, 26.5 E-2, etc. A exponent plus a multiplier must fall within the 5344S range, such as 990 E-1 ms = 99 ms.

For any entry, the ultimate value for Sweep Time will contain only one digit after the decimal point. Consecutive digits are not rounded, but instead are dropped.

The Sweep Time range is 10 ms to 100 s.

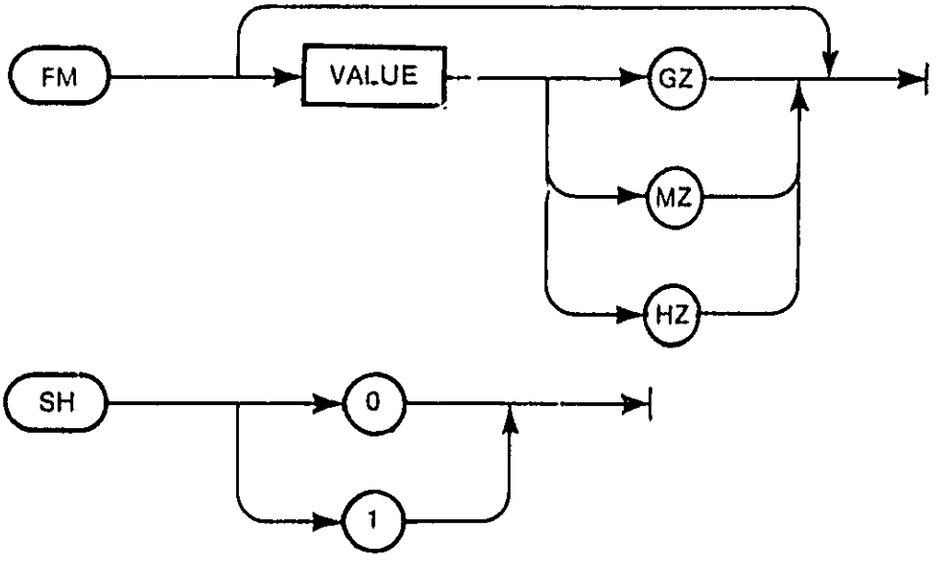
Entries outside of the limits default to the closest limit.

COMMAND CODES (Continued)

FREQUENCY MULTIPLIER

FM

The 5344S enters and displays the Frequency Multiplier.



VALUE:

The Frequency Multiplier can have a value of 1 to 99. If the FM is set to a value of 1, the 5344S can automatically determine the FM if it falls in the range of 1 to 4. An error will be displayed on the 5344A if the FM is determined to be greater than 4. If this occurs, the FM must be manually calculated and entered with the FM command.

Sending the command M9 (Marker 9) will not select FM.

The Subharmonic Mode command (SH1) must be sent to allow the use of Frequency Multipliers.

ACQUIRE

AQ

The AQ command causes the 5344S to enter and display the current frequency being counted by the counter. The 5344S will enter this frequency into the various modes as follows:

a. If CW is selected, the AQ frequency becomes the CW value.
b. If CF/ΔF is selected, only the CF can be acquired.
c. In START/STOP, if:
   1. START (SR or FA) is selected, the AQ frequency becomes the Start value.
   2. STOP (SP or FB) is selected, the AQ frequency becomes the Stop value.
d. If Lock/Roll (LR) is selected, the AQ frequency becomes the Lock/Roll Start value.

UP/DN Increment/Decrement

COMMAND CODES (Continued)

UP

Increments the currently selected frequency parameter by the current Step Size (SS).

DN

Decrements the currently selected frequency parameter by the current Step Size (SS).

The UP and DN commands may only be used to change frequency parameters including the Markers.

The 5344S will ignore any attempt to increment a time parameter such as Sweep Time.

To increment a parameter not currently selected, specify the parameter followed by the UP or DN command, such as:

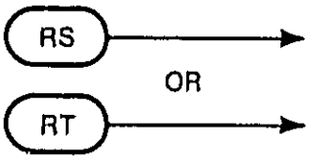
CWUP	CFDN
DFUP	FBDN
FAUP	SPDN
SRUP	LRDN
	M4DN

When incrementing the different parameters, there is a possibility of incrementing beyond the 5344S lock range. If this occurs the 5344A will display Err 01, and if the RM1 command is used a Service Request will be generated. The signal source must be tuned manually or over the HP-IB to within the 5344S lock range.

RESET

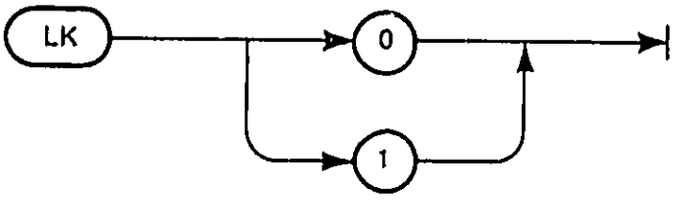
RS (RT)

Restarts the locl ing algorithm. RS will not return the 5344S to local. RT is the same as RS.



MANUAL LOCK

LK 1/0



Sets Manual Lock ON or OFF. The LK command may be part of a command string or placed on a separate line.

Sending the LK 1 command does not guarantee the 5344S will lock. LK1 tells the 5344S to make an attempt to lock. If the signal source is within the lock range, Lock will be achieved. If not, the 5344A will light the FREQ HI or FREQ LO annunciator. The signal source must be tuned manually or over the HP-IB if possible.

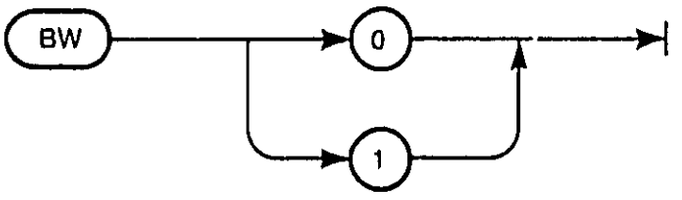
Auto Lock cannot be remotely programmed.

COMMAND CODES (Continued)

BANDWIDTH

BW 1/0

Set the 5344A to Wide or Narrow Bandwidth.



BW1 Sets Wide Bandwidth

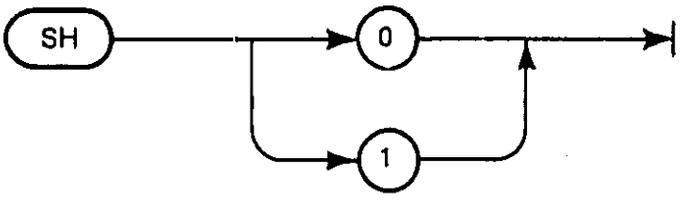
BW0 Sets Narrow Bandwidth

The Manual Lock light will flash when the Bandwidth is set to Narrow in Manual Lock.

SUBHARMONIC LOCKING

SH 1/0

Set the 5344A to Subharmonic Mode.



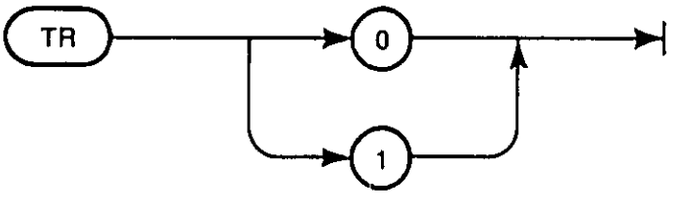
SH1 Sets Subharmonic ON

SH0 Sets Subharmonic OFF

If frequency values beyond 18 GHz (5342A) or 26.5 GHz (5343A) are to be used, the Subharmonic command must be sent before any mode command, such as:

SH1CW20GZ SH1CF30GZ

SWEEP TRIGGER



TR 1/0

Selects either Remote or Internal Sweep Trigger.

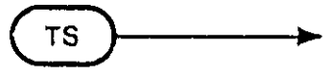
TR1 Selects Remote Trigger. TR1 does not initiate a sweep. The TS command must be used to trigger a sweep. TR1 tells the 5344S to sweep when a TS command is received.

TR0 Selects Internal Sweep Trigger. 5344S will trigger approximately 10 ms after completion of the last sweep.

COMMAND CODES (Continued)

TRIGGER SWEEP

TS



Initiates a Single Sweep. The TR1 message must have been previously sent, or must proceed the TS command in the command string.

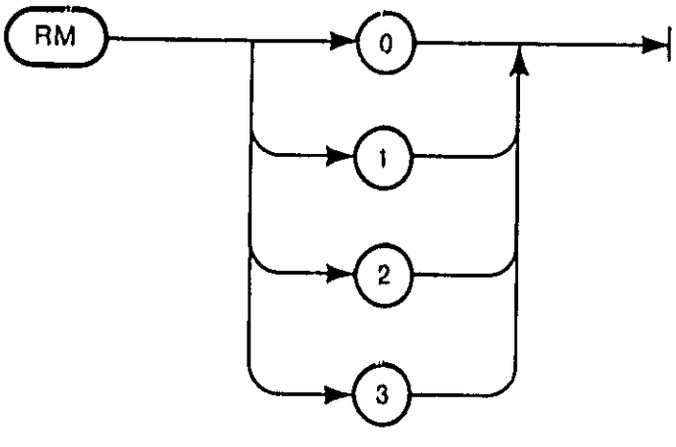
If the 5344S is in CW mode, sending the TS command is essentially the same as sending the Reset (RS) command. The 5344S will restart the locking process.

Group Execute Trigger (GET), such as the TRIGGER command (HP 85-Basic) may also be used to initiate a sweep. Refer to the specific controller's operating manual for more details.

SERVICE REQUEST MASK

RM

Set the 5344A Service Request mask. The RM command determines which of the following conditions will generate a Service Request.



The RM command is followed by a single digit which specifies the set of conditions that is to generate a service request:

0 —— NONE
1 —— OUT OF LOCK
2 —— END OF SWEEP
3 —— OUT OF LOCK or END OF SWEEP

Only one condition may be active at any one time. If more than one is specified, such as RM12, the second value will be ignored. Notice however, that RM3 considers two conditions to generate an SRQ interrupt.

3-162. Input Code Format

3-163. The 5344A will accept command strings in either upper or lower case. Spaces, carriage returns, linefeeds and invalid message sequences are ignored. For example, (in HP 85A-Basic):

OUTPUT 701; "CW2GZLK1" or output 701; "cw2gzlk1"

Either format will produce the same results. Depending on the controller, this can help speed programming.

3-164. Parameter data messages (CW, CF, DF, SR, SP, LR, M1, M2, M3, M4, SS, ST, FM) are usually, but not necessarily followed by a frequency. The parameter data message by itself results in the specified parameter being displayed on the front panel.

3-165. Special Programming Considerations

3-166. Only the first 11 digits of a simple number are significant. Others are ignored. Also, only the first decimal point has any effect.

3-167. Only the first 2 digits of an exponent are significant. Others are ignored.

3-168. The FM parameter may be terminated with any frequency units data message (GZ, MZ, HZ).

3-169. Output Format

3-170. The 5344A does not have the capability to output data. The 5344A can only output status information as described in paragraph 3-150.

3-171. Remote Frequency Offset Locking

3-172. To fully understand Frequency Offset Locking during remote, a few points should be discussed.

3-173. First, the 5344A and the counter cannot be in Remote at the same time. The 5344A needs the counter's circuitry to perform its functions. To avoid any conflict, whenever the 5344A is placed into Remote and Lock is ON, the counter is automatically switched to Local and the front panel controls are locked out.

3-174. In Frequency Offset Locking, the counter must have a frequency offset activated. The counter always adds the offset to the frequency being counted. For Frequency Offset Locking the offset value is entered as negative, such as -3.8 GHz. This can be done over the HP-IB (provided the counter has HP-IB) using the following command string:

SOM-3800EOM1 See the appropriate counter manual for specific details.

3-175. Both the 5342A and 5343A Microwave Counters will retain any offset entered when they return to Local. This is necessary, so when the 5344A is set to Remote, the counter will still have the offset active. This allows the 5344S System to operate completely under remote control.

3-176. To summarize, the following is the basic procedure for remote operation of Frequency Offset Locking.

a. Set both the counter and 5344A to Local.

b. Place the counter into Remote. Send the code string to enter the required frequency offset. For example, if -3.8 GHz must be subtracted, the code string SOM -3800EOM1 would be sent.

c. Place the 5344A into Remote and send the desired commands. When the 5344A goes Remote, the counter will automatically go to Local. The frequency offset will still be active in the counter. Remember to send the SH1 command (activate Subharmonic mode).

3-177. SYSTEM CONTROLLER MODE (AUTO LOCK)

3-178. In the Auto Lock mode, there is no calculator or computer controlling the HP-IB. Instead, the 5344A is placed in the System Controller mode by setting the rear panel ADDRESS switch to the SYS CONT position. The 5344A HP-IB connector is connected directly to the HP-IB connector of the 8350A or 8620C Option 011 Sweep Oscillator. No other powered-up controllers may be connected to the bus.

3-179. The 5344A now has the ability to program the sweep parameters based on data entered on the 5344A keyboard. For instance, 2 GHz is entered into the 5344A keyboard in the CW Mode. When the AUTO LOCK key is pressed, the 5344A will program the sweeper to 2 GHz. Provided the sweeper is properly aligned, the actual output frequency should be within the 5344S lock range. If the actual frequency is not within the lock range, the 5344A will alter the bus code in an attempt to bring the sweeper within lock range. If the 5344A is unsuccessful, Err 11 will be displayed on the 5344A.

3-180. The address of the 5344A and the sweeper must be set to the same value.

3-181. The 5344S cannot be operated in Auto Lock/Roll with an 8620 series sweeper.

3-182. For HP-IB interface capability in System Controller Mode, see *Table 3-14*.

SH1, AH1, T4, L2, SR0, RL0, PP0, DC0, DT0, C1, 2, 3, 4, 27, E1

Table 3-14. HP-IB Interface Functions (System Controller Mode)

Interface Function Subset Indentifier	Interface Function Description
SH1	Complete Source Handshake Capability
AH1	Complete Acceptor Handshake Capability
T4	Talker - (Basic Talker, No Serial Poll, No Talk Only, Doesn't Unaddress If MLA)
L2	Listener - (Basic Listener, No Listen Only, Doesn't Unaddress to Listen If MTA)
SR0	No Service Request Capability
RL0	No Complete Remote/Local Capability
PP0	No Parallel Poll Capability
DC0	No Complete Device Clear Capability
DT0	No Device Trigger Capability
C1	System Controller Capability
C2	Send IFC and Take Charge
C3	Send REN
C4	Responds to SRQ
C27	Send Interface Message, Cannot Receive Control, Cannot Pass Control to Self, No Parallel Poll, Can Take Control Synchronously
E1	Open Collector Outputs

3-183. The 5344S acts as a system controller for an HP 8620C or HP 8350A sweeper. No other system controller may be on the bus. The 5344S HP-IB address switch must be set to the address of the sweeper, and the system controller switch must be in the SYS CONT. position.

NOTE

The operating algorithm in this mode includes a measurement of output frequency with the HP 8620C programmed to its minimum and maximum frequency. The user must ensure that the sweeper output power and cabling to the 5342A/43A counter will deliver a sufficient signal level. For example, the user may wish to lock at 2 GHz using an 86290 plug-in and cables adequate for 2 GHz but not 18 GHz. When the automatic locking algorithm in the 5344S sets the sweeper to 18 GHz for calibration, Err 01 will result.

Table 3-15. Condensed HP-IB Command Code Set

IP	Instrument Preset Set the 5344S to the following conditions: Local Mode = CW, Frequency = 0 All Markers Off Sweep Time = 10 mS Step Size = 0 Frequency Multiplier = 1 RM = 0
CW	Sets 5344S to CW mode. Enters and displays CW frequency.
CF	Sets 5344S to CF/ΔF mode. Enters and displays CF frequency.
DF	Sets 5344S to CF/ΔF mode. Enters and displays ΔF frequency.
SR	Sets 5344S to Start/Stop mode. Enters and displays Start frequency.
FA	Sets 5344S to Start/Stop mode. Enters and displays Start frequency.
SP	Sets 5344S to Start/Stop mode. Enters and displays Stop frequency.
FB	Sets 5344S to Start/Stop mode. Enters and displays Stop frequency.
LR	Sets 5344S to Lock/Roll mode. Enters and displays Start frequency.
M0	Turns all Markers OFF.
MO	Turns all Markers OFF.
M1	Selects Marker 1. Enters and displays Marker 1.
M2	Selects Marker 2. Enters and displays Marker 2.
M3	Selects Marker 3. Enters and displays Marker 3.
M4	Selects Marker 4. Enters and displays Marker 4. Setting Marker N to 0 turns off Marker N.
SS	Selects Step Size. Enters and displays Step Size.
ST	Selects Sweep Time. Enters and displays Sweep Time.
FM 1	5344S automatically determines Frequency Multiplier.
FM N	Enters Frequency Multiplier 1 < N < 99
AQ	5344S acquires current frequency value for current mode.
UP	Increments current frequency mode by current Step Size.
DN	Decrements current frequency mode by current Step Size.
RS	Restarts locking process.
RT	Restarts locking process.

Table 3-15. Condensed HP-IB Command Code Set (Continued)

LK0	Manual Lock is turned OFF.
LK1	Manual Lock is turned ON.
BW0	Bandwidth is set Narrow.
BW1	Bandwidth is set Wide.
SH0	Subharmonic mode is turned OFF.
SH1	Subharmonic mode is turned ON. SH1 must precede frequency values greater than 18 GHz (5342A) or 26.5 GHz (5343A).
TR0	Sets 53445 to internal sweep trigger.
TR1	Sets 53445 to remote sweep trigger.
TS1	Triggers a sweep. TR1 must be active to use TS1.
RM0	53445 will not generate a Service Request.
RM1	53445 generates a Service Request when Out Of Lock. LK1 must be active for RM1 to generate a Service Request.
RM2	53445 generates a Service Request when at End Of Sweep.
RM3	53445 generates a Service Request when Out Of Lock or at End of Sweep. LK1 must be active for RM3 to generate a Service Request when Out Of Lock.

SECTION IV
PERFORMANCE TESTS

4-1. INTRODUCTION

4-2. The procedures in this section provide methods of verifying the operation of the HP 5344S Source Synchronizer. The operation verification tests (paragraphs 4-14 and 4-23) can be performed to give the operator a high degree of confidence that the 5344S is operating properly. The complete performance test consists of all the tests in this section. All tests can be performed without access to the interior of the instrument. The operation verification tests the front panel functions and remote operation.

4-3. EQUIPMENT REQUIRED

4-4. The equipment required for the operation verification and performance test procedure is listed in *Table 1-7*. Any equipment that satisfies the critical specifications given in the table may be substituted for the recommended model numbers.

4-5. TEST RECORD

4-6. Results of the performance test may be tabulated in *Table 4-2, Performance Test Record*, at the end of Section IV. The majority of the tests provide the equipment setup and keystroke instructions for the labeled function mode. The operator is required to verify the proper instrument response. The test record provides a "Pass/Fail" method of tabulating the performance tests for each indicated step within a test procedure.

4-7. PREREQUISITE TEST PROCEDURES

4-8. The 5344A is a component of the 5344S Microwave Source Synchronizer, which must include a 5342A or 5343A Microwave Frequency Counter. Before powering up the 5344A, first perform the operation verification for the 5342A/43A Microwave Frequency Counter used in the system. The microwave frequency counter operation can be verified without applying power to the 5344A. Refer to Section IV of the Operating and Service Manual for the frequency counter, stand alone self-check, and Operation Verification procedures.

4-9. OPERATION VERIFICATION TEST

4-10. The operation verification test is an abbreviated procedure that may be performed to give a high degree of confidence that the 5344S is operating properly without performing the complete performance test. The operation verification is useful for incoming QA, routine maintenance and after instrument repair.

4-11. To perform the operation verification, refer to paragraph 4-14 and perform the Keyboard and Display Annunciator Test. Next, perform the HP-IB Verification, paragraph 4-23.

NOTE

All performance test procedures which follow refer only to the 5344A half of the 5344S system, unless otherwise noted. References will be made to the "5344A" to indicate the right half of the full rack instrument pair, and to the "5342A/43A" to indicate the left half of the system.

4-12. PERFORMANCE TEST PROCEDURES

4-13. The performance test consists of the following procedures:

Paragraph	Procedure
4-14	KEYBOARD AND DISPLAY ANNUNCIATORS TEST
4-15	CW/MANUAL LOCK TEST
4-16	CF/ΔF and START/STOP TEST
4-17	STEP SIZE TEST
4-18	MARKER TEST
4-19	SUBHARMONIC LOCKING TEST
4-20	CAPTURE RANGE TEST
4-21	LK/R (LOCK AND ROLL) TEST
4-22	AUTO LOCK TEST
4-23	HP-IB VERIFICATION

4-14. KEYBOARD AND DISPLAY ANNUNCIATOR TEST

a. Verify that the following instrument interconnections and switch configurations, as shown in *Figure 4-1*, are correct:

1. IF OUT on 5342A/43A rear panel to IF IN on 5344A rear panel.
2. FREQ STD OUT on 5342A/43A rear panel to 10 MHZ IN on 5344A rear panel.
3. AC Power Cord of 5342A/43A and 5344A to AC Mains.
4. 5344A rear panel toggle switches: Mode switch to NORM, and LOOP BANDWIDTH to WB (WIDEBAND).
5. 5342A/43A rear panel slide switches: 10 MHz Timebase to INT, CW/FM mode switch (5342A) to CW, or FAST/MED/SLOW switch (5343A) to FAST.

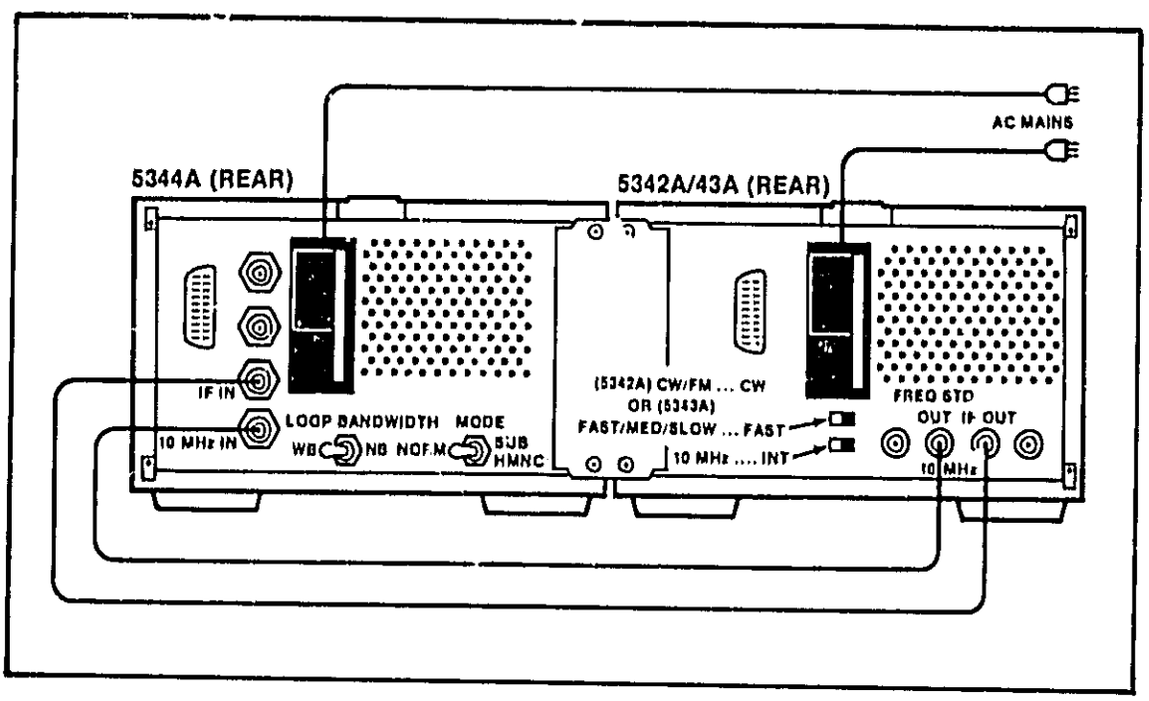


Figure 4-1. System Interconnections

b. Apply power to the 5344S by setting the Line switch on both the 5342A/43A and 5344A to the ON position.

c. With no inputs applied (and input switch set to the higher frequency position), verify that the 5342A/43A display contains "00 000 000 000". The AUTO key annunciator should be lighted and (if the SAMPLE RATE control is not in the HOLD position) the gate light should be flashing. See *Figure 4-2*.

d. Verify the following:

- The 5344A display contains "0.000000".
- The MHz annunciator is lighted.
- The CW annunciator is lighted.
- The F1 annunciator is lighted.
- The 10 Segment meter has two center segments dimly lighted.

e. Press the 5344A MODE key several times. Verify that each successive key press lights the mode annunciators in a scrolling fashion as follows:

Action	Mode
Initially	CW
1st press	CF/ΔF
2nd press	STRT/STOP
3rd press	LK/R
4th press	CW

f. With the MODE key, scroll the 5344A to the LK/R mode. Press the F2 key. Verify that the F2 key indicator flashes and the display contains "ddddddddddd".

This display indicates that the 5344A diagnostic mode has been entered. To exit the diagnostic mode, turn the 5342A/43A LINE switch from ON to STBY, then back to ON.

g. While in the diagnostic mode, press the numeric "1" key, followed by the reset key to enter the "d1" diagnostic. This places the 5344S in the keyboard test diagnostic, "d1". Do not follow the "1" entry with a numeric key. Pressing "1", followed by a "5", for instance, will place the 5344S in the "d15" diagnostic. Verify that the display contains "d 1".

h. *Table 4-1* lists the front panel keys, and the corresponding diagnostic display codes. Press each of the keys listed in the table (in any order) and verify that the proper display code is displayed.

NOTE

The display will contain "d 1" on the right side throughout the test. The diagnostic display code will appear on the left side of the display, only momentarily, while the selected key is pressed.

i. Switch the LINE switch on the 5342A/43A from ON to STBY, then back to ON. This resets both the 5342A/43A and the 5344A. The displays should appear as in steps c. and d.

j. Locate the large round RPG (Rotary Pulse Generator) control on the right half of the 5344A. Turn the RPG knob clockwise. Verify that the display changes from "0.000000 MHz" to "500.000000 MHz" and the second digit position to the right of the decimal point increments as the control is rotated.

k. Turn the RPG counterclockwise. Verify that the second digit position to the right of the decimal point decrements until "500.000000 MHz" is reached. The display should decrement no lower in this mode.

Table 4-1. Keyboard Diagnostic

Front Panel Key	Diagnostic Code Display
MODE	dd
F1	F1
F2	F2
SWP TIME	St
MKR FREQ	FF
STEP SIZE	SS
0	00
1	01
2	02
3	03
4	04
5	05
6	06
7	07
8	08
9	09
.	..
ACQUIRE	AC
GHz	gh
MHz/ms	HH
down arrow	dn
*up arrow	branches to Lamp Test Diagnostic (down arrow returns to keyboard diagnostic)
FINE/COARSE	FC
RESET	rt
MANUAL LOCK	LL
AUTO LOCK	AL

*Pressing the "up arrow", while in the Keyboard diagnostic automatically branches to the Lamp test diagnostic. The Lamp test diagnostic lights all front panel LEDs and annunciators, as shown in *Figure 4-2*. Pressing the "down arrow" will return the 5344A to the Keyboard diagnostic.

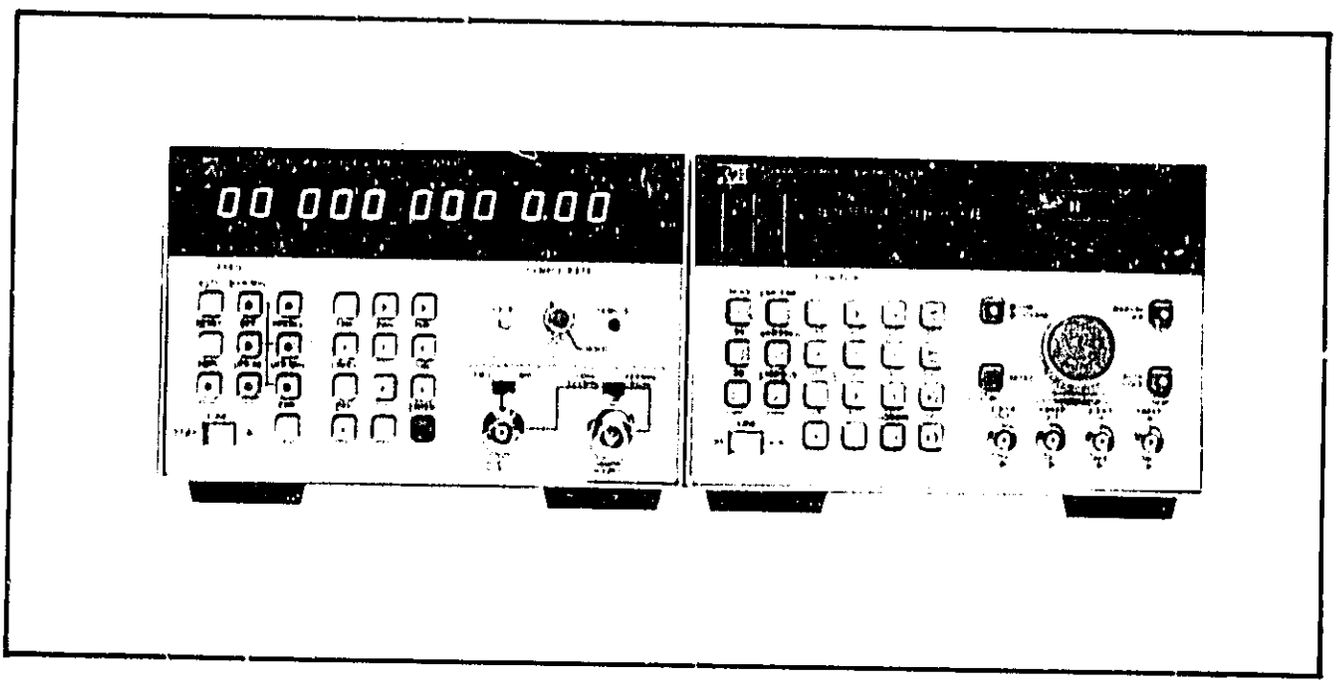


Figure 4-2. Lamp Test Diagnostic

l. Press the FINE/COARSE key. Verify that the LED key indicator lights, indicating the RPG is in the Fine adjustment mode.

m. Turn the RPG clockwise. Verify that the display increments in one Hertz increments (the rightmost digit in the display).

n. Turn the RPG counterclockwise. Verify that the display decrements in one hertz increments, until "500.000 000 MHz". The display should decrement no lower in this mode.

o. Place the NORM/SUB HRMNC switch on the rear panel to the SUB HRMNC (Sub Harmonic) position. Verify the rightmost decimal point in the display lights. Return the rear panel switch to the NORM pos 'ion. Verify that the rightmost decimal point turns off.

p. Record the results on the Performance Test Record, *Table 4-2*

NOTE

The remainder of the performance test utilizes an 8350A Sweep Oscillator mainframe. The examples are shown using the 83525A RF PLUG-IN. However, any compatible plug-in (listed in *Table 3-8*) may be used. The AUTOLOCK feature of the 5344A cannot be completely verified without an 8350A Sweep Oscillator Mainframe.

NOTE

Although the operating frequency range for the 5344S is 500 MHz to 18.0 GHz (26.5 GHz for the 5343A counter option), the performance test is performed only in the range of frequencies that the user has sweeper plug-ins to accommodate.

4-15. CW MODE/MANUAL LOCK TEST

a. Connect the equipment as shown in *Figure 4-3*.

NOTE

For the following tests a Spectrum Analyzer is not necessary but helpful to observe the results.

b. Set LINE switch on the 5342A/43A from ON to STBY, then back to ON.

c. Set the 8350A LINE switch from OFF to ON. Press the INSTR PRESET key.

d. Set the 8350A to CW, at a frequency within the plug-in range, (example: 2.0 GHz). Set the 83525A Plug-In CW FILTER to OFF, RF to ON, and adjust the power for −0.0 dBm.

e. Verify that the 5342A/43A is performing a valid frequency measurement and that the 5344A is in the CW mode.

f. Press the ACQUIRE key on the 5344A front panel and verify that the 5344A display contains a number very close to the 5342A/43A display number.

g. Press the 5344A MANUAL LOCK key. Verify that the LOCKED annunciator lights after a short pause.

h. Verify that the value in the 5342A/43A display and the 5344A are the same (±1 Hz).

i. Press the MANUAL LOCK key to the off position (key indicator light goes off).

j. Set the 8350A to the lower limit of the plug-in's frequency range and repeat steps d through h.

k. Press the MANUAL LOCK key to the off position.

l. Set the 8350A to the upper limit of the plug-in's frequency range and repeat steps d through h.

m. Record the results on the Performance Test Record, *Table 4-2*.

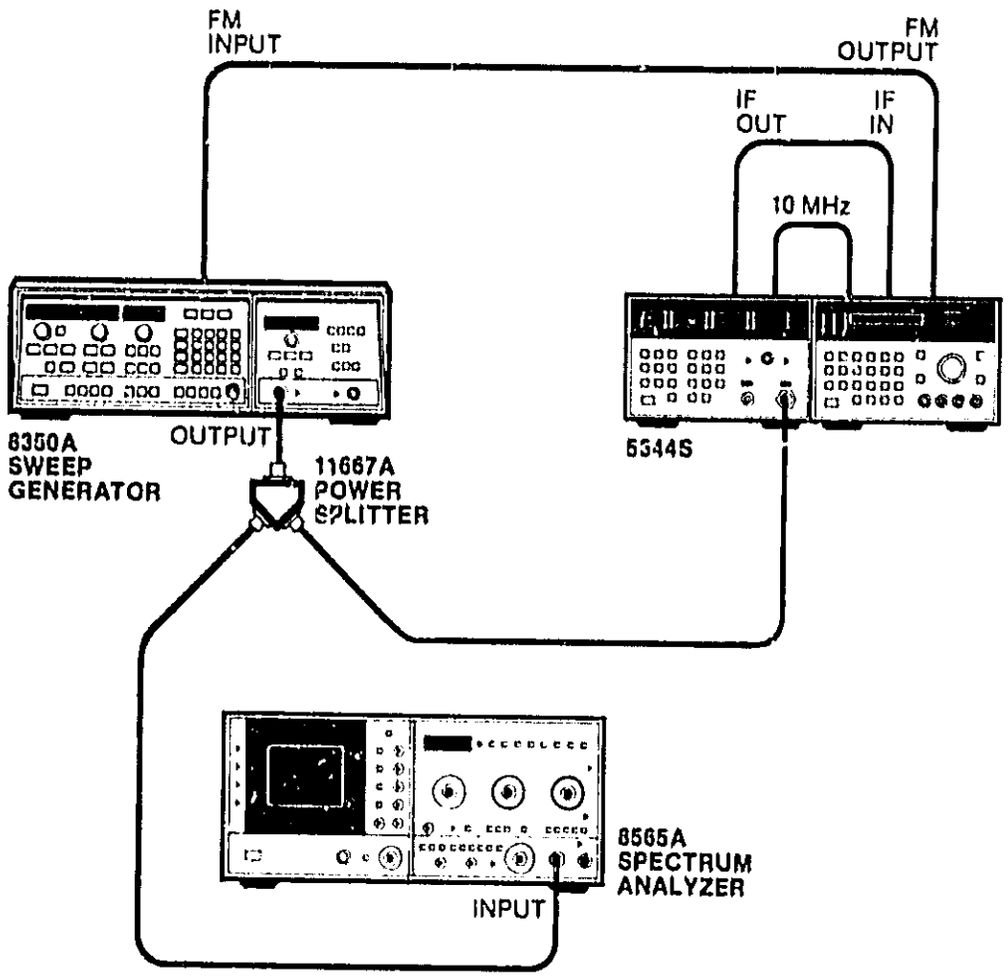


Figure 4-3. Performance Test Setup

4-16. CF/ΔF and START/STOP TEST

a. Connect the equipment as shown in *Figure 4-3*.

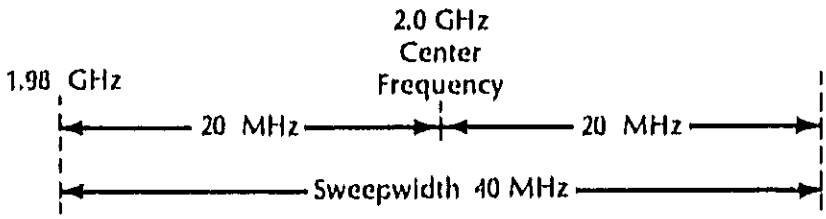
NOTE

For the following tests a Spectrum Analyzer is not necessary bu' is helpful to observ. the results.

b. Set the LINE switch on the 5342A/43A from ON to STBY, then back to ON.

c. Set the 8350A LINE switch from OFF to ON. Press the INSTR PRESET key.

d. Set the 8350A to CW, at a frequency within the plug-in range (example: 2.0 GHz). When choosing the CW frequency, be sure to allow 20 MHz on both sides, for the sweep (see below). Set the 83525A Plug-In CW FILTER to OFF, RF to ON, and adjust the power for ~0.0 dBm.



e. With the MODE key, scroll the 5344A to the CF/ΔF mode.

f. Press the ACQUIRE key on the 5344A front panel and verify that the 5344A display contains a number very close to the 5342A/43A display number. The acquired frequency should be the F1 center frequency.

g. Set the ΔF (sweepwidth) on the 5344A to 40 MHz, by pressing:

h. Press the 5344A MANUAL LOCK key.

i. Verify that the LOCKED annunciator lights, the 10-segment meter has several segments lighted, and the 8350A output is sweeping as described in step d.

j. Press the SWP TIME key. Verify that the 5344A displays the default sweep time value of "10.0 ms".

k. Change the sweep time from 10.0 ms to one second, by pressing:

l. Verify the sweep by observing the 5344A meter (sweeping back and forth), and the 8565A Spectrum Analyzer. The sweep output should be 40 MHz wide, centered on the programmed CF at a 1 second rate.

m. Press the 5344A MODE key once, to change from CF/ΔF to STRT/STOP mode.

n. Verify that the sweep is still active. Review the START frequency displayed (F1), and the STOP frequency (press F2). Verify that the START frequency equals CF (previously entered) -1/2ΔF (previously entered), and the STOP frequency equals CF (previously entered) +1/2ΔF (previously entered). For example:

If CF (entered) = 2 GHz and ΔF (entered) = 40 MHz, then the START should be 1.980 GHz and STOP should be 2.020 GHz.

CF (entered) ..... 2 GHz
ΔF (entered) ..... 40 MHz
START ..... 1.980 GHz [2 GHz - 1/2(40 MHz)]
STOP ..... 2.020 GHz [2 GHz + 1/2(40 MHz)]

o. Press the MANUAL LOCK key to the off position (key indicator light goes off).

p. Set the 8350A to the lower limit of the plug-in's frequency range, plus 20 MHz. Repeat steps e through n.

q. Press the MANUAL LOCK key to the off position.

r. Set the 8350A to the upper limit of the plug-in's frequency range, minus 20 MHz. Repeat steps e through n.

s. Record the results on the Performance Test Record, *Table 4-2*.

4-17. STEP SIZE TEST

a. Connect the equipment as shown in *Figure 4-3*.

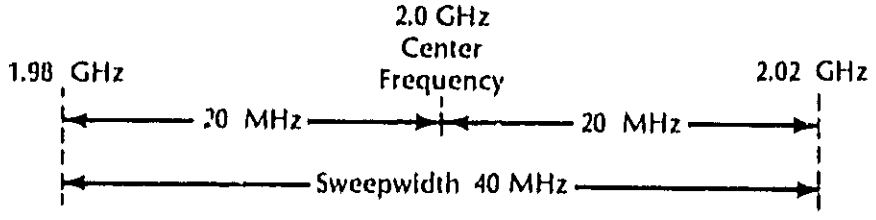
NOTE

For the following tests a Spectrum Analyzer is not necessary but is helpful to observe the results.

b. Set the LINE switch on the 5342A/43A from ON to STBY, then back to ON.

c. Set the 8350A LINE switch from OFF to ON. Press the INSTR PRESET key.

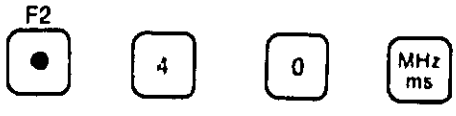
d. Set the 8350A to CW, at a frequency within the plug-in range (example: 2.0 GHz). When choosing the CW frequency, be sure to allow 20 MHz on both sides for the sweep (see below). Set the 83525A Plug-In CW FILTER to OFF, RF to ON, and adjust the power for ~0.0 dBm.



e. With the MODE key, scroll the 5344A to the CF/ΔF mode.

f. Press the ACQUIRE key on the 5344A front panel and verify that the 5344A display contains a number very close to the 5342A/43A display. The acquired frequency should be the F1 center frequency.

g. Set the ΔF (sweepwidth) on the 5344A to 40 MHz, by pressing:



h. Press the 5344A MANUAL LOCK key.

i. Verify that the LOCKED annunciator lights, the 10-segment meter has several segments lighted, and the 8350A output is sweeping as described in step d.

j. Press the 5344A STEP SIZE key. Verify that the 5344A displays "0.000000 MHz".

k. Enter a Step Size value of 1 MHz by pressing:

l. Recall the ΔF value by pressing F2 . Verify that the 5344A displays "40.000000 MHz".

m. Press the  key three times. Verify that the 5344A displays and the sweep output responds as follows.

	Display	Sweep Output
	40.000000	LOCKED
1st press	39.000000	LOCKED
2nd press	38.000000	LOCKED
3rd press	37.000000	LOCKED

n. Press the  key three times. Verify that the 5344A display and the sweep output responds as follows:

	Display	Sweep Output
	37.000000	LOCKED
1st press	38.000000	LOCKED
2nd press	39.000000	LOCKED
3rd press	40.000000	LOCKED

Verify that the 5344A will not step over 40 MHz with a 4th press.

o. Record the results on the Performance Test Record, *Table 4-2*.

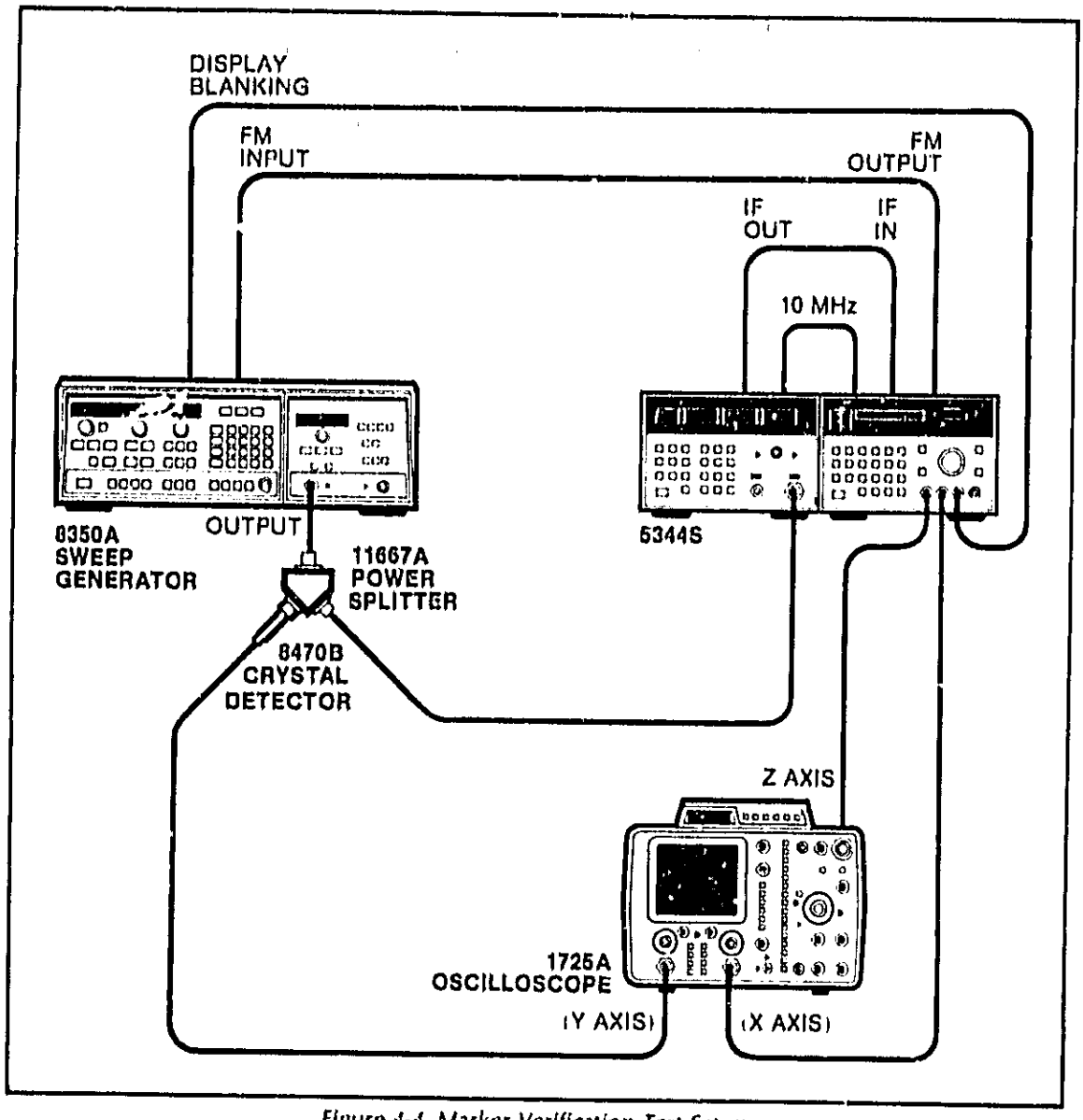


Figure 4-4. Marker Verification Test Setup

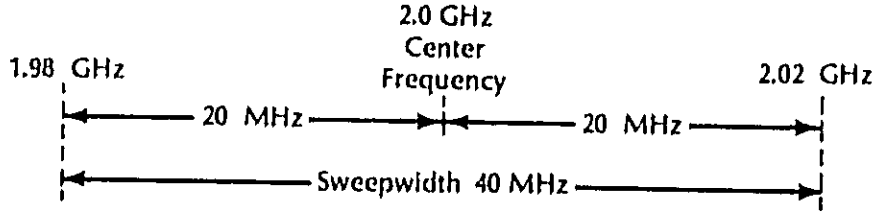
4-18. MARKER TEST

a. Connect the equipment as shown in *Figure 4-4*.

b. Set the LINE switch on the 5342A/43A from ON to STBY, then back to ON.

c. Set the 8350A LINE switch from OFF to ON. Press the INSTR PRESET key.

d. Set the 8350A to CW, at a frequency within the plug-in range (example: 2.0 GHz). When choosing the CW frequency, be sure to allow 20 MHz on both sides for the sweep (see below). Set the 83525A Plug-In CW FILTER to OFF, RF to ON, and adjust the power for ~0.0 dBm.



e. With the MODE key, scroll the 5344A to the CF/ΔF mode.

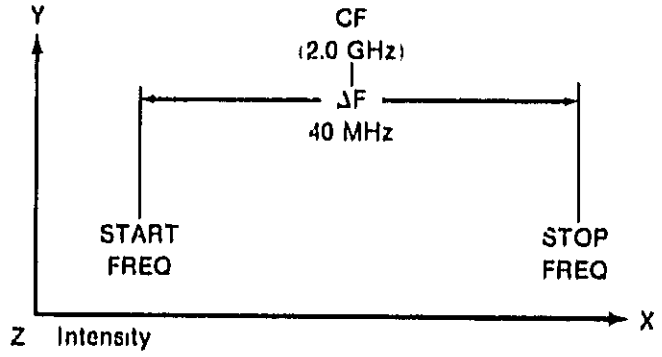
f. Press the ACQUIRE key on the 5344A front panel and verify that the 5344A display contains a number very close to the 5342A/43A display. The acquired frequency should be the F1 center frequency.

g. Set the ΔF (sweepwidth) on the 5344A to 40 MHz, by pressing:

h. Press the 5344A MANUAL LOCK key.

i. Verify that the LOCKED annunciator lights, the 10-segment meter has several segments lighted, and the 8350A output is sweeping as described in step d.

j. Adjust the oscilloscope to produce a stable display as shown below:

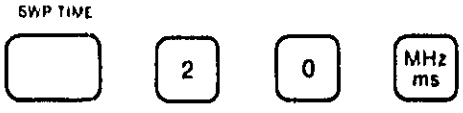


CHAN A ..... DC
CHAN B ..... AC

CHAN A ..... .01 v/cm
CHAN B ..... 1 v/cm
Function ..... X/Y

- (y) Vertical generated by output of crystal detector (dc coupled) to CHAN A.
- (x) Horizontal generated by SWEEP OUT to CHAN B.
- (z) Blanking generated by Z-OUT to Z-AXIS.

k. Change the sweep time to 20 ms by pressing:



l. Up to four markers may be set, by pressing the "MKR FREQ" key followed by a numeric identifier: "1, 2, 3, or 4". Recall the first marker value by pressing the "MKR FREQ" key (key indicator flashes to prompt for numeric entry), followed by the numeric "1" key. Verify that the 5344A display contains "0.000000".

Note

Calling "MARKER 0" will reset all marker values to 0.

m. Enter a frequency for marker 1, between the Start and Stop values, by pressing the desired numeric keys followed by a terminator key (MHz or GHz). For example:

SWEEP
Start = 1.98 GHz (Press F1 to review value)
Stop = 2.02 GHz (Press F2 to review value)

Press: [MKR FREQ] [1] to call marker 1, then

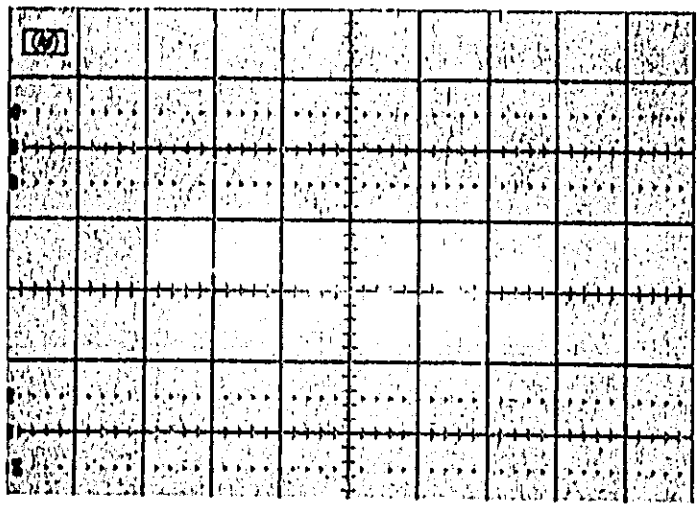
Press: [1] [.] [9] [8] [5] to set a marker at 1.985 GHz.

Repeat the sequence, entering markers 2, 3, and 4 as follows:

Marker 2 ..... 1.995 GHz
Marker 3 ..... 2.005 GHz
Marker 4 ..... 2.015 GHz

If an Err 02 is displayed, refer to the restrictions on markers described in paragraph 3-43. Correct the error and repeat the test.

n. Verify that a bright point appears on the oscilloscope display at each of the designated marker frequency(s), as shown below.



CHAN A ..... DC
CHAN B ..... AC

CHAN A ..... .01 v/cm
CHAN B ..... 1 v/cm
Function ..... X/Y

- (y) Vertical generated by output of crystal detector (dc coupled) to CHAN A.
- (x) Horizontal generated by SWEEP OUT to CHAN B.
- (z) Blanking generated by Z-OUT to Z-AXIS.

o. Press the MANUAL LOCK key to the off position (key indicator light goes off).

p. Set the 8350A to the lower limit of the plug-in's frequency range, plus 20 MHz. Repeat steps f, h, i, j, m and n. Use corresponding marker frequencies for step m.

q. Press the MANUAL LOCK key to the off position.

r. Set the 8350A to the upper limit of the plug-in's frequency range, minus 20 MHz. Repeat steps f, h, i, j, m, and n. Use corresponding marker frequencies for step m.

s. Record the results on the Performance Test Record, *Table 4-2*.

4-19. SUBHARMONIC LOCKING TEST

a. Connect the equipment as shown in *Figure 4-3*.

b. Set the LINE switch on the 5342A/43A from ON to STBY, then back to ON.

c. Set the 8350A LINE switch from OFF to ON. Press the INSTR PRESET key.

d. Set the 8350A to CW, at a frequency within the plug-in range (example: 2.0 GHz). Set the 83525A Plug-In CW FILTER to OFF, RF to ON, and adjust the power for ~ 0.0 dBm.

e. Place the MODE (NORM/SUB HMNC) toggle switch on the 5344A rear panel to the SUB HMNC (Sub Harmonic; position. Verify the rightmost decimal point in the display lights.

f. Press [0] [MKR FREQ •] [9]

This enables the subharmonic multiplier register. Verify that the right side of the display contains "1" initially (or the previously entered value).

g. Press [2] [GHz 5] .This enables a multiplier of "2". Verify that the display now contains: 2.

h. Verify that the 5342A/43A counter displays a frequency reading.

i. Enter a CW frequency into the 5344A, equal to the value of the 5342A/43A counter reading times the multiplier, by pressing [FI •] , then the desired frequency.

j. Press the 5344A MANUAL LOCK key.

k. Verify that the LOCKED annunciator lights and the 5342A/43A display is the same (±2 Hz) as the 5344A display. For example:

   1. The 5342A/43A counter display is "2 GHz".
   2. Set the 5344A to CW, at a frequency of "4 GHz".
   3. After pressing MANUAL LOCK, the 5342A/43A should change to "4 GHz" and the 5344A LOCKED annunciator should light.

l. Return the 5344A rear panel MODE toggle switch to the NORM position. Verify that the rightmost decimal point in the display goes out, and the 5342A/43A displays the source frequency (~2 GHz).

m. Press the MANUAL LOCK key to the off position (key indicator light goes off).

n. Repeat steps e through m using a frequency multiplier of 4 in step g. Note that the frequency reading in step k will change to 8 GHz.

o. Press the MANUAL LOCK key to the off position.

p. Repeat steps e through m using a frequency multiplier of 10 in step g. Note that the frequency reading in step k will change to 20 GHz.

q. Record the results on the Performance Test Record, *Table 4-2*.

4-20. CAPTURE RANGE TEST

a. Connect the equipment as shown in *Figure 4-3.*

b. Set the LINE switch on the 5342A/43A from ON to STBY, then back to ON.

c. Set the 8350A LINE switch from OFF to ON. Press the INSTR PRESET key.

d. Set the 8350A to CW at a frequency within the plug-in range (example 2.050 GHz). Set the 83525A RF Plug-In CW FILTER to OFF, RF to ON, and adjust the power for ~ 0.0 dBm.

e. On the 5344A, press [2] [GHz]

f. Press the MANUAL LOCK key and verify that the FREQ HI annunciator lights.

g. Tune the 8350A closer to 2 GHz. Verify that the LOCKED annunciator lights before or at 2.025 GHz as displayed by the 8350A.

h. Press the MANUAL LOCK key to the off position (key indicator light goes off).

i. Repeat step d using a frequency such as 1.950 GHz. Repeat steps f and g.

j. Record the results on the Performance Test Record, *Table 4-2.*

4-21. LK/R (LOCK AND ROLL) TEST

a. Connect the equipment as shown in *Figure 4-5.*

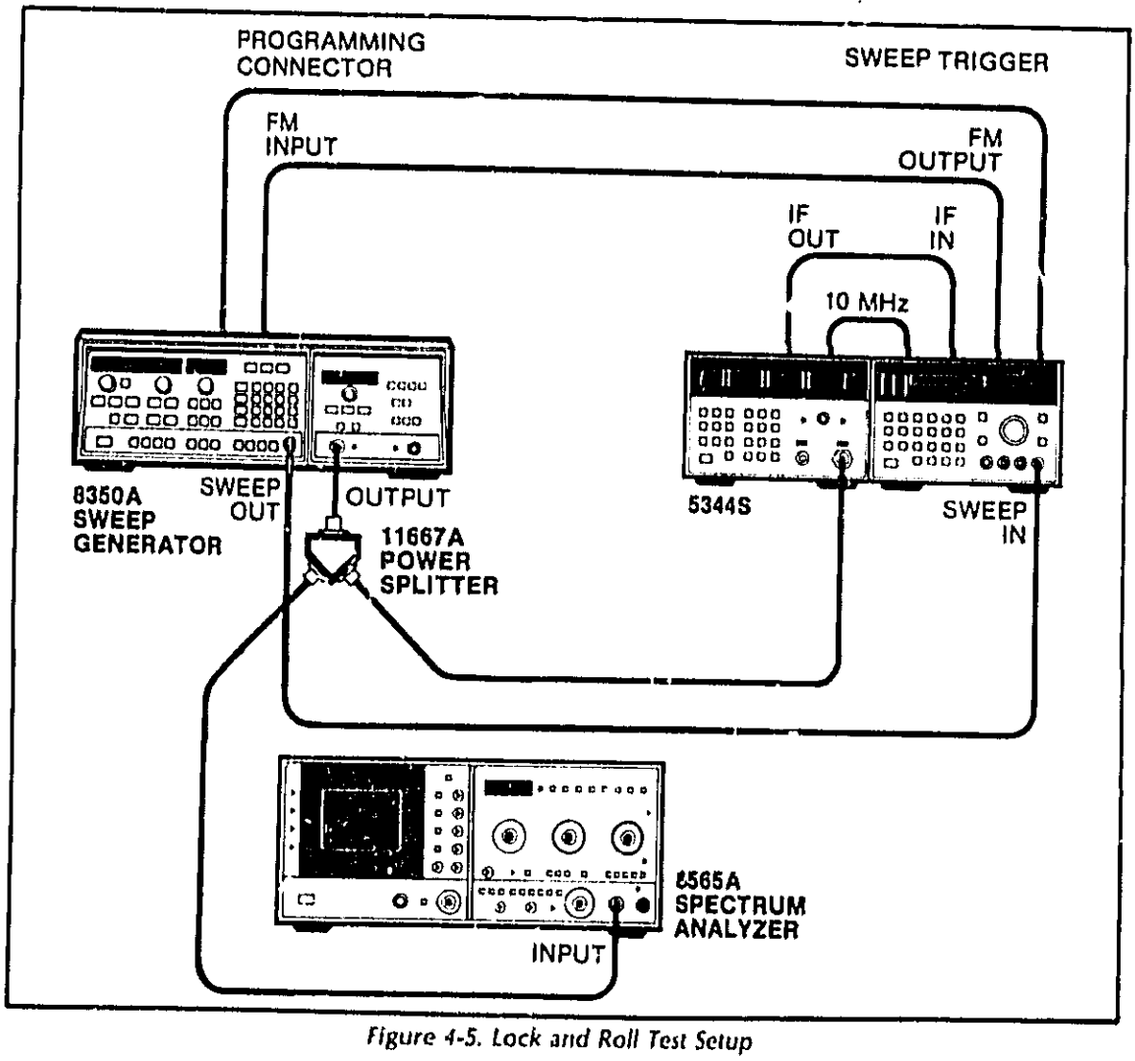


Figure 4-5. Lock and Roll Test Setup

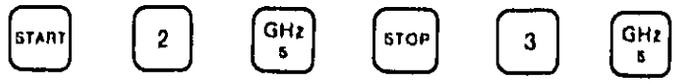
NOTE

For the following tests a Spectrum Analyzer is not necessary but helpful to observe the results.

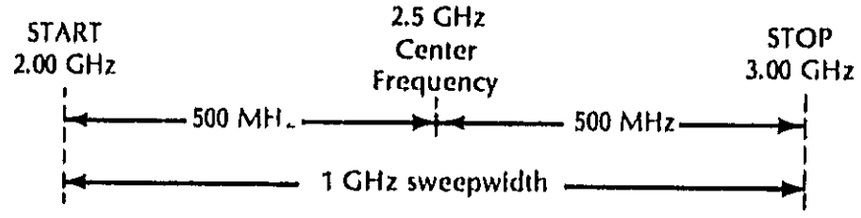
b. Set the LINE switch on the 5342A/43A from ON to STBY, then back to ON.

c. Set the 8350A LINE switch from OFF to ON. Press the INSTR PRESET key.

d. Set the 8350A for a wide sweep, > 40 MHz within the plug-in range. For example, to set a 1 GHz sweep between 2.0 and 3.0 GHz, press:



Set the 83525A Plug-In CW FILTER to OFF, RF to ON, and adjust the power for ~ 0.0 dBm.



e. Using the 5344A MODE key, scroll the 5344A function to the LK/R mode.

f. Set the SWEEP TRIGGER mode on the 8350A to EXT.

g. Enter the F1 START frequency into the 5344A, by pressing:

h. Press the 5344A MANUAL LOCK key.

i. Verify that the LOCKED annunciator lights. If the LOCKED annunciator does not light, and a FREQ HI or FREQ LO annunciator lights, manually retune the starting frequency of the sweep oscillator in a corrective direction, until a LOCKED indication is achieved.

NOTE

If an "- - - - EOS - - - -" display appears, the 5344A has internally timed out, without receiving an End of Sweep message from the sweeper. This is a potential error condition, which may be caused by one of the following:

1. The Sweep Time configured on the sweeper is too long; change the sweeper to a shorter Sweep Time.
2. The 5344A is setup incorrectly for the LK/R mode. Refer to *Figure 3-11*, then repeat the procedure.
3. The sweeper is setup incorrectly for an externally triggered sweep. Consult the operation section of the sweeper manual.

j. Press the MANUAL LOCK key to the off position (key indicator light goes off).

k. Repeat steps d using the plug-in's lower limit as the START frequency and the upper limit as the STOP frequency. Repeat steps f through i.

l. Record the results on the Performance Test Record, *Table 4-2*.

4-22. AUTO LOCK TEST

NOTE

This test requires an HP 8350A programmable Sweep Oscillator and the 8350A BNC to Programming Connector cable.

a. Set up the equipment as shown in *Figure 4-6*.

b. Set the 5344A rear panel HP-IB switch to "SYS. CONT" (system controller). Set the LINE switch on the 5342A/43A from ON to STBY, then back to ON. Verify that the front panel "CONT" annunciator lights.

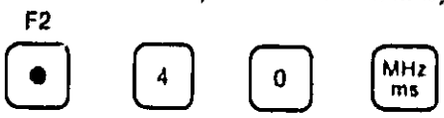
c. Set the 8350A LINE switch from OFF to ON. Press the INSTR PRESET key.

d. Set the 8350A HP-IB address to "0" by pressing:

(blue)

e. Set the 8350A Plug-In CW FILTER to OFF, RF to ON, and adjust the power for ~ 0.0 dBm.

f. Set the 5344A mode to CF/ΔF, and enter a CF frequency within the plug-in range (example: 2.0 GHz). Enter a ΔF sweepwidth of 40 MHz by pressing:



g. Set up the 5344A for a sweep time of 1 second, by pressing:

h. Press the 5344A AUTO LOCK key.

i. Verify that the 8350A displays the programmed CF (2.0 GHz), as the CW frequency, and that the 8350A output sweep is as programmed (40 MHz sweep, centered at 2 GHz, at a one-second rate).

j. Press the AUTO LOCK key to the off position (key indicator light goes off).

k. Set the 8350A to the lower limit of the plug-in's frequency range, plus 20 MHz. Repeat steps h and i.

l. Press the AUTO LOCK key to the off position.

m. Set the 8350A to the upper limit of the plug-in's frequency range, minus 20 MHz. Repeat steps h and i.

n. Record the results on the Performance Test Record, *Table 4-2*.

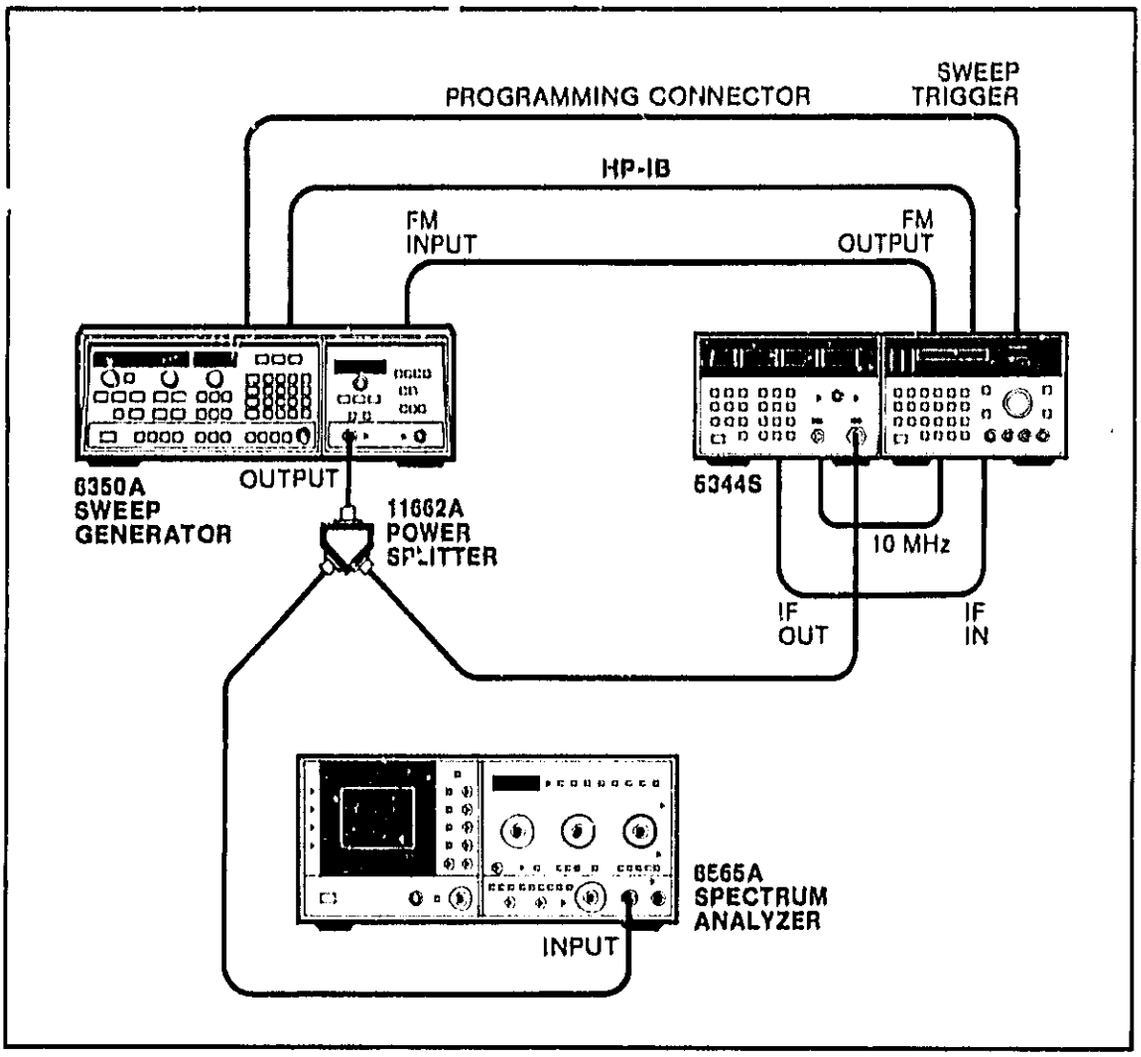


Figure 4-6. Auto Lock Test Setup

4-23. HP-IB VERIFICATION

4-24. The HP 85A program listed in *Table 4-3* exercises the 53445 through various operating mode. via its HP-IB Interface. If the 53445 successfully completes all phases of the verification program, there is a high probability that the HP-IB Interface (A4 assembly) is working properly.

NOTE

For the following tests a Spectrum Analyzer is not necessary but is helpful to observe the results.

4-25. To perform the verification, set up the equipment as shown in *Figure 4-7* (for the 8350A) or Figure 4-8 (for the 8620A/B/C). The program listed in *Table 4-3* may be keyed into the HP 85A, or loaded from an HP-IB Verification Cassette, HP P/N 59300-10002. To run the program from cassette, insert the cassette into the HP 85A and power-up the controller. If the controller power is already on, insert the cassette and type:

CHAIN "Autost"

then press END LINE. Press the solft key corresponding to 53445 and follow the instructions shown on the HP 85A screen.

4-26. The program begins by requesting the following information:

1. The 53445 system select code (e.g."703").
2. System microwave frequency counter (e.g. HP 5342A or HP 5343A).
3. Is the configured sweep oscillator a programmable HP 8350A?

4-27. After this initial information is entered, the program goes through 18 Check Points. The HP 85A display provides the necessary Check Point description and operator instructions, as each test is performed. At the end of the last test, the operator is given the opportunity to randomly repeat any test(s), or end the program. Record the results on the Performance Test Record, *Table 4-2*.

CHECK POINT #1 ..... INSTRUMENT PRESET
CHECK POINT #2 ..... REMOTE
CHECK POINT #3 ..... CW MODE
CHECK POINT #4 ..... CF /DF/ST MODE
CHECK POINT #5 ..... STRT/STOP MODE
CHECK POINT #6 ..... LOCK/ROLL MODE
CHECK POINT #7 ..... MARKER FREQUENCIES
CHECK POINT #8 ..... STEP SIZE and UP/DN
CHECK POINT #9 ..... LOCK MODE
CHECK POINT #10 ..... ACQUIRE
CHECK POINT #11 ..... RESET
CHECK POINT #12 ..... WIDE/NARROW BANDWIDTH
CHECK POINT #13 ..... SUBHARMONIC/OFFSET LOCKING MODE
CHECK POINT #14 ..... SINGLE SWEEP/TRIGGER MODE
CHECK POINT #15 ..... STATUS BYTE/REQUIRE SERVICE OUT OF LOCK
CHECK POINT #16 ..... STATUS BYTE/REQUIRE SERVICE END OF SWEEP
CHECK POINT #17 ..... LOCAL LOCKOUT
CHECK POINT #18 ..... GO TO LOCAL

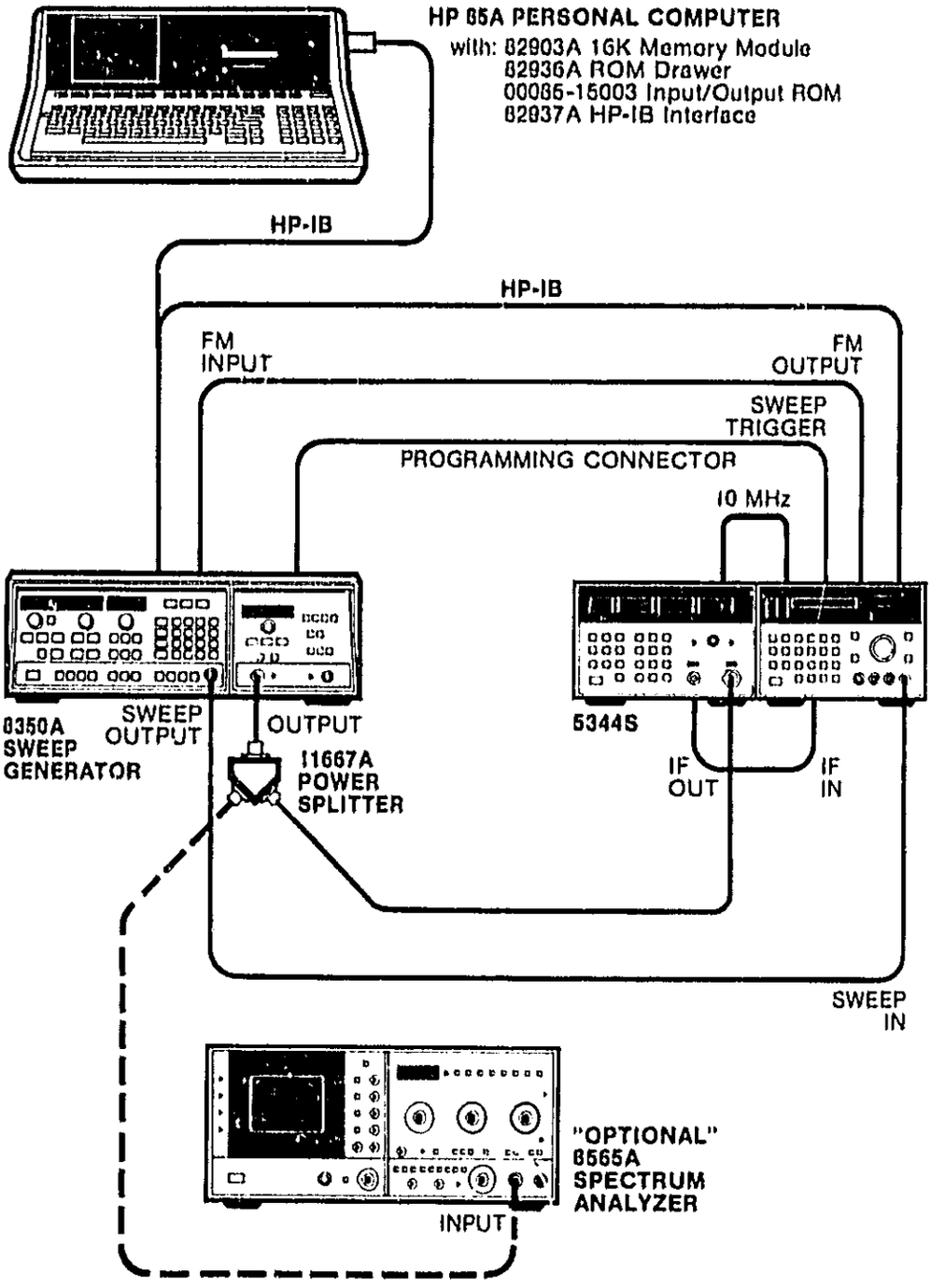


Figure 4-7. HP-IB Verification Test Setup for 8350A

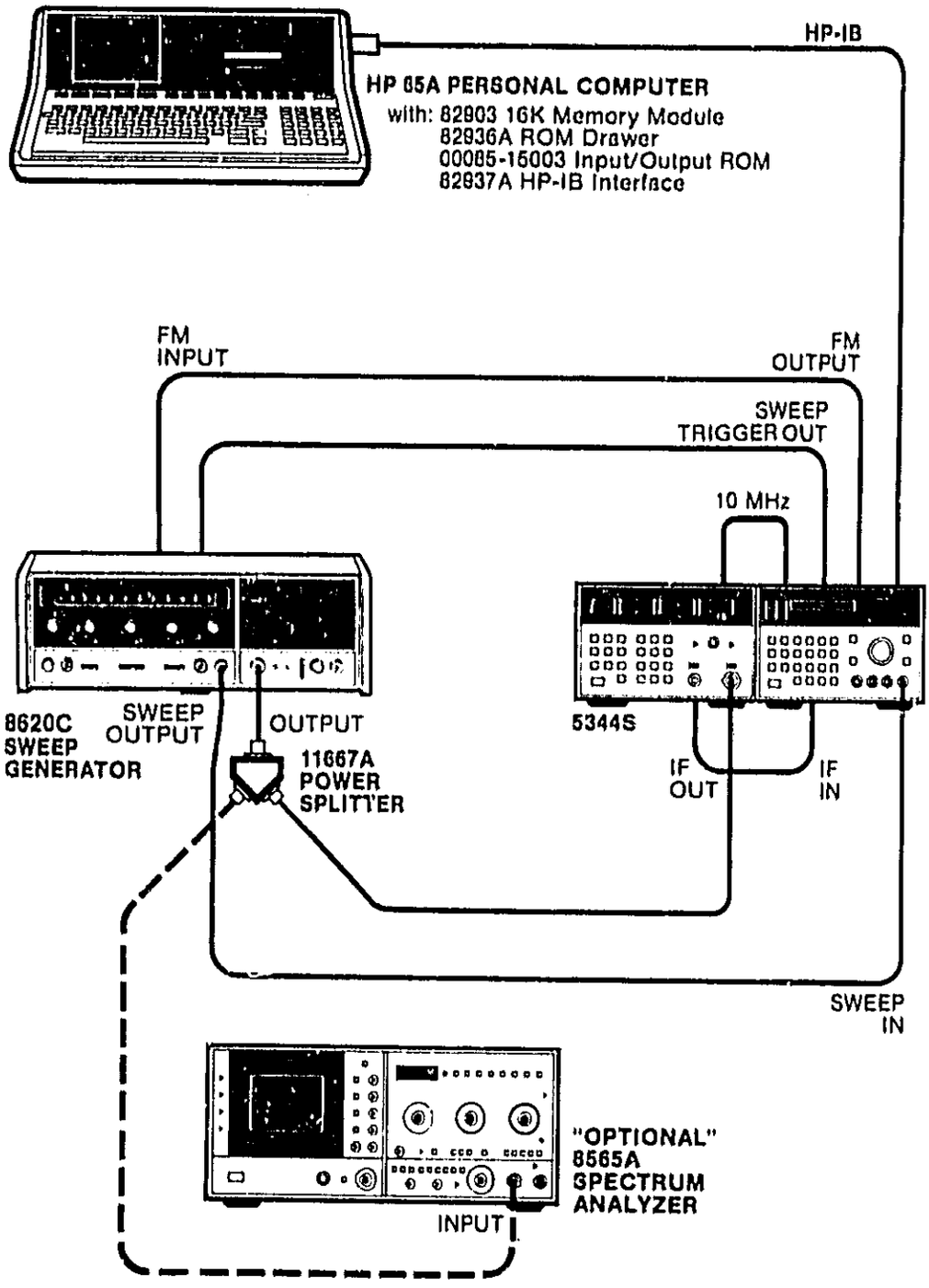


Figure 4-8. HP-IB Verification Test Setup for 8620A/B/C

Table 4-2. Performance Test Record

HEWLETT-PACKARD 53445
SOURCE SYNCHRONIZER

Date _____

Test Performed by _____ Serial No. _____

PARAGRAPH NUMBER	TEST/STEP	PASS/FAIL
4-14. KEYBOARD AND DISPLAY ANNUNCIATOR		
	Step c.	
	Step d.	
	Step e.	
	Step f.	
	Step g.	
	Step h.	
	Step i.	
	Step j.	
	Step k.	
	Step l.	
	Step m.	
	Step n.	
	Step o.	
4-15. CW/MANUAL LOCK		
	Step e.	
	Step f.	
	Step g.	
	Step h.	
	Step j.	
	Step l.	
4-16. CF/ΔF and START/STOP		
	Step f.	
	Step i.	
	Step j.	
	Step l.	
	Step n.	
	Step p.	
	Step r.	

PARAGRAPH NUMBER	TEST/STEP	PASS/FAIL
4-17. STEP SIZE		
	Step f.	
	Step i.	
	Step j.	
	Step l.	
	Step m.	
	Step n.	
4-18. MARKER		
	Step f.	
	Step i.	
	Step j.	
	Step l.	
	Step n.	
	Step p.	
	Step r.	
4-19. SUBHARMONIC LOCKING		
	Step e.	
	Step f.	
	Step g.	
	Step h.	
	Step k.	
	Step l.	
	Step n.	
	Step p.	
4-20. CAPTURE RANGE		
	Step f.	
	Step g.	
	Step i.	

Table 4-2. Performance Test Record (Continued)

HEWLETT-PACKARD 53445
SOURCE SYNTHESIZER

Date _____

Test Performed by _____ Serial No. _____

PARAGRAPH NUMBER	TEST/STEP	PASS/FAIL	PARAGRAPH NUMBER	TEST/STEP	PASS/FAIL
4-21. LK/R (LOCK AND ROLL					
	Step i.				
	Step k.				
4-22. AUTO LOCK					
	Step b.				
	Step i.				
	Step k.				
	Step m.				
4-23. HP-IB					
	Check Point 1.				
	Check Point 2.				
	Check Point 3.				
	Check Point 4.				
	Check Point 5.				
	Check Point 6.				
	Check Point 7.				
	Check Point 8.				
	Check Point 9.				
	Check Point 10.				
	Check Point 11.				
	Check Point 12.				
	Check Point 13.				
	Check Point 14.				
	Check Point 15.				
	Check Point 16.				
	Check Point 17.				
	Check Point 18.				

Table 4-3. Model HP 85A Operation Verification Program for HP 53445

```
10 ! 5344A HP-IB VERIFICATION PROGRAM ******** "5344A" ********
20 ENABLE KBD 1+32
30 ON KEY# 2,"5342A" GOTO 6350
40 ON KEY# 3,"5343A" GOTO 6360
50 DIM A$[40],B$[40],C$[40],D$[40],E$[40],F$[40],G$[40],H$[60],I$[60]
60 A$="Press 'CONT' to perform test."
70 B$="Press 'CONT' when done."
80 C$="Verify that 5344A front panel"
90 D$="Verify that 5344A display"
100 E$="After pressing 'CONT',"
110 I$="Press 'CONT' for next display."
120 F$="       CHECK POINT #"
130 G$="------------------------------"
140 L=0 @ CRT IS 1 @ PRINTER IS 2
150 !
160 ! DISPLAYS SETUP INSTRUCTIONS AND GETS 5344A HP-IB ADDRESS
170 !
180 CLEAR @ GOSUB 5010 @ GOSUB 5020 @ WAIT 1500 @ GOSUB 4920
190 CLEAR @ GOSUB 5010 @ GOSUB 5060
200 CLEAR @ GOSUB 5010 @ GOSUB 5020 @ GOSUB 5170
210 IF NOT (S=721) THEN 230 ELSE DISP "ERROR: Calculator Address!!"
220 DISP "calculator address=computer dump" @ WAIT 2000 @ GOTO 200
230 IF NOT (S>730) THEN 250 ELSE DISP "out of address range }high"
240 WAIT 2000 @ GOTO 200
250 IF NOT (S<700) THEN 300 ELSE DISP "out of address range }low"
260 WAIT 2000 @ GOTO 200
270 !
280 ! DISPLAYS SOFT KEY LABELS FOR ENTERING 5342A OR 5343A
290 !
300 CLEAR @ KEY LABEL
310 GOSUB 6200
320 GOTO 320
330 !
340 ! GETS UPPER LIMIT OF PLUG-IN
350 !
360 GOSUB 6270
370 !
380 ! ASKS IF USING A PROGRAMMABLE SWEEPER; IF YES, GETS HP-IB ADDRESS
390 !
400 CLEAR @ DISP @ DISP @ GOSUB 6050
410 IF S5<>0 THEN OUTPUT S5 ;"IP" @ WAIT 1500
420 IF S5<>0 THEN OUTPUT S5 ;"CW1GZPL-10DMRF1A1FI0CW"
430 !
440 H$="----- INSTRUMENT PRESET -----"
450 Z=1 @ GOSUB 4960 @ OUTPUT S ;"IP"
460 DISP "5344A is set to power up"
470 DISP "conditions by controller," @ DISP D$
480 DISP "annunciator CW is lighted and"
490 DISP "5344A numeric display is","0.000000 MHz."
500 DISP C$ @ DISP "F1 key is lighted." @ DISP @ DISP B$ @ PAUSE
510 WAIT 200 @ REMOTE S
520 IF L<>0 THEN 4540 ELSE GOSUB 4920
530 !
540 !
550 H$="---------- REMOTE ----------"
```

Table 4-3. Model HP 85A Operation Verification Program for HP 53445 (Continued)

```
560 Z=2 @ GOSUB 4960 @ REMOTE S
570 DISP D$ @ DISP "annunciator RMT and LSN are","lighted."
580 DISP "This indicates 5344A is in","REMOTE mode." @ DISP @ DISP B$ @
PAUSE
590 IF L<>0 THEN 4540 ELSE GOSUB 4920
600 !
610 !
620 H$="---------- CW mode ----------"
630 Z=3 @ GOSUB 4960
640 DISP "Enter a Continuous Wave"
650 DISP "frequency in MHz between 500 MHz"
660 DISP "and";F3;"MHz. Then press","'END LINE'."
670 DISP @ INPUT X@ GOSUB 4960
680 IMAGE "CW",K,"MZ"
690 IF FNR(X) THEN 640
700 X=FNT(X) @ OUTPUT S USING 680 ; X
710 DISP D$ @ DISP "annunciator CW is lighted and"
720 DISP "display is:";@ GOSUB 5310
730 DISP C$ @ DISP "F1 key is lighted." @ DISP @ DISP B$ @ PAUSE
740 IF L<>0 THEN 4540 ELSE GOSUB 4920
750 !
760 !
770 H$="------- CF/" @ M$="F/ST mode -------"
780 Z=4 @ GOSUB 4970
790 DISP "Enter a Center Frequency in"
800 DISP "MHz between 500 MHz and"
810 DISP F3;"MHz. Press 'END LINE'." @ DISP @ INPUT X@ GOSUB 4970
820 IMAGE "CF",K,"MZ"
830 IF FNR(X) THEN 790
840 X=FNT(X) @ OUTPUT S USING 820 ; X
850 DISP D$ @ DISP "annunciators CF and ";CHR$(8);"F are"
860 DISP "lighted and 5344A display is:" @ T1=X @ GOSUB 5310
870 DISP C$ @ DISP "F1 key is lighted."
880 DISP @ DISP B$ @ PAUSE
890 GOSUB 4970
900 DISP "Enter a Delta Frequency in MHz"
910 DISP "between 0 MHz and 40 MHz.","Press 'END LINE'.",,"CAUTION!"
920 DISP CHR$(8);"F must be such that"
930 DISP "CF-";CHR$(8);"F/2 > 500MHz and CF+";CHR$(8);"F/2 <"
940 DISP F3;"MHz." @ DISP @ INPUT Y@ GOSUB 4970
950 IF Y<0 OR Y>40 THEN 970
960 IF NOT (T1-Y/2<500 OR T1+Y/2>F3) THEN 990
970 DISP "LIMIT ERROR OR RANGE ERROR" @ GOTO 900
980 IMAGE "DF",K,"MZ"
990 Y=FNT(Y) @ OUTPUT S USING 980 ; Y
1000 DISP D$ @ DISP "annunciators CF and ";CHR$(8);"F are"
1010 DISP "lighted and display is:" @ X=Y @ GOSUB 5310
1020 DISP C$ @ DISP "F2 key is lighted."
1030 DISP @ DISP B$ @ PAUSE
1040 GOSUB 4970
1050 DISP "Enter a Sweep Time in seconds"
1060 DISP "between 1 s and 100 s. Press","'END LINE'."
1070 DISP @ INPUT X@ GOSUB 4970
1080 IF NOT (X<1 OR X>100) THEN 1100
1090 DISP "LIMIT ERROR ON INPUT" @ GOTO 1050
```

Table 4-3. Model HP 85A Operation Verification Program for HP 5344S (Continued)

```
1100 IF X<10 THEN X=IP(X*100)/100 ELSE X=IP(X*10)/10
1110 IMAGE "ST",K,"SC"
1120 OUTPUT S USING 1110 ; X
1130 DISP D$ @ DISP "annunciators CF and ";CHR$(8);"F are"
1140 DISP "lighted and display is:";
1150 IF X<10 THEN DISP USING 5630 ; X ELSE DISP USING 5610 ; X
1160 DISP C$ @ DISP "SWP TIME key is lighted."
1170 DISP @ DISP B$ @ PAUSE
1180 GOSUB 4970
1190 DISP "Enter a Sweep Time in milli-"
1200 DISP "seconds between 10 ms and","999 ms. Press 'END LINE'."
1210 DISP @ INPUT X@ GOSUB 4970
1220 IF NOT (X<10 OR X>=1000) THEN 1240
1230 DISP "LIMIT ERROR ON INPUT" @ GOTO 1190
1240 IF X<100 THEN X=IP(X*10)/10 ELSE X=IP(X)
1250 IMAGE "ST",K,"MS"
1260 OUTPUT S USING 1250 ; X @ DISP D$
1270 DISP "annunciators CF and ";CHR$(8);"F are"
1280 DISP "lighted and display is:";
1290 IF X<100 THEN DISP USING 5620 ; X ELSE DISP X;"ms."
1300 DISP C$ @ DISP "SWP TIME key is lighted."
1310 DISP @ DISP B$ @ PAUSE
1320 IF L<>0 THEN GOTO 4540 ELSE GOSUB 4920
1330 !
1340 !
1350 H$="------- STRT/STOP mode -------"
1360 Z=5 @ GOSUB 4960 @ OUTPUT S ;"CF1GZDF4OMZCF"
1370 DISP "Enter a Start frequency in MHz"
1380 DISP "between 980 MHz and 1000 MHz.","Press 'END LINE'."
1390 DISP @ INPUT X@ GOSUB 4960
1400 IF NOT (X<980 OR X>1000) THEN 1420
1410 DISP "LIMIT ERROR!!" @ GOTO 1370
1420 IMAGE "SR",K,"MZ"
1430 X=FNT(X) @ OUTPUT S USING 1420 ; X @ DISP D$
1440 DISP "annunciators STRT and STOP are"
1450 DISP "lighted and display is:" @ GOSUB 5310 @ DISP C$
1460 DISP "F1 key is lighted." @ DISP @ DISP B$ @ PAUSE
1470 GOSUB 4960
1480 DISP "Enter a Stop frequency in MHz"
1490 DISP "between 1000 MHz and 1020 MHz.","Press 'END LINE'."
1500 DISP @ INPUT X@ GOSUB 4960
1510 IF NOT (X<1000 OR X>1020) THEN 1530
1520 DISP "LIMIT ERROR!!" @ GOTO 1480
1530 IMAGE "SP",K,"MZ"
1540 X=FNT(X) @ OUTPUT S USING 1530 ; X @ DISP D$
1550 DISP "annunciators STRT and STOP are"
1560 DISP "lighted and display is:" @ GOSUB 5310 @ DISP C$
1570 DISP "F2 key is lighted." @ DISP @ DISP B$ @ PAUSE
1580 IF L<>0 THEN 4540 ELSE GOSUB 4920
1590 !
1600 !
1610 H$="------- LOCK/ROLL mode -------"
1620 Z=6 @ GOSUB 4960 @ DISP "5344A programmed for LOCK/ROLL","mode."
1630 DISP "Enter a starting frequency"
1640 DISP "between 500 MHz and";F3;"MHz.","Press 'END LINE'."
```

Table 4-3. Model HP 85A Operation Verification Program for HP 53445 (Continued)

```
1650 DISP @ INPUT X@ GOSUB 4960
1660 IF FNR(X) THEN 1630
1670 IMAGE "LR",K,"MZ"
1680 X=FNT(X) @ OUTPUT S USING 1670 ; X @ DISP D$
1690 DISP "annunciator LK/R is lighted"
1700 DISP "and display is:";@ GOSUB 5310
1710 DISP C$ @ DISP "F1 key is lighted."
1720 DISP @ DISP B$ @ PAUSE
1730 IF L<>0 THEN 4540 ELSE GOSUB 4920
1740 !
1750 !
1760 H$="---- MARKER FREQUENCIES ----"
1770 Z=7 @ GOSUB 4960 @ OUTPUT S ;"CF1GZDF40MZCF"
1780 DISP "Up to 4 Marker Frequencies can"
1790 DISP "be entered in one sweep","interval. However, the marker"
1800 DISP "frequencies cannot be too close","to each other or to the start"
1810 DISP "and stop frequencies. The","separation depends on sweep"
1820 DISP "time and interval. Refer to","Operating Manual for details."
1830 DISP @ DISP B$ @ PAUSE
1840 FOR I=1 TO 4 @ GOSUB 4960
1850 DISP "Enter Marker Frequency";I;"in MHz"
1860 DISP "between 500 MHz and";F3;"MHz.","Press 'END LINE'."
1870 DISP @ INPUT X@ GOSUB 4960
1880 IF FNR(X) THEN 1850
1890 IMAGE "M",K,K,"MZ"
1900 X=FNT(X) @ OUTPUT S USING 1890 ; I,X
1910 DISP "MARKER FREQUENCY";I;":" @ DISP D$
1920 DISP "annunciators CF and ";CHR$(8);"F are"
1930 DISP "lighted and display is:" @ GOSUB 5310 @ DISP C$
1940 DISP "MKR FREQ key is lighted." @ DISP @ DISP B$ @ PAUSE
1950 NEXT I
1960 IF L<>0 THEN 4540 ELSE GOSUB 4920
1970 !
1980 !
1990 H$="---- STEP SIZE and UP/DN ----"
2000 Z=8 @ GOSUB 4960 @ OUTPUT S ;"CW1GZ"
2010 DISP "5344A is placed in CW mode by","controller."
2020 DISP "Enter a Step Size between","0 MHz and";F3;"MHz."
2030 DISP "Press 'END LINE'." @ INPUT X@ GOSUB 4960
2040 IF NOT (X<0 OR X>F3) THEN 2060
2050 DISP "LIMIT ERROR!!" @ GOTO 2020
2060 IMAGE "SS",K,"MZ"
2070 X=FNT(X) @ OUTPUT S USING 2060 ; X @ DISP D$
2080 DISP "annunciator CW is lighted"
2090 DISP "and display is:";@ T1=X @ GOSUB 5310 @ DISP C$
2100 DISP "STEP SIZE key is lighted." @ DISP @ DISP B$ @ PAUSE
2110 OUTPUT S ;"CW1GZ"
2120 GOSUB 4960 @ DISP D$ @ DISP "annunciator CW is lighted"
2130 DISP "and display is: 1.000000000 GHz." @ DISP @ DISP B$ @ PAUSE
2140 GOSUB 4960 @ DISP "When the 5344A receives the UP"
2150 DISP "then DN command from the HP-85,"
2160 DISP "v";D$[2]
2170 DISP "is incremented 3 times by" @ X=T1 @ GOSUB 5310
2180 DISP "Then verify that 5344A display"
2190 DISP "is decremented 3 times by" @ X=T1 @ GOSUB 5310
```

Table 4-3. Model HP 85A Operation Verification Program for HP 53445 (Continued)

```
2200 DISP "Press 'CONT' to send the UP then","DN command." @ PAUSE
2210 FOR I=1 TO 6
2220 IF NOT (I>3) THEN OUTPUT S ;"UP" ELSE OUTPUT S ;"DN"
2230 BEEP @ WAIT 1500
2240 NEXT I
2250 DISP B$ @ PAUSE
2260 IF L<>0 THEN 4540 ELSE GOSUB 4920
2270 !
2280 !
2290 H$="--------- LOCK mode ---------"
2300 Z=9 @ GOSUB 4960 @ GOSUB 5400
2310 GOSUB 4960 @ DISP "When the LOCK command is sent"
2320 DISP "to the 5344A by the controller,","the Lock routine is initiated."
2330 DISP D$
2340 DISP "annunciator FREQ HI or FREQ LO","lights then the LOCKED"
2350 DISP "annunciator lights and remains","lighted."
2360 DISP "Press 'CONT' to send LOCK","command." @ PAUSE
2370 OUTPUT S ;"LK1" @ GOSUB 4960 @ DISP "Verify the 10 segment meter on"
2380 DISP "5344A display sweeps at 5","second intervals."
2390 DISP C$ @ DISP "MANUAL LOCK key is lighted." @ DISP @ DISP B$ @ PAUSE
2400 OUTPUT S ;"LK0"
2410 IF L<>0 THEN 4540 ELSE GOSUB 4920
2420 !
2430 !
2440 H$="---------- ACQUIRE ----------"
2450 Z=10 @ GOSUB 4960 @ OUTPUT S ;"DF40MZST5SCDFLK0"
2460 IF S5<>0 THEN 5900
2470 DISP "Set sweep oscillator to CW","operation at any desired"
2480 DISP "frequency between 520 MHz and",F9-20;"MHz."
2490 DISP @ DISP B$ @ PAUSE
2500 IF S5=0 THEN GOSUB 4960
2510 DISP "The 5344A acquires the signal"
2520 DISP "from the sweep oscillator as its"
2530 DISP "Center Frequency. ";CHR$(8);"F and ST have"
2540 DISP "been preset to 40 MHz and 5","seconds respectively by the"
2550 DISP "controller." @ DISP @ DISP A$ @ PAUSE
2560 OUTPUT S ;"CFAQLK1" @ GOSUB 4960 @ DISP D$[1,17];" has"
2570 DISP "acquired the signal from the","sweep oscillator as its CF."
2580 DISP "The LOCKED annunciator and the","MANUAL LOCK key should be"
2590 DISP "lighted.","The 5344A should be sweeping at"
2600 DISP "5 second intervals indicated by"
2610 DISP "the 10 segment meter." @ DISP @ DISP B$ @ PAUSE
2620 OUTPUT S ;"LKOMO"
2630 IF L<>0 THEN 4540 ELSE GOSUB 4920
2640 !
2650 !
2660 H$="---------- RESET ----------"
2670 Z=11 @ GOSUB 4960 @ GOSUB 5400 @ GOSUB 4960 @ OUTPUT S ;"LK1"
2680 DISP "5344A should be in LOCK mode","and sweeping."
2690 DISP @ DISP I$ @ PAUSE
2700 GOSUB 4960 @ DISP "When the 5344A receives the",
2710 DISP "RESET command, the sweep"
2720 DISP "in progress is interrupted and","a new lock routine is"
2730 DISP "initiated. FREQ HI or FREQ LO","then LOCKED annunciators should"
2740 DISP "light. Front panel parameters","should remain unchanged."
```

Table 4-3. Model HP 85A Operation Verification Program for HP 5344S (Continued)

```
2750 DISP "Press 'CONT' to RESET 5344A." @ PAUSE
2760 OUTPUT S ;"RT" @ WAIT 2000 @ BEEP ) DISP B$ @ PAUSE
2770 OUTPUT S ;"LK0"
2780 IF L<>0 THEN 4540 ELSE GOSUB 4920
2790 !
2800 !
2810 H$="---- WIDE/NARROW BANDWIDTH ----"
2820 Z=12 @ GOSUB 4960 @ GOSUB 5400 @ GOSUB 4960 @ OUTPUT S ;"BW1LK1"
2830 DISP "5344A should be in LOCK mode","and sweeping."
2840 DISP C$ @ DISP "MANUAL LOCK key is lighted."
2850 DISP "This indicates Wide Locking Loop","Bandwidth."@DISP@DISP B$ @ PAUSE
2860 OUTPUT S ;"BW0" @ GOSUB 4960 @ DISP C$
2870 DISP "MANUAL LOCK key is flashing.","This indicates Narrow Locking"
2880 DISP "Loop Bandwidth." @ DISP @ DISP B$ @ PAUSE
2890 OUTPUT S ;"BW1LK0"
2900 IF L<>0 THEN 4540 ELSE GOSUB 4920
2910 !
2920 !
2930 H$="SUBHARMONIC/OFFSET LOCKING mode "
2940 Z=13 @ GOSUB 4960 @ OUTPUT S ;"CW1GZBW1LK0"
2950 DISP "Enter a Center Frequency between","500 MHz and 99999.999999 MHz."
2960 DISP "Press 'END LINE'." @ DISP @ INPUT Y1@ GOSUB 4960
2970 IF NOT (Y1<500 OR Y1>=100000) THEN 2990
2980 DISP "LIMIT ERROR!!" @ GOTO 2950
2990 Y1=FNT(Y1) @ T3=IP(Y1/500) @ T4=IP(Y1/F9)
3000 T3=T3-1 @ T4=T4+1 @ IF T3<1 THEN T3=1
3010 IF T3>99 THEN T3=99
3020 DISP "Enter a Frequency Multiplier,"
3030 DISP "an integer between";T4;"and";T3;"."
3040 DISP "Press 'END LINE'."
3050 DISP @ INPUT Y2@ GOSUB 4960
3060 IF NOT (FP(Y2)=0) THEN 3090
3070 IF Y2<T4 OR Y2>T3 THEN 3090
3080 X=Y1/Y2 @ IF FNR(X) THEN 3020 ELSE 3100
3090 DISP "LIMIT ERROR: CF/FM OUT OF RANGE","OR FM NOT INTEGER!!" @ GOTO 3020
3100 X=FNT(X) @ T1=X @ IF S5<>0 THEN GOSUB 6000
3110 DISP "In Subharmonic Locking mode,"
3120 DISP "The 5344A uses CF/FM as","the locking frequency. The"
3130 IF S5<>0 THEN DISP "8350A has been programmed for" @ GOTO 3150
3140 DISP "sweep oscillator must be set to"
3150 DISP "approximately this frequency,"
3160 DISP " CF/FM, ";@ GOSUB 5330 @ DISP @ DISP A$ @ PAUSE
3170 GOSUB 4960
3180 IMAGE "SH1FM",K,"HZCF",K,"MZDF40MZST1SCLK0CF"
3190 OUTPUT S USING 3180 ; Y2 ^1
3200 X=Y1 @ DISP D$ @ DISP "is:";@ GOSUB 5350
3210 DISP "Verify rightmost decimal place","is lighted. To achieve LOCK,"
3220 DISP "verify sweep oscillator is","set at approximately:";@ X=T1
3230 GOSUB 5330
3240 DISP "Press 'CONT' to place 5344A in"
3250 DISP "LOCK mode." @ PAUSE
3260 GOSUB 4960
3270 OUTPUT S ;"LK1" @ DISP @ DISP D$ @ DISP "annunciator LOCKED is lighted."
3280 DISP "Verify rightmost decimal place","is lighted."
3290 DISP @ DISP B$ @ PAUSE
```

Table 4-3. Model HP 85A Operation Verification Program for HP 53445 (Continued)

```
3300 OUTPUT S ;"LKOSHOCW1GZ"
3310 IF L<>0 THEN 4540 ELSE GOSUB 4920
3320 !
3330 !
3340 H$="-- SINGLE SWEEP/TRIGGER mode --"
3350 Z=14 @ GOSUB 4960 @ GOSUB 5400 @ GOSUB 4960
3360 DISP "5344A is programmed for Single","Sweep mode. 5344A is put in"
3370 DISP "LOCK mode by controller.","The HP-85 BEEPS 3 times."
3380 DISP "With each BEEP from the HP-85,","a new sweep is initiated as"
3390 DISP "indicated by the 10 segment","meter."
3400 DISP @ DISP I$ @ PAUSE
3410 OUTPUT S ;"TR1LK1ST" @ GOSUB 4960 @ WAIT 1000
3420 DISP D$ @ DISP "annunciator LOCKED is lighted."
3430 DISP "5344A numeric display should be:","S.S.     5.00s."
3440 DISP "Press 'CONT' to initiate sweeps." @ DISP @ PAUSE
3450 FOR I=1 TO 3
3460 OUTPUT S ;"TS" @ BEEP @ DISP "SWEEP ";I;" INITIATED." @ WAIT 6500
3470 NEXT I @ DISP @ DISP B$ @ PAUSE
3480 OUTPUT S ;"LKOTROCF"
3490 IF L<>0 THEN 4540 ELSE GOSUB 4920
3500 !
3510 !
3520 H$="  STATUS BYTE/REQUIRE SERVICE              OUT OF LOCK"
3530 Z=15 @ GOSUB 4960 @ GOSUB 5400 @ GOSUB 4960
3540 OUTPUT S ;"LK1"
3550 DISP "5344A is programmed for LOCK","mode and REQUIRE SERVICE message"
3560 DISP "is enabled. If 5344A goes out","of lock, the REQUIRE SERVICE"
3570 DISP "message is sent causing","the program to jump to a"
3580 DISP "service routine." @ DISP @ DISP I$ @ PAUSE
3590 GOSUB 4960
3600 DISP "In the service routine, the","Status Byte is read and"
3610 DISP "displayed by the HP-85. The","program causes the 5344A"
3620 DISP "to go out of lock, FREQ HI,","then FREQ LO, and the Status"
3630 DISP "Byte is displayed on the HP-85."
3640 ON INTR 7 GOTO 4700
3650 ENABLE INTR 7;8 @ OUTPUT S ;"RM1"
3660 DISP @ DISP A$ @ PAUSE
3670 OUTPUT S ;"CF1GZ" @ WAIT 1000
3680 OUTPUT S ;"CF3GZ" @ WAIT 1000 @ ENABLE INTR 7;8
3690 OUTPUT S ;"CF2GZ" @ WAIT 1000
3700 OUTPUT S ;"RMOLKO"
3710 IF L<>0 THEN 4540 ELSE GOSUB 4920
3720 !
3730 !
3740 H$="STATUS BYTE/REQUIRE SERVICE              END OF SWEEP"
3750 Z=16 @ GOSUB 4960
3760 DISP "5344A is programmed for Single","Sweep LOCK/ROLL mode. Consult"
3770 DISP "Service Manual for proper sweep","oscillator settings and 5344A"
3780 DISP "hookup procedures for LOCK/ROLL mode."
3790 DISP @ DISP I$ @ PAUSE
3800 GOSUB 4960
3810 IF S5=0 THEN 3840
3820 DISP "8350A has been programmed for","a wide sweep equal to 600MHz."
3830 OUTPUT S5 ;"FI0DF600MZST1SCPL-10DMT3RF1A1DF" @ GOTO 3850
3840 DISP "Sweep oscillator should be set","for a wide sweep(e.g. 400MHz)."
```

Table 4-3. Model HP 85A Operation Verification Program for HP 53445 (Continued)

```
3850 DISP "Program asks for a starting","frequency for LOCK/ROLL between"
3860 IF S5<>0 THEN DISP "500 MHz and";F9-600;"MHz. The" @ GOTO 3880
3870 DISP "500 MHz and";F9;"MHz. The"
3880 DISP "REQUIRE SERVICE message is"
3890 DISP "enabled and interrupts program","at the end of each sweep."
3900 DISP @ DISP I$ @ PAUSE
3910 GOSUB 4960
3920 DISP "Enter a Starting Frequency","in MHz between 500MHz and"
3930 IF S5<>0 THEN DISP F9-600;"MHz. Press 'END LINE'." @ GOTO 3950
3940 DISP F9;"MHz. Press 'END LINE'."
3950 IF S5=0 THEN 3980
3960 DISP "(NOTE: The 8350A will be","programmed with the starting"
3970 DISP "frequency entered here.)" @ GOTO 4010
3980 DISP "(NOTE: This frequency must be","the same as the starting"
3990 DISP "frequency of the sweep","oscillator to achieve"
4000 DISP "LOCK/ROLL mode.)"
4010 DISP @ INPUT X@ GOSUB 4960
4020 IF S5=0 THEN 4040
4030 IF NOT (X>F9) THEN 4070 ELSE 4050
4040 IF NOT (X+600>F9) THEN 4070
4050 DISP "ERROR: Stop frequency out of","range of sweep oscillator"
4060 DISP "plug-in." @ GOTO 3920
4070 IF FNR(X) THEN 3920
4080 X=FNT(X)
4090 IMAGE "LR",K,"MZTR1RM2LK1"
4100 IMAGE "FA",K,"MZFB",K,"MZ"
4110 IF S5<>0 THEN OUTPUT S5 USING 4100 ; X,X+600
4120 OUTPUT S USING 4090 ; X @ WAIT 2000
4130 DISP D$ @ DISP "annunciator LK/R is lighted"
4140 DISP "and display is:";@ GOSUB 5310
4150 DISP C$ @ DISP "MANUAL LOCK key is lighted." @ DISP D$
4160 DISP "annunciator LOCKED is lighted." @ DISP @ DISP B$ @ PAUSE
4170 GOSUB 4960 @ ON INTR 7 GOTO 4860
4180 DISP "The HP-85 will initiate 3","sweeps. For each sweep the"
4190 DISP "Status Byte will be displayed","during the sweep and at the"
4200 DISP "END OF SWEEP. The Status Byte","should change from 1 during the"
4210 DISP "sweep to 97 at END OF SWEEP." @ DISP @ DISP A$ @ PAUSE
4220 GOSUB 4960 @ DISP "Status Byte during sweep should"
4230 DISP "be 1 and at EOS should be 97."
4240 I=1 @ A=SPOLL(S)
4250 ENABLE INTR 7;8
4260 OUTPUT S ;"TS" @ A=SPOLL(S) @ IF NOT (A=1) THEN 4260
4270 BEEP @ DISP "SWEEP ";I @ DISP "STATUS BYTE during sweep= ";A
4280 WAIT 100 @ GOTO 4280
4290 DISP @ DISP B$ @ PAUSE
4300 OUTPUT S ;"CW1GZTROLKO"
4310 IF L<>0 THEN 4540 ELSE GOSUB 4920
4320 !
4330 !
4340 H$="-------- LOCAL LOCKOUT --------"
4350 Z=17 @ GOSUB 4960 @ LOCAL LOCKOUT 7
4360 DISP "5344A issued LOCAL LOCKOUT","command by controller. Press"
4370 DISP "5344A front panel RESET button","to verify 5344A remains in"
4380 DISP "REMOTE mode." @ DISP @ DISP B$
4390 PAUSE
```

Table 4-3. Model HP 85A Operation Verification Program for HP 53445 (Continued)

```
4400 LOCAL 7
4410 REMOTE S
4420 IF L<>0 THEN 4540 ELSE GOSUB 4920
4430 !
4440 !
4450 H$="-------- GO TO LOCAL --------"
4460 Z=18 @ GOSUB 4960 @ LOCAL S
4470 DISP "5344A programmed in LOCAL mode." @ DISP D$
4480 DISP "annunciator RMT is not lighted.","Press front panel MODE button."
4490 DISP "5344A should switch modes if in","LOCAL." @ DISP @ DISP B$ @ PAUSE
4500 REMOTE S
4510 IF L<>0 THEN 4540 ELSE GOSUB 4920
4520 !
4530 !
4540 CLEAR @ DISP @ DISP "This is the end of the program." @ DISP
4550 DISP "If you need to repeat a Check","Point, enter the Check Point"
4560 DISP "number(1 thru 18) and press","'END LINE', if not, enter 0,"
4570 DISP "and press 'END LINE'." @ DISP @ INPUT L
4580 IF L<0 OR L>18 THEN 4540
4590 IF L=0 THEN 4630
4600 IF L>10 THEN 4620
4610 ON L GOTO 440,550,620,770,1350,1610,1760,1990,2290,2440
4620 ON L-10 GOTO 2660,2810,2930,3340,3520,3740,4340,4450
4630 CLEAR @ GOSUB 4920 @ DISP @ DISP @ DISP @ DISP @ DISP G$ @ DISP
4640 DISP "       END OF 5344S SOURCE       SYNCHRONIZER HP-IB VERIFICATION"
4650 DISP "              TEST" @ DISP @ DISP G$
4660 WAIT 2500 @ LOCAL S @ REWIND @ END
4670 !
4680 ! REQUIRE SERVICE (OUT OF LOCK) interrupt service routine.
4690 !
4700 STATUS 7,1 ; A@ A=SPOLL(S) @ WAIT 500
4710 GOSUB 4960
4720 IF NOT (A=89) THEN 4760
4730 DISP "5344A OUT OF LOCK: FREQ HI."
4740 DISP D$ @ DISP "FREQ HI annunciator is lighted."
4750 DISP "Status Byte should be 89." @ GOTO 4800
4760 IF NOT (A=85) THEN DISP "ERROR IN REQUIRE SERVICE MESSAGE" @ GOTO 3690
4770 DISP "5344A OUT OF LOCK: FREQ LO."
4780 DISP D$ @ DISP "FREQ LO annunciator is lighted."
4790 DISP "Status Byte should be 85."
4800 DISP @ DISP "STATUS BYTE = ";A;@ DISP "  Press 'CONT'." @ PAUSE
4810 IF NOT (A=89) THEN 3690
4820 GOTO 3680
4830 !
4840 ! REQUIRE SERVICE(END OF SWEEP) interrupt service routine.
4850 !
4860 STATUS 7,1 ; A@ A=SPOLL(S)
4870 BEEP @ DISP "STATUS BYTE at EOS = ";A @ I=I+1
4880 IF I=4 THEN 4290
4890 WAIT 1500 @ ENABLE INTR 7;8 @ GOTO 4260
4900 !
4910 !
4920 BEEP @ WAIT 250 @ BEEP @ RETURN
4930 !
4940 ! DISPLAYS CHECK POINT HEADINGS
```

Table 4-3. Model HP 85A Operation Verification Program for HP 5344S (Continued)

```
4950 !
4960 CLEAR @ DISP F$;Z @ DISP H$ @ DISP @ RETURN
4970 CLEAR @ DISP F$;Z @ DISP H$;CHR$(8);M$ @ DISP @ RETURN
4980 !
4990 ! PROGRAM TITLING SUBROUTINE
5000 !
5010 DISP " 5344S HP-IB Verification Test" @ DISP @ RETURN
5020 DISP "   ******** '5344S' ********" @ DISP @ DISP @ RETURN
5030 !
5040 ! SUBROUTINE DISPLAYS VERIFICATION SETUP INSTRUCTIONS
5050 !
5060 DISP "Before beginning the HP-IB"
5070 DISP "Verification program, refer to"
5080 DISP "the 5344A Service Manual for"
5090 DISP "recommended test equipment and"
5100 DISP "instructions for instrument"
5110 DISP "setup. Be sure to follow all"
5120 DISP "hookup procedures and setup"
5130 DISP "instructions carefully." @ DISP @ DISP B$ @ PAUSE @ RETURN
5140 !
5150 ! SUBROUTINE FOR ENTERING 5344A HP-IB ADDRESS
5160 !
5170 DISP "Enter the 3 digit select code","consisting of the 1 digit HP-IB"
5180 DISP "interface select code and the 2","digit primary address that"
5190 DISP "corresponds to your specific","5344A HP-IB address. Then press"
5200 DISP "'END LINE'." @ DISP @ INPUT S@ RETURN
5210 !
5220 ! SUBROUTINE FOR ENTERING 8350A HP-IB ADDRESS
5230 !
5240 DISP "Enter the 3 digit select code","consisting of the 1 digit HP-IB"
5250 DISP "interface select code and the 2","digit primary address that"
5260 DISP "corresponds to your specific","8350A HP-IB address. Then press"
5270 DISP "'END LINE'." @ DISP @ INPUT S5@ RETURN
5280 !
5290 ! SUBROUTINE ACCEPTS X AND DISPLAYS X IN PROPER FORMAT, MHz OR GHz
5300 !
5310 IF X>=1000 THEN X=X/1000 @ DISP USING 5560 ; X ELSE DISP USING 5550; X
5320 RETURN
5330 IF X>=1000 THEN X=X/1000 @ DISP USING 5580 ; X ELSE DISP USING 5570; X
5340 RETURN
5350 IF X>=1000 THEN X=X/1000 @ DISP USING 5600 ; X ELSE DISP USING 5590; X
5360 RETURN
5370 !
5380 ! SUBROUTINE PRESETS 5344A FRONT PANEL PARAMETERS FOR SEVERAL TESTS
5390 !
5400 OUTPUT S ;"CF2GZDF40MZST5SCCFLKO"
5410 IF S5<>0 THEN OUTPUT S5 ;"CW2GZPL-10DMCW"
5420 DISP "The follow. , 5344A parameters"
5430 DISP "are preset by the controller: CF"
5440 DISP "is set at 2 GHz, ";CHR$(8);"F at 40 MHz,"
5450 DISP "and ST at 5 seconds. Sweep"
5460 IF S5<>0 THEN 5500
5470 DISP "oscillator must be set for CW"
5480 DISP "operation at approximately","2 GHz."
5490 DISP @ DISP B$ @ PAUSE @ RETURN
```

Table 4-3. Model HP 85A Operation Verification Program for HP 53445 (Continued)

```
5500 DISP "oscillator, 8350A, has been","remotely programmed for CW"
5510 DISP "operation at 2 GHz." @ DISP @ DISP I$ @ PAUSE @ RETURN
5520 !
5530 ! DISPLAY FORMATTING STATEMENTS
5540 !
5550 IMAGE 3D.6D," MHz."
5560 IMAGE 2D.9D," GHz."
5570 IMAGE 3D.3D," MHz."
5580 IMAGE 2D.3D," GHz."
5590 IMAGE 3D.6D,", MHz."
5600 IMAGE 2D.9D,", GHz."
5610 IMAGE 3D.D," s."
5620 IMAGE 3D.D," ms."
5630 IMAGE D.2D," s."
5640 !
5650 ! THIS FUNCTION GETS A NUMBER AND RETURNS 1 IF IN PROPER RANGE ELSE 0
5660 !
5670 DEF FNR(Y)
5680 IF NOT (Y<500 OR Y>F3) THEN FNR=0 ELSE FNR=1 @ DISP "LIMIT ERROR!!"
5690 FN END
5700 !
5710 ! THIS FUNCTION TRUNCATES NUMBER AFTER 6 DECIMAL PLACES
5720 !
5730 DEF FNT(W)
5740 FNT=IP(W*1000000)/1000000
5750 FN END
5760 !
5770 ! SUBROUTINE FOR SELECTING PROGRAMMABLE OR MANUAL SWEEPER
5780 !
5790 ON KEY# 2,"YES" GOTO 6400
5800 ON KEY# 3,"NO" GOTO 6410
5810 CLEAR @ KEY LABEL
5820 DISP "If your test setup uses an HP-IB","controlled 8350A Sweep"
5830 DISP "Oscillator, press Soft Key #2","for 'YES'. Otherwise, press"
5840 DISP "Soft Key #3 for 'NO'." @ DISP
5850 GOTO 5850
5860 RETURN
5870 !
5880 ! SUBROUTINE FOR PROGRAMMING 8350A WITH ENTERED CW FOR CHECK POINT #10
5890 !
5900 DISP "The 8350A is programmed for CW","operation. Enter a CW frequency"
5910 DISP "between 520 MHz and";F9-20;"MHz.","Press 'END LINE'."
5920 DISP @ INPUT X@ GOSUB 4960
5930 IF NOT (X<520 OR X>F4) THEN 5960
5940 DISP "LIMIT ERROR!!" @ GOTO 5900
5950 IMAGE "FIOCW",K,"MZPL-10DMRF1A1CW"
5960 OUTPUT S5 USING 5950 ; X @ GOTO 2500
5970 !
5980 ! PROGRAMS 8350A WITH CF/FM FROM CHECK POINT #13
5990 !
6000 IMAGE "FIOCW",K,"MZPL-10DMRF1A1CW"
6010 OUTPUT S5 USING 6000 ; T1 @ RETURN
6020 !
6030 ! SUBROUTINE FOR GETTING 8350A HP-IB ADDRESS AND CHECKS FOR ERROR
6040 !
```

Table 4-3. Model HP 85A Operation Verification Program for HP 5344S (Continued)

```
6050 S5=0 @ GOSUB 5790 @ IF NOT (A5=1) THEN 6160
6060 CLEAR @ DISP @ DISP @ GOSUB 5240
6070 IF NOT (S5=S) THEN 6100
6080 DISP "ERROR: 8350A address same as","5344A address."
6090 WAIT 1500 @ GOTO 6060
6100 IF NOT (S5=721) THEN 6120 ELSE DISP "ERROR: Calculator Address!!"
6110 DISP "calculator address=computer dump" @ WAIT 2000 @ GOTO 6060
6120 IF NOT (S5>730) THEN 6140 ELSE DISP "out of address range )high"
6130 WAIT 2000 @ GOTO 6060
6140 IF NOT (S5<700) THEN 6160 ELSE DISP "out of address range )low"
6150 WAIT 2000 @ GOTO 6060
6160 RETURN
6170 !
6180 ! DISPLAY SUBROUTINE FOR SOFT KEY LABELS
6190 !
6200 DISP @ DISP @ DISP "Does your 5344S include a 5342A"
6210 DISP "or a 5343A Microwave Frequency","Counter? Press Soft Key #2 if"
6220 DISP "5342A or Soft Key #3 if 5343A."
6230 RETURN
6240 !
6250 ! SUBROUTINE FOR ENTERING UPPER LIMIT OF SWEEPER PLUG-IN
6260 !
6270 CLEAR @ DISP @ DISP @ DISP "Enter the upper limit frequency"
6280 DISP "in MHz of your specific sweep","oscillator plug-in."
6290 DISP "Press 'END LINE'."
6300 DISP "(NOTE: Entry must be in MHz.)" @ DISP @ INPUT F9@ RETURN
6310 !
6320 ! INITILIZES F3 AND F4 WITH VALUES CORRESPONDING TO USE OF
6330 ! 5342A OR 5343A
6340 !
6350 F3=18000 @ F4=17980 @ GOTO 360
6360 F3=26500 @ F4=26480 @ GOTO 360
6370 !
6380 ! INITIALIZES A5 WITH 1 OR 0 SWEEPER/NO SWEEPER
6390 !
6400 A5=1 @ GOTO 5860
6410 A5=0 @ GOTO 5860
```

SECTION V
ADJUSTMENTS

5-1. INTRODUCTION

5-2. This section describes the adjustments required to maintain the 5344A's operating characteristics within specifications. Adjustments should be made when required, such as after a performance test failure or when components are replaced that may affect an adjustment.

5-3. *Table 5-1* is a list of all adjustable components in the 5344A and indicates the order in which adjustments should be performed.

5-4. EQUIPMENT REQUIRED

5-5. The test equipment required for the adjustment procedures is listed in *Table 1-7*, Recommended Test Equipment. Substitute equipment may be used if it meets the critical specifications.

5-6. ADJUSTMENT LOCATIONS

5-7. Adjustment locations are identified in the component locators in Section VIII (diagrams for the boards) and in the top view of the 5344A, *Figure 8-5*.

5-8. SAFETY CONSIDERATIONS

5-9. This section contains warnings that must be followed for your protection and to avoid equipment damage.

WARNING

ADJUSTMENTS DESCRIBED IN THIS SECTION ARE PERFORMED WITH POWER SUPPLIED TO THE 5344A, AND WITH PROTECTIVE COVERS REMOVED. THE ADJUSTMENTS SHOULD BE PERFORMED ONLY BY SERVICE-TRAINED PERSONS WHO ARE AWARE OF THE HAZARDS INVOLVED IN ELECTRICAL CIRCUITS.

Table 5-1. Adjustments

Name	Adjustment	Function
Power Supply	A12R11(+5V) A12R16(-5.2V) A12R21(+15V) A12R51(-15V)	Sets power supply voltage levels.
VCO	A7L1	Sets VCO tuning voltage.
Ramp peak voltage	A8R3	Sets peak voltage of ramp.
Analog phase interpolation (API)	A9R21 A9R26 A9R1	Sets API circuits to proper levels.

5-10. ADJUSTMENT PROCEDURES

5-11. The adjustment procedures listed in *Table 5-1* are described in the following paragraphs. Remove the top covers of the 5344A as described in paragraph 8-21, apply power and proceed.

5-12. Power Supply Adjustments

5-13. Adjust the +5 volt output as follows:

a. Connect an HP3465 DMM to the +5V test point on A12 board.

b. Adjust A12R11 *(Figure 8-35)* for +5(±0.01) volts on the DMM.

5-14. Adjust the -5.2 volt output as follows:

a. Connect the 3465 to the -5.2V test point on A12 board.

b Adjust A12R16 for -5.2 (±0.02) volts on the DMM.

5-15. Adjust the +15 volt output as follows:

a. Connect the 3465 to the +15V test point on A12 board.

b. Adjust A12R2 for +15(±0.05) volts on the DMM.

5-16. Adjust the -15 volt output as follows:

a. Connect the 3465 to the -15V test point on A12 board.

b. Adjust A12R5 for -15(±0.05) volts on the DMM.

5-17. VCO Adjustment

5-18. Adjust the VCO by adjusting A7L1 (see *Figure 8-30*) as follows:

a. Place A7 VCO assembly on extender board, part number 05342-60030.

b. Press the MODE key repeatedly on the 5344A front panel until LK/R is displayed. Press the F2 key, then the 1 key, 1 key again, then press RESET. This action enters diagnostic 11.

c. Connect a 3465 DMM to A9TP2, VCO Control Voltage (see *Figure 8-32*).

d. Adjust A7L1 with a nonconductive tuning tool for 10.80 (±0.01) volts on the DMM.

e. Press the  key (increment) on the 5344A front panel to enter diagnostic 12.

f. Verify that the 3465 DMM indicates less than 0 volts.

g. Press the RESET key twice to exit the diagnostic mode.

h. Remove the A7 assembly from the extender board and return to the instrument.

5-19. Ramp Peak Voltage Adjustment

5-20. Adjust the ramp peak voltage by adjusting variable resistor A8R3 as follows:

a. Press the MODE key repeatedly on the 5344A front panel until LK/R is displayed. Press the F2 key, then the 1 key, 5 key, and the RESET key to enter diagnostic 15.

b. Connect a 3465 DMM to RAMP OUT test point TP1 on A8 assembly (see *Figure 8-31*).

c. Adjust variable resistor A8R3 for 10.00(±0.01) volts on the DMM.

d. Press the RESET key twice to exit the diagnostic mode.

5-21. Analog Phase Interpolation Adjustment

5-22. To perform the analog phase interpolation adjustment, place the A9 Analog assembly on extender board, part number 05342-60034. Connect the equipment in the setup shown in *Figure 5-1*, and proceed:

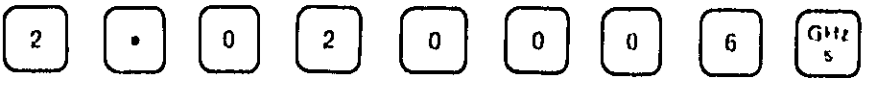
a. Connect the 8556 INPUT connector through a 1 KΩ resistor (part number 0757-0280) to the A9 board at the junction of capacitor C21 and IC U7, pin 6 (connect to the lead of the capacitor).

b. On the 8350A/83595A, press the INSTR PRESET key, then set:

CW FILTER ..... Off
RF ..... On
POWER ..... 0 dBm
CW Frequency ..... 2.02 GHz

c. Set the 5344A to a CW manual lock at 2.025 GHz by pressing the MODE key repeatedly until the CW annunciator lights, then press the following key sequence:

f. Set the 5344A to a CW frequency of 2.020006 GHz by pressing the following key sequence:



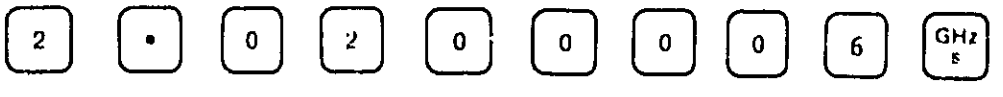
g. Set the spectrum analyzer controls as follows:

BANDWIDTH ..... 100 Hz
SCAN WIDTH ..... 1 kHz/division
INPUT LEVEL ..... -50 dBm
RANGE ..... 0-30 kHz
SCALE dBm/600-ohm
SCAN TIME ..... 0.2 sec/div
LOG REF LEVEL ..... -30 dBm
VIDEO FILTER ..... OFF
SCAN MODE ..... INT
SCAN TRIGGER ..... AUTO

h. Tune the spectrum analyzer to place the 3 kHz peak at the center of the display.

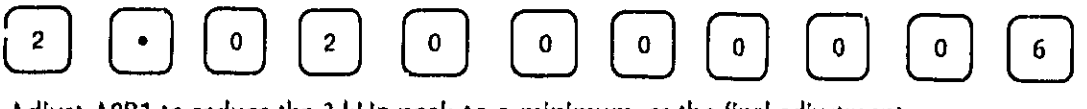
i. Adjust A9R21 to reduce the 3 kHz peak to a minimum.

j. Set the 5344A to a CW frequency of 2.0200006 by pressing the following key sequence.



k. Adjust A9R26 to reduce the 3 kHz peak to a minimum.

l. Set the 5344A to a CW frequency of 2.020000006 GHz by pressing the following key sequence:



m. Adjust A9R1 to reduce the 3 kHz peak to a minimum, as the final adjustment.

n. Remove A9 from the extender board and return to the instrument.

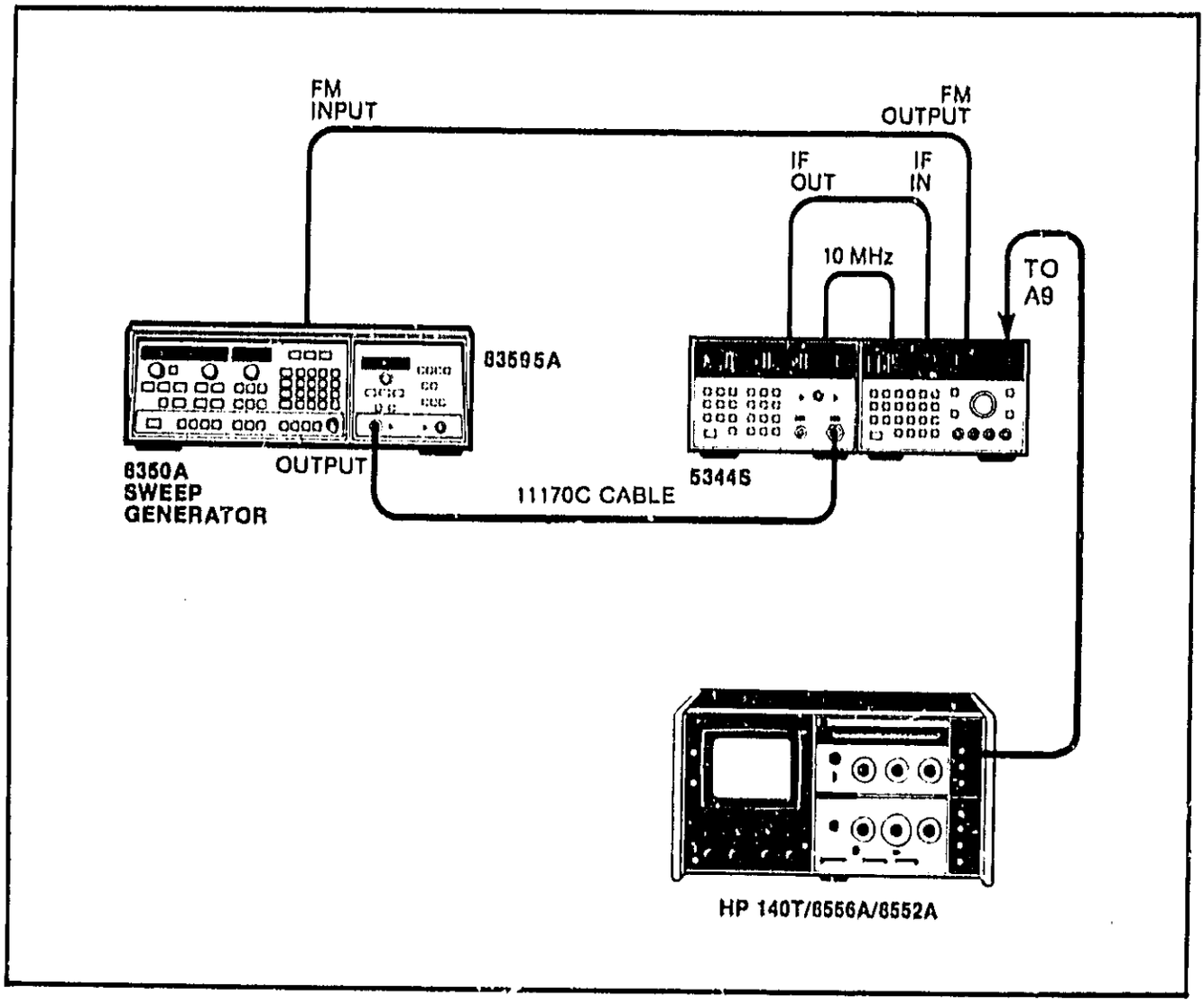


Figure 5-1. Analog Phase Interpolation (API) Adjustment Setup

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION

6-2. This section contains information for ordering replacement parts. *Table 6-1* lists reference designations and abbreviations used in the parts list and throughout the manual. *Table 6-2* lists 5344A parts in alphanumerical order of their reference designators and indicates the description and HP Part Number of each part, together with any applicable notes. A description of the parts list and ordering information is included in this section.

6-3. MANUFACTURERS CODE LIST

6-4. *Table 6-3* contains the names and addresses that correspond to the manufacturers code numbers.

6-5. REPLACEABLE PARTS LIST

6-6. *Table 6-2* is a list of replaceable parts and is organized as follows:

a. Electrical assemblies and their components in alphanumerical order by reference designation for each assembly.

b. Chassis-mounted parts in alphanumerical order by reference designation.

c. Miscellaneous parts.

6-7. The information given for each part consists of the following:

a. The Hewlett-Packard part number.

b. Part number check digit (CD).

c. The total quantity (Qty) in the instrument.

d. The description of the part.

e. A typical manufacturer of the part in a five-digit code.

f. The manufacturer's number of the part.

6-8. The total quantity for each part is given for each assembly — at the first appearance of the part number in the list.

6-9. ORDERING INFORMATION

6-10. To order a part listed in the replaceable parts tables, quote the Hewlett-Packard part number, the check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard office. The check digit will ensure accurate and timely processing of your order.

6-11. To order a part that is not listed in the replaceable parts tables, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Office.

Table 6-1. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	assembly	DL	delay line	K	relay	T	transformer
AT	attenuator, isolator, termination	DS	annunciator, signaling device (audible or visual), lamp, LED	L	coil, inductor	TB	terminal board
B	fan, motor	E	miscellaneous electrical part	M	metre	TC	thermocouple
BT	battery	F	fuse	MP	miscellaneous mechanical part	TP	test point
C	capacitor	FL	filter	P	electrical connector, movable portion, plug	U	integrated circuit, microcircuit
CP	coupler	H	hardware	Q	transistor, SCR, triode thyristor	V	electron tube
CR	diode, diode thyristor, varactor	MY	circulator	R	resistor	VR	voltage regulator, breakdown diode
DC	directional coupler	J	electrical connector, stationary portion, jack	RT	thermistor	W	cable, transmission path, wire
				S	switch	X	socket
						Y	crystal unit, piezo-electric
						Z	tuned cavity, tuned circuit

ABBREVIATIONS

A	ampere	HD	head	NE	neon	SPST	single-pole, single-throw
ac	alternating current	HDW	hardware	NEG	negative	SSB	single sideband
ACCESS	accessory	HF	high frequency	nF	nanofarad	SST	stainless steel
ADJ	adjustment	HG	mercury	NI PL	nickel plate	STL	steel
A/D	analog-to-digital	HI	high	N.O	normally open	SQ	square
AF	audio frequency	HP	Hewlett-Packard	NOM	nominal	SWR	standing-wave ratio
AFC	automatic frequency control	HPF	high pass filter	NORM	normal	SYNC	synchronize
AGC	automatic gain control	HR	hour, used in parts list	NPN	negative-positive-negative	T	timed, slow-blow fuse
AL	aluminum	HV	high voltage	NPO	negative-positive zero, zero temperature coefficient	TA	tantalum
ALC	automatic level control	Hz	hertz	NRFR	not recommended for field replacement	TC	temperature compensating
AM	amplitude modulation	IC	integrated circuit	ns	nanosecond	TD	time delay
AMPL	amplifier	ID	inside diameter	NSR	not separately replaceable	TERM	terminal
APC	automatic phase control	IF	intermediate frequency	nW	nanowatt	TFT	thin-film transistor
ASSY	assembly	IMPG	impregnated	OBD	order by description	TGL	toggle
AUX	auxiliary	in	inch	OD	outside diameter	THD	thread
AVG	average	INCD	incandescent	OH	oval head	THRU	through
AWG	american wire gauge	INCL	include s	OP AMPL	operational amplifier	TI	titanium
BAL	balance	INP	input	OPT	option	TOL	tolerance
BCD	binary coded decimal	INS	insulation	OSC	oscillator	TRIM	trimmer
BD	board	INT	internal	Ox	oxide	TSTR	transistor
BE CU	beryllium copper	kg	kilogram	oz	ounce	TTL	transistor-transistor logic
BFO	beat frequency oscillator	kHz	kilohertz	Ω	ohm	TV	television
BH	binder head	kΩ	kilohm	P	peak, used in parts list	TVI	television interference
BKDN	breakdown	kV	kilovolt	PAM	pulse-amplitude modulation	TWT	traveling wave tube
BP	bandpass	lb	pound	PC	printed circuit	U	micro (10⁻⁶), used in parts list
BPF	bandpass filter	LC	inductance-capacitance	PCM	pulse-code modulation, pulse-count modulation	UF	microfarad, used in parts list
BRS	brass	LED	light emitting diode	PDM	pulse-duration modulation	UHF	ultrahigh frequency
BWO	backward-wave oscillator	LF	low frequency	pF	picofarad	UNREG	unregulated
CAL	calibrate	LG	long	PH BRZ	phosphor bronze	V	volt
ccw	counterclockwise	LH	left hand	PHL	phillips	VA	voltampere
CER	ceramic	LIM	limit	PIN	positive-intrinsic-negative	Vac	volts ac
CHAN	channel	LIN	linear taper, used in parts list	PIV	peak inverse voltage	VAR	variable
cm	centimeter	lin	linear	pk	peak	VCO	voltage-controlled oscillator
CMO	coaxial	LK WASH	lockwasher	PL	phase lock	Vdc	volts dc
COEF	coefficient	LO	low, local oscillator	PLO	phase lock oscillator	VDCW	volts, dc, working, used in parts list
COM	common	LOG	logarithmic taper, used in parts list	PM	phase modulation	V F	volts, filtered
COMP	composition	log	logarithmic	PNP	positive-negative-positive	VFO	variable-frequency oscillator
COMPL	complete	LPF	low pass filter	P/O	part of	VHF	very-high frequency
CONN	connector	LV	low voltage	POLY	polystyrene	Vpk	volts peak
CP	cadmium plate	m	metre, distance	PORC	porcelain	Vp-p	volts peak-to-peak
CRT	cathode-ray tube	mA	milliampere	POS	positive, position, used in parts list	Vrms	volts rms
CTL	complementary transistor logic	MAX	maximum	POSN	position	VSWR	voltage standing wave ratio
CW	continuous wave	MEG	megohm	POT	potentiometer	VTO	voltage-tuned oscillator
cw	clockwise	MET FLM	meg (10⁶), used in parts list	p-p	peak-to-peak	VTVM	vacuum-tube voltmeter
D/A	digital-to-analog	MET OX	metal film	PP	peak-to-peak, used in parts list	V-X	volts, switched
dB	decibel	MF	metal oxide	PPM	pulse-position modulation	W	watt
dBm	decibel referred to 1mW	MFR	medium frequency, microfarad, used in parts list	PREAMPL	preamplifier	W/	with
dc	direct current	mg	manufacturer	PRF	pulse-repetition frequency	WIV	working inverse voltage
deg	degree, temperature interval or difference	MHz	milligram	PRR	pulse repetition rate	WW	wirewound
°	degree, plane angle	mH	megahertz	ps	picosecond	W/O	with out
°C	degree Celsius (centigrade)	mho	millihenry	PT	point	YIG	yttrium-iron garnet
°F	degree Fahrenheit	MIN	conductance	PTM	pulse-time modulation	Zo	characteristic impedance
°K	degree Kelvin	min	minimum	PWM	pulse-width modulation		
DEPC	deposited carbon	′	minute, time	PWV	peak working voltage		
DET	detector	″	minute, plane angle	RC	resistance-capacitance		
diam	diameter	MINAT	miniature	RECT	rectifier		
DIA	diameter, used in parts list	mm	millimetre	REF	reference		
DIFF AMPL	differential amplifier	MOD	modulator	REG	regulated		
div	division	MOM	momentary	REPL	replaceable		
DPDT	double-pole, double-throw	MOS	metal-oxide semiconductor	RF	radio frequency		
DR	drive	ms	millisecond	RFI	radio frequency interference		
DSB	double sideband	MTG	mounting	RH	round head, right hand		
DTL	diode transistor logic	MTR	meter (indicating device)	RLC	resistance-inductance-capacitance		
DVM	digital voltmeter	mV	millivolt	RMO	rack mount only		
ECL	emitter coupled logic	mVac	millivolt, ac	rms	root-mean-square		
EMF	electromotive force	mVdc	millivolt, dc	RND	round		
EDP	electronic data processing	mVpk	millivolt, peak	ROM	read-only memory		
ELECT	electrolytic	mVp-p	millivolt, peak-to-peak	R&P	rack and panel		
ENCAP	encapsulated	mVrms	millivolt, rms	RWV	reverse working voltage		
EXT	external	mW	milliwatt	S	scattering parameter		
F	farad	MUX	multiplex	s	second, time		
FET	field-effect transistor	MY	mylar	″	second, plane angle		
F/F	flip-flop	μA	microampere	S-B	slow-blow fuse, used in parts list		
FH	flat head	μF	microfarad	SCR	silicon controlled rectifier, screw		
FOL H	fillister head	μH	microhenry	SE	selenium		
FM	frequency modulation	μmho	micromho	SECT	sections		
FP	front panel	μs	microsecond	SEMICON	semiconductor		
FREQ	frequency	μV	microvolt	SHF	superhigh frequency		
FXD	fixed	μVac	microvolt, ac	SI	silicon		
g	gram	μVdc	microvolt, dc	SIL	silver		
GE	germanium	μVpk	microvolt, peak	SL	slide		
GHz	gigahertz	μVp-p	microvolt, peak-to-peak	SNR	signal-to-noise ratio		
GL	glass	μVrms	microvolt, rms	SPDT	single-pole, double-throw		
GND	ground, ed	μW	microwatt	SPG	spring		
H	henry	nA	nanoampere	SR	split ring		
h	hour	NC	no connection				
HET	heterodyne	N/C	normally closed				
HEX	hexagonal						

NOTE

All abbreviations in the parts list will be in upper case.

MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	10^{12}
G	giga	10^{9}
M	mega	10^{6}
k	kilo	10^{3}
da	deka	10^{1}
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

6-12. DIRECT MAIL ORDER SYSTEM

6-13. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices — to provide these advantages, a check or money order must accompany each order.

6-14. Mail order forms and specific ordering information is available through your HP office Addresses and phone numbers are located at the back of this manual.

6-15. CABINET PARTS

6-16. Refer to *Figure 6-1* for identification of mechanical cabinet parts.

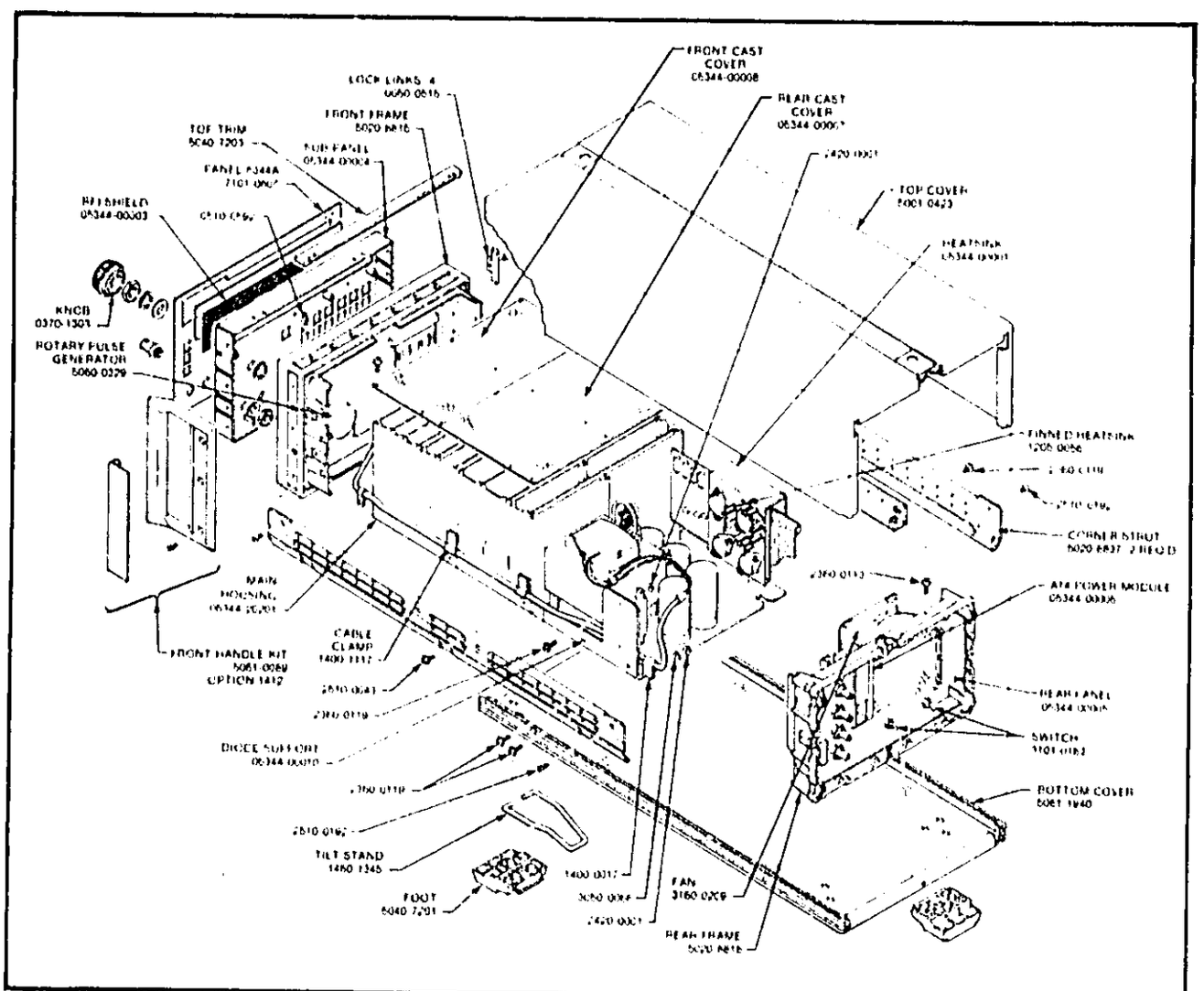


Figure 6-1. 5344A Mechanical Parts, Exploded View

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	05344-60001	0	1	KEYBOARD/DISPLAY ASSEMBLY (SERIES 2140)	28480	05344-60001
A1C1	0160-3879	7	1	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C2	0180-2929	0	1	CAPACITOR-FXD 600UF+-10% 10VDC TA	28480	0180-2929
A1DS1	1990-0656	0	14	LED LIGHT BAR MODULE LOW INT-3MCD	28480	HLMP-2300
A1DS2	1990-0656	0		LED LIGHT BAR MODULE LOW INT-3MCD	28480	HLMP-2300
A1DS3	1990-0656	0		LED LIGHT BAR MODULE LOW INT-3MCD	28480	HLMP-2300
A1DS4	1990-0656	0		LED LIGHT BAR MODULE LOW INT-3MCD	28480	HLMP-2300
A1DS5	1990-0670	0	6	LED LAMP LOW INT-1MCD IF=20MA MAX BVR=5V	28480	1990-0670
A1DS6	1990-0670	0		LED LAMP LOW INT-1MCD IF=20MA MAX BVR=5V	28480	1990-0670
A1DS7	1990-0656	0		LED LIGHT BAR MODULE LOW INT-3MCD	28480	HLMP-2300
A1DS8	1990-0656	0		LED LIGHT BAR MODULE LOW INT-3MCD	28480	HLMP-2300
A1DS9	1990-0670	0		LED LAMP LOW INT-1MCD IF=20MA MAX BVR=5V	28480	1990-0670
A1DS10	1990-0670	0		LED LAMP LOW INT-1MCD IF=20MA MAX BVR=5V	28480	1990-0670
A1DS11	1990-0670	0		LED LAMP LOW INT-1MCD IF=20MA MAX BVR=5V	28480	1990-0670
A1DS12	05344-20702	2	1	DISPLAY MODULE	28480	05344-20702
A1DS13	1990-0656	0		LED LIGHT BAR MODULE LOW INT-3MCD	28480	HLMP-2300
A1DS14	1990-0659			LED LIGHT BAR MODULE LOW INT-2MCD	28480	HLMP-2350
A1DS15	1990-0656	0		LED LIGHT BAR MODULE LOW INT-3MCD	28480	HLMP-2300
A1DS16	1990-0656	0		LED LIGHT BAR MODULE LOW INT-3MCD	28480	HLMP-2300
A1DS17	1990-0670	0		LED LAMP LOW INT-1MCD IF=20MA MAX BVR=5V	28480	1990-0670
A1DS18	1990-0659			LED LIGHT BAR MODULE LOW INT-2MCD	28480	HLMP-2350
A1DS19	1990-0659	5		LED LIGHT BAR MODULE LOW INT-2MCD	28480	HLMP-2350
A1DS20	1990-0659	5		LED LIGHT BAR MODULE LOW INT-2MCD	28480	HLMP-2350
A1DS21	1990-0659	5		LED LIGHT BAR MODULE LOW INT-2MCD	28480	HLMP-2350
A1DS22	1990-0656	0		LED LIGHT BAR MODULE LOW INT-3MCD	28480	HLMP-2300
A1DS23	1990-0656	0		LED LIGHT BAR MODULE LOW INT-3MCD	28480	HLMP-2300
A1DS24	1990-0656	0		LED LIGHT BAR MODULE LOW INT-3MCD	28480	HLMP-2300
A1DS25	1990-0656	0		LED LIGHT BAR MODULE LOW INT-3MCD	28480	HLMP-2300
A1DS26	1990-0670	0		LED LAMP LOW INT-1MCD IF=20MA MAX BVR=5V	28480	1990-0670
A1DS27	1990-0670	0		LED LAMP LOW INT-1MCD IF=20MA MAX BVR=5V	28480	1990-0670
A1J1	1251-0600	0	4	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A1J2	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A1J3	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A1J4	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A1R1	1810-0279	5	1	NETWORK-RES 10-SIP 4.7K OHM X 9	01121	210A472
A1R2	0757-0424	5	1	RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
A1R3	0698-3157	0	1	RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A1R4	1810-[illegible]	0	1	NETWORK-RES [illegible] 330.0 OHM X [illegible]	01121	207A331
A1R5	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
A1S1	5060-9436	7	26	PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S2	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S3	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S4	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S5	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S6	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S7	5060-9436			PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S8	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S9	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S10	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S11	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S12	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S13	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S14	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S15	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S16	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S17	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S18	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S19	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S20	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S21	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S22	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S23	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S24	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S25	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S26	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1U1	1820-1012	1	1	IC DRVR TTL OR DUAL 2-INP	01295	SN75451BP
A1U2	1820-1012	1		IC DRVR TTL OR DUAL 2-INP	01295	SN75451BP
A1U3	1820-1012	1		IC DRVR TTL OR DUAL 2-INP	01295	SN75451BP
A1U4	1820-1012	1		IC DRVR TTL OR DUAL 2-INP	01295	SN75451BP
A1U5	1820-1012	1		IC DRVR TTL OR DUAL 2-INP	01295	SN75451BP

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U6	1826-0655	4	1	IC 10 DIP-P PKG	27014	LM3914N
A1U7	1820-1416	1		IC DRVR TTL OR DUAL 2-INP	01295	SN75453BP
A1U8	1820-1416	1		IC DRVR TTL OR DUAL 2-INP	01295	SN75453BP
A1U9	1820-1429	0	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS155N
A1U10	1820-1416	1		IC DRVR TTL OR DUAL 2-INP	01295	SN75453BP
A1W1	8120-3437	7	1	CABLE ASSEMBLY DISPLAY	28480	8120-3437
A1XDS1-12	1200-0949	1	2	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0949
				A1 MISCELLANEOUS PARTS		
	5041-0309	5	2	KEY CAP-QUARTER (PTY)	28480	5041-0309
	5041-0310	6	5	KEY CAP-QUARTER (PUT GEP)	28480	5041-0310
	5041-0142	6	1	KEY CAP-QUARTER (SKJ)	28480	5041-0142
	5041-0351	7	4	KEY CAP-QUARTER (L SUKY)	28480	5041-0351
	5041-0704	0	1	KEY CAP- 5	28480	5041-0704
	5041-0705	1	2	KEY CAP- 6 OR 9	28480	5041-0705
	5041-0706	2	1	KEY CAP- 7	28480	5041-0706
	5041-0707	3	1	KEY CAP- 8	28480	5041-0707
	5041-0708	4	1	KEY CAP- 0	28480	5041-0708
	5041-0709	5	1	KEY CAP- .	28480	5041-0709
	5041-0802	3	1	KEY CAP- 1	28480	5041-0802
	5041-0803	4	1	KEY CAP- 2	28480	5041-0803
	5041-0804	5	1	KEY CAP- 3	28480	5041-0804
	5041-0805	6	1	KEY CAP- 4	28480	5041-0805
	5041-1045	6	2	KEY CAP (SPL)	28480	5041-1045
	5041-1552	6	1	KEY CAP- (GRAY)	28480	5041-1552
	5041-1553	7	1	KEY CAP (GRAY)	28480	5041-1553
	1200-0525	1	10	SOCKET-STRP 4-CONT SIP DIP-SLDR	28480	1200-0525
	1200-0639	0	1	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
	1200-0748	4	5	SOCKET-STRP 8-CONT DIP DIP-SLDR	28480	1200-0748

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A-	05342-60029	A	1	[illegible]	[illegible]	05342-60029
A-J1 A-J2	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
A-MP1 A-MP2 A-MP3	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
A-S1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
A-W1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3	05344-60003	0	1	KEYBOARD/DISPLAY INTERFACE ASSEMBLY (SERIES 2140)	28480	05344-60003
A3C1	0160-3879	7	14	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C2	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C3	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C6	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C7	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C8	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C9	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C10	0180-2929	8	1	CAPACITOR-FXD 68UF+-10% 10VDC TA	28480	0180-2929
A3C11	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C12	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C13	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C14	0160-0575	4	1	CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C15	0160-3878	6	1	CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A3C16	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C17	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3L1	9100-1788	6	1	CHOKE-WIDE BAND ZMAX=680 OHM@ 180 MHZ	02114	VK200 20/4B
A3Q1	1858-0010	2	2	TRANSISTOR ARRAY (4) MPQ2906	04713	MPQ2906
A3Q2	1858-0010	2		TRANSISTOR ARRAY (4) MPQ2906	04713	MPQ2906
A3Q3	1853-0281	9	2	TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A3Q4	1853-0281	9		TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A3R1	0698-4037	0	8	RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A3R2	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A3R3	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A3R4	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A3R5	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A3R6	0698-3441	8	2	RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A3R7	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A3R8	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A3R9	1810-0225	1	1	NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
A3R10	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A3R11	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A3R12	1810-0206	8	1	NETWORK-RES 16-DIP22K OHM X 8	01121	316B223
A3R13	0698-0085	0	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
A3R14	0698-8961	7	1	RESISTOR 909K 1% .125W F TC=0+-100	28480	0698-8961
A3TP1	0360-1682	0	9	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A3TP2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A3TP3	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A3TP4	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A3TP5	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A3TP6	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A3TP7	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A3TP8	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A3TP9	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A3U1	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U2	1820-0174	0	1	IC INV TTL HEX	01295	SN7404N
A3U3	1820-2150	6	1	IC INTERFACE ACCESS NMOS	34649	P8279-5
A3U4	1820-2075	4	1	IC MISC TTL LS	01295	SN74LS245N
A3U5	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A3U6	1820-1730	6	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U7	1820-1449	5	1	IC LCH TTL LS QUAD	01295	SN74LS279N
A3U8	1820-2024	3	1	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U9	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A3U10	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A3U11	1820-1207	2	1	IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
A3U12	1820-1210	7	1	IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
A3U13	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A3U14	1826-0180	6	1	IC TIMER TTL MONO/ASTBL	01295	NE555P
A3U15	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A3W1	1258-0124	7	1	PIN PROGRAMMING JUMPER 1 CONTACT	91506	8136-475G1
A3XU1	1200-0552	4	1	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0552
A3XW1	1200-0425	0	2	CONNECTOR-SGL CONT SKT .032-IN-BSC-SZ	28480	1200-0425
A3XW2	1200-0425	0		CONNECTOR-SGL CONT SKT .032-IN-BSC-SZ	28480	1200-0425
				A3 MISCELLANEOUS PARTS		
	5000-9043	6	1	PIN:P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6852	3	1	PC EXTRACTOR (ORANGE)	28480	5040-6852

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4	05344-60004	1	1	HPIB INTERFACE ASSEMBLY (SERIES 2052)	28480	05344-60004
A4C1	0160-4640	2	1	CAPACITOR-FXD 1UF +-10% 100VDC	28480	0160-4640
A4C2	0160-3405	5	1	CAPACITOR-FXD 2UF +-10% 50VDC MET POLYE	28480	0160-3405
A4C3	0160-4557	0	1	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A4C4	0160-4554	7	4	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A4C5	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A4C6	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A4C7	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A4C8	0160-4031	1	1	CAPACITOR-FXD 4700PF +-10% 100VDC CER	28480	0160-4031
A4C9	0180-0116	1	2	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A4C10	0180-0228	6	1	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A4C11	0160-3879	7	8	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A4C12	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A4C13	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A4C14	0180-2929	8	1	CAPACITOR-FXD 68UF+-10% 10VDC TA	28480	0180-2929
A4C15	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A4C16	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A4C17	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A4C18	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A4C19	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A4C20	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A4CR1	1901-0376	6	4	DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A4CR2	1901-0376	6		DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A4CR3	1901-0376	6		DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A4CR4	1901-0050	3	9	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4CR5	1901-0376	6		DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A4CR6	1901-0044	5	2	DIODE-SWITCHING 50V 50MA 4NS	28480	1901-0044
A4CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4CR9	1901-0044	5		DIODE-SWITCHING 50V 50MA 4NS	28480	1901-0044
A4CR10	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4CR11	1901-0518	8	2	DIODE-SM SIG SCHOTTKY	28480	1901-0518
A4CR12	1901-0518	8		DIODE-SM SIG SCHOTTKY	28480	1901-0518
A4CR13	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4CR14	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4CR15	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4L1	9100-1788	6	1	CHOKE-WIDE BAND ZMAX=680 OHM@180 MHZ	02114	VK200 20/4B
A4Q1	1854-0215	1	6	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A4Q2	1853-0036	2	4	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A4Q3	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A4Q4	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A4Q5	1855-0420	2	4	TRANSISTOR J-FET 2N4391 N-CHAN D-MODE	01295	2N4391
A4Q6	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A4Q7	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A4Q8	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A4Q9	1855-0420	2		TRANSISTOR J-FET 2N4391 N-CHAN D-MODE	01295	2N4391
A4Q10	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A4Q11	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A4Q12	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A4Q13	1855-0420	2		TRANSISTOR J-FET 2N4391 N-CHAN D-MODE	01295	2N4391
A4Q14	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A4Q15	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A4Q16	1855-0420	2		TRANSISTOR J-FET 2N4391 N-CHAN D-MODE	01295	2N4391
A4R1	0698-3442	9	1	RESISTOR 237 1% .125W F TC=0+-100	24546	C4-1/8-T0-237R-F
A4R2	0698-3452	1	4	RESISTOR 147K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1473-F
A4R3	0698-3160	8	2	RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
A4R4	0699-0069	2	1	RESISTOR 2.15M 1% .125W F TC=0+-100	28480	0699-0069
A4R5	0757-0427	0	6	RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A4R6	0698-3136	8	2	RESISTOR 17.8K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1782-F
A4R7	0757-0427	0		RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A4R8	0757-0443	0	1	RESISTOR 11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1102-F
A4R9	0757-0441	8	1	RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A4R10	0698-3160	8		RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
A4R11	0698-3155	1	1	RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A4R12	0698-3136	8		RESISTOR 17.8K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1782-F
A4R13	0698-3452	1		RESISTOR 147K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1473-F
A4R14	0698-0082	7	1	RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
A4R15	0698-3452	1		RESISTOR 147K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1473-F
A4R16	0698-3154	0	1	RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A4R17	0698-6264	9	4	RESISTOR 400 .5% .125W F TC=0+-100	24546	C4-1/8-T0-400R-D
A4R18	0698-0084	9	1	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A4R19	0757-0465	6	5	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A4R20	0698-6264	9		RESISTOR 400 .5% .125W F TC=0+-100	24546	C4-1/8-T0-400R-D

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4R21	0757-0442	9	6	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R22	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R23	0698-5052	5	2	RESISTOR 500 1% .125W F TC=0+-100	24546	C4-1/8-T0-500R-F
A4R24	0757-0420	3	1	RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A4R25	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A4R26	0698-3450	1		RESISTOR 42.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4222-F
A4R27	0757-0427	0		RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A4R28	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R29	0698-3162	0	1	RESISTOR 46.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4642-F
A4R30	0698-6264	5		RESISTOR 400 .5% .125W F TC=0+-100	24546	C4-1/8-T0-400R-D
A4R31	0757-0427	0		RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A4R32	0698-6264	5		RESISTOR 400 .5% .125W F TC=0+-100	24546	C4-1/8-T0-400R-D
A4R33	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A4R34	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A4R35	0698-3150	6	1	RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
A4R36	0757-0472	5	1	RESISTOR 200K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2003-F
A4R37	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R38	0757-0427	0		RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A4R39	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A4R40	0757-0199	3	4	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A4R41	0757-0427	0		RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A4R42	0698-5052	5		RESISTOR 500 1% .125W F TC=0+-100	24546	C4-1/8-T0-500R-F
A4R43	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R44	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R45	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A4R46	1810-0269	3	1	NETWORK-RES 9-SIP10.0K OHM X 8	28480	1810-0269
A4R47	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A4R48	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A4R49	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A4TP1	0360-1682	0	6	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A4TP2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A4TP3	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A4TP4	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A4TP5	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A4TP6	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A4U1	1826-0521	3	1	IC OP AMP LOW-BIAS-H-IMPD DUAL 8-DIP-P	01295	TL072CP
A4U2	1826-0315	3	1	IC OP AMP GP QUAD 14-DIP-P PKG	27014	LM348N
A4U3	1820-2540	6	1	IC-TI TMS 9914	28480	1820-2540
A4U4	1820-2024	3	1	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A4U5	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A4U6	1820-2403	8	1	IC XCVR TTL LS BUS OCTL	01295	SN75160N
A4U7	1820-2405	0	1	IC XCVR TTL LS BUS OCTL	01295	SN75161N
A4U8	1820-1202	2	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A4U9	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
				A4 MISCELLANEOUS PARTS		
	5000-9043	6	1	PIN:P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6848	2	1	EXTRACTOR YELLOW	28480	5040-6848
	1200-0552	4	1	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0552

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5	05344-60005	[illegible]	1	[illegible] MEMORY/DECODER ASSEMBLY (SERIES [illegible])	28480	05344-60005
A5C1	0160-3879	7	11	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C2	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C3	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C5	0180-2929	0	1	CAPACITOR-FXD [illegible] +-10% 10VDC TA	28480	0180-2929
A5C6	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C7	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C8	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C9	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C10	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C11	0160-4547	8	2	CAPACITOR-FXD 150PF +-5% 200VDC CER	28480	0160-4547
A5C12	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C13	0160-4547	8		CAPACITOR-FXD 150PF +-5% 200VDC CER	28480	0160-4547
A5C14	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5L1	9100-1788	6	1	CHOKE-WIDE BAND ZMAX=680 OHM @ 180 MHZ	02114	VK200 20/4B
A5R1	0757-0199	3	3	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A5R2	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A5R3	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A5TP1	0360-1682	0	9	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A5TP2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A5TP3	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A5TP4	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A5TP5	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A5TP6	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A5TP7	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A5TP8	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A5TP9	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A5U1	1818-1213	5	1	IC NMOS [illegible] ROM	[illegible]	[illegible]
A5U2	1820-1245	0	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS155N
A5U3	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A5U5	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A5U7	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A5U9	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A5U10	1820-[illegible]	[illegible]	1	IC [illegible] TTL LS COM CLEAR [illegible]	01295	[illegible]
A5U11	1820-1502	[illegible]	1	IC [illegible] TTL LS COM CLEAR [illegible]	01295	[illegible]
A5U12	1820-[illegible]	[illegible]		IC [illegible] TTL LS COM CLEAR [illegible]	01295	[illegible]
A5U13	1820-[illegible]	4	1	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	[illegible]
A5U14	1820-[illegible]	[illegible]		IC [illegible] TTL LS COM CLEAR [illegible]	[illegible]	[illegible]
A5W1	1258-0124	7	2	PIN-PROGRAMMING JUMPER [illegible] CONTACT	[illegible]	[illegible]
A5W2	1258-0124	7		PIN-PROGRAMMING JUMPER [illegible] CONTACT	[illegible]	[illegible]
A5XU1	1200-0541	1	[illegible]	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A5XU[illegible]	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
				A5 MISCELLANEOUS PARTS		
	1251-[illegible]	0	4	CONNECTOR [illegible]	28480	1251-[illegible]
	5000-9043	6	1	PIN:P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-[illegible]	[illegible]	1	EXTRACTOR GREEN	28480	5040-[illegible]

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	[illegible]	1	1	MAIN [illegible]	[illegible]	[illegible]
A1C1	0160-[illegible]	7	5	CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C2	0160-[illegible]	6	14	CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C3	0160-[illegible]	6		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C4	0160-[illegible]	6		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C5	0160-[illegible]	6	2	CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C6	0160-[illegible]	7		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C7	0160-[illegible]	6		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C8	0160-[illegible]	0		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C9	0160-[illegible]	6		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C10	0160-[illegible]	6		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C11	0160-[illegible]	7	11	CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C12	0160-[illegible]	7		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C13	0160-[illegible]	6		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C14	0160-[illegible]	6		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C15	0160-[illegible]	6		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C16	0160-[illegible]	6		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C17	0160-[illegible]	6		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C18	0160-[illegible]	7		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C19	0160-[illegible]	7		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C20	0160-[illegible]	3	.1	CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C21	0160-[illegible]	3	.1	CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C22	0160-[illegible]	6		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C23	0160-[illegible]	6		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C24	0160-[illegible]	6		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C25	0160-[illegible]	6		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C26	0160-[illegible]	0	4	CAPACITOR-FXD [illegible]	[illegible]	[illegible]
A1C27	0160-[illegible]	0		CAPACITOR-FXD [illegible]	[illegible]	[illegible]
A1C28	0160-[illegible]	0		CAPACITOR-FXD [illegible]	[illegible]	[illegible]
A1C29	0160-[illegible]	6		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C30	0160-[illegible]	3		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C31	0160-[illegible]	0		CAPACITOR-FXD [illegible]	[illegible]	[illegible]
A1C32	0160-[illegible]	7		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C33	0160-[illegible]	7		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C34	0180-[illegible]	3	.1	CAPACITOR-FXD [illegible]	[illegible]	[illegible]
A1CR1	0160-[illegible]	7		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C35	0160-[illegible]	3		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C36	0160-[illegible]	7	1	CAPACITOR-FXD [illegible]	[illegible]	[illegible]
A1C37	0160-[illegible]	7	.1	CAPACITOR-FXD [illegible]	[illegible]	[illegible]
A1C38	0160-[illegible]	6	1	CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C39	0160-[illegible]	7		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C40	0160-[illegible]	7		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C41	0160-[illegible]	1		CAPACITOR-FXD [illegible]	[illegible]	[illegible]
A1C42	0160-[illegible]	7		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C43	0180-[illegible]	1	.1	CAPACITOR-FXD [illegible]	[illegible]	[illegible]
A1C44	0160-[illegible]	0	1	CAPACITOR-FXD [illegible]	[illegible]	[illegible]
A1C45	0160-[illegible]	6	1	CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C46	0160-[illegible]	7		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C47	0160-[illegible]	7		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C48	0160-[illegible]	7	1	CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C49	0160-[illegible]	1		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C50	0160-[illegible]	7		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1C51	0160-[illegible]	4		CAPACITOR-FXD [illegible]	[illegible]	0160-[illegible]
A1CR1	1901-[illegible]	1	6	DIODE-SWITCHING 100V 200MA [illegible]	[illegible]	[illegible]
A1CR2	1901-[illegible]	3		DIODE-SWITCHING 80V 200MA [illegible]	[illegible]	1901-[illegible]
A1CR3	1901-[illegible]	0		DIODE-[illegible]	[illegible]	1901-[illegible]
A1CR4	1901-[illegible]	3		DIODE-SWITCHING 80V 200MA [illegible]	[illegible]	1901-[illegible]
A1CR5	1901-[illegible]	3		DIODE-SWITCHING 80V 200MA [illegible]	[illegible]	1901-[illegible]
A1CR6	1902-[illegible]	0	.1	DIODE-ZNR 5.6V 5% DO-35 PD=.4W TC=+.043%	[illegible]	1902-[illegible]
A1CR7	1902-[illegible]	0		DIODE-ZNR 5.6V 5% DO-35 PD=.4W TC=+.043%	[illegible]	1902-[illegible]
A1J1	[illegible]	5	1	[illegible]	[illegible]	[illegible]
A1K1	0490-[illegible]	5		RELAY-REED 1A 500MA [illegible]	[illegible]	0490-[illegible]
A1K2	0490-[illegible]	5		RELAY-REED 1A 500MA [illegible]	[illegible]	0490-[illegible]
A1L1	9100-[illegible]	3	.1	INDUCTOR-RF CH-MLD 100UH [illegible]	[illegible]	9100-[illegible]
A1L2	9100-[illegible]	4		INDUCTOR-RF CH-MLD 100UH [illegible]	[illegible]	9100-[illegible]
A1L3	9100-[illegible]	3	1	INDUCTOR-RF CH-MLD 10UH [illegible]	[illegible]	9100-[illegible]
A1Q1	1854-[illegible]	7	4	TRANSISTOR NPN [illegible]	[illegible]	[illegible]
A1Q2	1853-[illegible]	0		TRANSISTOR PNP [illegible]	[illegible]	1853-[illegible]
A1Q3	1854-[illegible]	7		TRANSISTOR NPN [illegible]	[illegible]	[illegible]
A1Q4	1854-[illegible]			TRANSISTOR NPN [illegible]	[illegible]	[illegible]
A1Q5	1854-[illegible]	7		TRANSISTOR NPN [illegible]	[illegible]	[illegible]

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6Q6	1854-0058	6	1	TRANSISTOR NPN SI TO-39 PD=1W FT=[illegible]	28480	1854-0058
A6Q7	1853-0045	1	1	TRANSISTOR PNP SI TO-39 PD=1W FT=[illegible]	[illegible]	2N4036
A6R1	0698-3437	2	2	RESISTOR 133 1% .125W F TC=0+-100	24546	C4-1/8-T0-133R-F
A6R2	0698-6364	5	2	RESISTOR 400 .5% .125W F TC=0+-100	24546	C4-1/8-T0-400R-D
A6R3	0757-0401	0	6	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A6R4	0757-0180	2	4	RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A6R5	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A6R6	0757-0180	2		RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A6R7	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A6R8	0757-0180	2		RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A6R9	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A6R10	0757-0416	7	5	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A6R11	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A6R12	0757-0438	3	2	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A6R13	0698-3152	8	2	RESISTOR 3.48K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3481-F
A6R14	0698-3150	6	4	RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
A6R15	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A6R16	0698-3152	8		RESISTOR 3.48K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3481-F
A6R17	0698-3150	6		RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
A6R18	0757-0400	9	4	RESISTOR 90.9 1% .125W F TC=0+-100	24546	C4-1/8-T0-90R9-F
A6R19	0698-3150	6		RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
A6R20	0757-0400	9		RESISTOR 90.9 1% .125W F TC=0+-100	24546	C4-1/8-T0-90R9-F
A6R21	0757-0400	9		RESISTOR 90.9 1% .125W F TC=0+-100	24546	C4-1/8-T0-90R9-F
A6R22	0757-0180	2		RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A6R23	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A6R24	0757-0280	3	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R25	0698-3155	1	12	RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A6R26	0698-6364	9		RESISTOR 400 .5% .125W F TC=0+-100	24546	C4-1/8-T0-400R-D
A6R27	0698-3437	2		RESISTOR 133 1% .125W F TC=0+-100	24546	C4-1/8-T0-133R-F
A6R28	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A6R29	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A6R30	0757-0462	3	4	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
A6R31	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A6R32	0757-0400	9		RESISTOR 90.9 1% .125W F TC=0+-100	24546	C4-1/8-T0-90R9-F
A6R33	0698-0085	0	7	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
A6R34	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R35	0698-0085	0		RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
A6R36	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A6R37	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A6R38	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A6R39	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A6R40	0757-0442	9	4	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R41	0698-3154	0	1	RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A6R42	0757-0462	3		RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
A6R43	0757-0462	3		RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
A6R44	0757-0462	3		RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
A6R45	0757-0465	6	5	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A6R46	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A6R47	0757-0283	6	3	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A6R48	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A6R49	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A6R50	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A6R51	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A6R52	0757-1094	9	1	RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A6R53	0757-0427	0	2	RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A6R54	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R55	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R56	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R57	0698-0085	0		RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
A6R58	0698-0085	0		RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
A6R59	0698-4009	6	1	RESISTOR 50K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5002-F
A6R60	0698-0085	0		RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
A6R61	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A6R62	0757-0427	0		RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A6R63	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A6R64	0698-0085	0		RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
A6R65	0698-3150	6		RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
A6R66	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A6R67	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A6R68	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A6R69	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A6R70	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A6R71	0757-0417	8	1	RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-T0-562R-F
A6R72	0757-0439	4	2	RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A6R73	0757-0417	8		RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-T0-562R-F
A6R74	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A6R75	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6R74	0757-0804	7	1	RESISTOR 200 1% .5W F TC=0+-100	28480	0757-0804
A6R75	0757-0412	6		RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-T0-562R-F
A6R76	0757-0178	0	2	RESISTOR 100 1% .25W F TC=0+-100	24546	C5-1/4-T0-101-F
A6R79	0757-0178	0		RESISTOR 100 1% .25W F TC=0+-100	24546	C5-1/4-T0-101-F
A6R80	0757-0439	4		RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A6TP1	0360-1682	0	11	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A6TP2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A6TP3	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A6TP4	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A6TP5	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A6TP6	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A6TP7	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A6TP8	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A6TP9	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A6TP10	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A6TP11	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A6U1	1820-1225	4	1	IC FF ECL D-M/S DUAL	04713	MC10231P
A6U2	1826-0372	2	4	IC 6 GHZ LIMITER AMP	28480	1826-0372
A6U3	1826-0372	2		IC 6 GHZ LIMITER AMP	28480	1826-0372
A6U4	1826-0372	2		IC 6 GHZ LIMITER AMP	28480	1826-0372
A6U5	1820-0802	1	1	IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A6U6	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A6U7	1820-1344	0	1	IC PL LOOP 14-DIP-C PKG	04713	MC12040L
A6U8	1826-0372	2		IC 6 GHZ LIMITER AMP	28480	1826-0372
A6U9	1826-0040	9	1	IC SPCL ZNR 14-DIP-C PKG	24355	AD561
A6U10	1826-0622	4	1	IC OP AMP LOW-BIAS-H-IMPD QUAD 14-DIP-P	01295	TL074CN
A6U11	1826-0?	4	1	IC D/A 16-DIP-P PKG	24355	AD7524JN
A6U12	1826-07??	7	1	IC OP AMP LOW-NOISE 8-DIP-P PKG	18324	NE5534AN
A6W1	8159-0005	0	5	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
A6W2	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
A6W3	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
A6W4	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
A6W5	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
				A6 MISCELLANEOUS PARTS		
	1205-0011	0	2	HEAT SINK TO-5/TO-39-CS	28480	1205-0011
	5000-9043	6	1	PIN:P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6149	0	1	EXTRACTOR, P.C. BOARD BLUE	28480	5040-6149
	2110-0269	0	2	FUSEHOLDER-CLIP TYPE .250-FUSE	28480	2110-0269

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7	05344-60007	4	1	SYN ASSEMBLY (SERIES 2140)	28480	05344-60007
A7C1	0180-0228	6	1	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A7C2	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A7C3	0160-4557	0	4	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A7C4	0160-4554	7	1	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A7C5	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A7C6	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A7C7	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A7C8	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A7C9	0180-0376	5	1	CAPACITOR-FXD .47UF+-10% 35VDC TA	56289	150D474X9035A2
A7C10	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A7C11	0160-0945	2	1	CAPACITOR-FXD 910PF +-5% 100VDC MICA	28480	0160-0945
A7C12	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A7C13	0160-2204	0	5	CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A7C14	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A7C15	0160-2204	0		CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A7C16	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A7C17	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A7C18	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A7C19	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A7C20	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A7C21	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A7C22	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A7C23	0160-2204	0		CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A7CR1	0122-0059	9	2	DIODE-VVC DO-7 Q>200 MIN	28480	0122-0059
A7CR2	0122-0059	9		DIODE-VVC DO-7 Q>200 MIN	28480	0122-0059
A7CR3	1901-0518	8	1	DIODE-SM SIG SCHOTTKY	28480	1901-0518
A7CR4	1901-0050	3	5	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A7CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A7CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A7CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A7CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A7DS1	1990-0467	7	1	LED-LAMP LUM-INT=1MCD IF=50MA-MAX BVR=5V	28480	5082-4584
A7L1	9140-0356	0	1	COIL-VAR 58.4NH-61.6NH Q=140 FC MTG	28480	9140-0356
A7L2	9100-1139	5	1	INDUCTOR [illegible]	28480	9100-1139
A7L3	9100-0537	3	1	INDUCTOR (MISC ITEM)	28480	9100-0537
A7Q1	1854-0296	0	4	TRANSISTOR NPN SI TO-92 PD=310MW	28480	1854-0296
A7Q2	1854-0296	0		TRANSISTOR NPN SI TO-92 PD=310MW	28480	1854-0296
A7Q3	1854-0215	1	1	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A7Q4	1854-0296	0		TRANSISTOR NPN SI TO-92 PD=310MW	28480	1854-0296
A7Q5	1853-0089	5	1	TRANSISTOR PNP 2N4917 SI PD=200MW	04713	2N4917
A7Q6	1854-0296	0		TRANSISTOR NPN SI TO-92 PD=310MW	28480	1854-0296
A7R1	0757-0279	0	7	RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A7R2	0757-0419	0	1	RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A7R3	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A7R4	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A7R5	0698-3440	7	1	RESISTOR 196 1% .125W F TC=0+-100	24546	C4-1/8-T0-196R-F
A7R6	0757-0438	3	4	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A7R7	0757-0442	9	3	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A7R8	0698-3155	1	1	RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A7R9	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A7R10	0757-0290	5	1	RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
A7R11	0757-0289	2	1	RESISTOR 13.3K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-1332-F
A7R12	0757-0180	2	2	RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A7R13	0757-0280	3	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A7R14	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A7R15	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A7R16	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A7R17	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A7R18	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A7R19	0698-3446	3	4	RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-T0-383R-F
A7R20	0698-3446	3		RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-T0-383R-F
A7R21	0698-3162	0	1	RESISTOR 46.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4642-F
A7R22	0698-4037	0	2	RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A7R23	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A7R24	0757-0288	1	1	RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-9091-F
A7R25	0757-0180	2		RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A7R26	0698-3446	3		RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-T0-383R-F
A7R27	0757-0439	4	1	RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A7R28	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A7R29	0698-3132	4	1	RESISTOR 261 1% .125W F TC=0+-100	24546	C4-1/8-T0-2610-F
A7R30	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C O	Qty	Description	Mfr Code	Mfr Part Number
A2R31	[illegible]	2	1	[illegible]	[illegible]	[illegible]
A701	[illegible]	1	1	[illegible]	[illegible]	[illegible]
A702	[illegible]	9	1	[illegible]	[illegible]	[illegible]
				A7 [illegible] ASSEMBLIES PARTS:		
	0380-0970	2	1	STANDOFF-HEX .375 IN LG 4-40 THD	[illegible]	[illegible]
	[illegible]	3	1	NUT-HEX-W/LKWR 4-40 THD .094 IN THK	[illegible]	[illegible]
	[illegible]	3	1	SCREW GROUND	[illegible]	[illegible]

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8	05344-60008	5	1	I/O BOARD/INTERFACE ASSEMBLY (SERIES 2140)	28480	05344-60008
A8C1	0160-0572	1	1	CAPACITOR-FXD 2200PF +-20% 100VDC CER	28480	0160-0572
A8C2	0160-3879	7	10	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A8C3	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A8C4	0140-0191	8	1	CAPACITOR-FXD 56PF +-5% 300VDC MICA	72136	DM15E560J0300WV1CR
A8C5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A8C6	0160-0576	5	2	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A8C7	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A8C8	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A8C9	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A8C10	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A8C11	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A8C12	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A8C13	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A8C14	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A8L1	9170-0029	3	1	CORE-SHIELDING BEAD	28480	9170-0029
A8Q1	1853-0440	0	1	TRANSISTOR PNP SI TO-92 PD=625MW	04713	[illegible]
A8R1	0757-0439	4	1	RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A8R2	0698-3162	0	1	RESISTOR 46.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4642-F
A8R3	2100-3161	6	1	RESISTOR-TRMR 20K 10% C SIDE-ADJ 17-TRN	02111	43P203
A8R4	0698-3432	7	1	RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
A8R5	0757-0398	4	1	RESISTOR 75 1% .125W F TC=0+-100	24546	C4-1/8-T0-75R0-F
A8R6	0757-0442	9	4	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A8R7	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A8R8	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A8R9	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A8TP1	0360-1682	0	9	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A8TP2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A8TP3	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A8TP4	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A8TP5	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A8TP6	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A8TP7	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A8TP8	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A8TP9	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A8U1	1820-2096	9	4	IC CNTR TTL LS BIN DUAL 4-BIT	01295	SN74LS393N
A8U2	1820-1951	1	1	IC CNTR TTL LS DECD DUAL 4-BIT	01295	SN74LS390N
A8U3	1826-0493	6	1	IC OP AMP GP 8-DIP-P PKG	27014	LM307N
A8U4	1826-0274	1	1	IC CONV 10-B D/A 16-DIP-P PKG	24355	AD7520LN
A8U5	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A8U6	1820-1430	3	2	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A8U7	1820-2096	9		IC CNTR TTL LS BIN DUAL 4-BIT	01295	SN74LS393N
A8U8	1820-2096	9		IC CNTR TTL LS BIN DUAL 4-BIT	01295	SN74LS393N
A8U9	1820-1050	9	1	IC FF TTL LS D-TYPE OCTL	01295	SN74LS374N
A8U10	1820-4640	5	1	IC MUXR/DATA-SEL TTL 16-TO-1-LINE 16-INP	01295	SN74150N
A8U11	1820-2544	9	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A8U12	1820-2096	9		IC CNTR TTL LS BIN DUAL 4-BIT	01295	SN74LS393N
A8U13	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A8U14	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A8U15	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A8U16	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A8XU10	1200-0541	1	1	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
				A8 MISCELLANEOUS PARTS		
	5000-9043	6	1	PIN:P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6846	5	1	P C BOARD EXTRACTOR GRAY	28480	5040-6846

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A9	05344-60009	6	1	ANALOG ASSEMBLY (SERIES 2140)	28480	05344-60009
A9C1	0180-0229	7	3	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A9C2	0160-4557	0	16	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A9C3	0180-1746	5	3	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A9C4	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A9C5	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A9C6	0160-3874	2	1	CAPACITOR-FXD 10PF +-.5PF 200VDC CER	28480	0160-3874
A9C7	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A9C8	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A9C9	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A9C10	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A9C11	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A9C12	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A9C13	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A9C14	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A9C15	0140-0193	8	2	CAPACITOR-FXD 82PF +-5% 300VDC MICA	72136	DM15F820J0300WV1CR
A9C16	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A9C17	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A9C18	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A9C19	0140-0193	8		CAPACITOR-FXD 82PF +-5% 300VDC MICA	72136	DM15F820J0300WV1CR
A9C20	0160-2250	6	1	CAPACITOR-FXD 5.1PF +-.25PF 500VDC CER	28480	0160-2250
A9C21	0160-0168	1	1	CAPACITOR-FXD .1UF +-10% 200VDC POLYE	28480	0160-0168
A9C22	0160-2222	2	1	CAPACITOR-FXD 1500PF +-5% 300VDC MICA	28480	0160-2222
A9C23	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A9C24	0160-4461	5	1	CAPACITOR-FXD 150PF +-2.5% 100VDC POLYE	28480	0160-4461
A9C25	0160-3533	0	1	CAPACITOR-FXD 470PF +-5% 300VDC MICA	28480	0160-3533
A9C26	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A9C27	0160-2236	8	1	CAPACITOR-FXD 1PF +-.25PF 500VDC CER	28480	0160-2236
A9C28	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A9C29	0160-2204	0	1	CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A9C30	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A9C31	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A9C32	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A9CR1	1901-0050	3	9	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A9CR2	1901-0535	9	4	DIODE-SM SIG SCHOTTKY	28480	1901-0535
A9CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A9CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A9CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A9CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A9CR7	1902-0777	3	2	DIODE-ZNR 1N825 6.2V 5% DO-7 PD=.4W	04713	1N825
A9CR8	1902-0777	3		DIODE-ZNR 1N825 6.2V 5% DO-7 PD=.4W	04713	1N825
A9CR9	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A9CR10	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A9CR11	1902-0180	7	1	DIODE-ZNR 1N827 6.2V 5% DO-7 PD=.4W	24046	1N827
A9CR12	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A9CR13	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A9CR14	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A9CR15	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A9CR16	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A9CR17	1902-3054	5	1	DIODE-ZNR 3.65V 5% DO-35 PD=.4W	28480	1902-3054
A9L1	9100-1788	6	3	CHOKE-WIDE BAND ZMAX=680 OHM@ 180 MHZ	02114	VK200 20/4B
A9L2	9100-1788	6		CHOKE-WIDE BAND ZMAX=680 OHM@ 180 MHZ	02114	VK200 20/4B
A9L3	9100-1788	6		CHOKE-WIDE BAND ZMAX=680 OHM@ 180 MHZ	02114	VK200 20/4B
A9Q1	1853-0089	5	9	TRANSISTOR PNP 2N4917 SI PD=200MW	07263	2N4917
A9Q2	1854-0221	9	1	TRANSISTOR-DUAL NPN PD=750MW	28480	1854-0221
A9Q3	1853-0089	5		TRANSISTOR PNP 2N4917 SI PD=200MW	07263	2N4917
A9Q4	1853-0089	5		TRANSISTOR PNP 2N4917 SI PD=200MW	07263	2N4917
A9Q5	1853-0089	5		TRANSISTOR PNP 2N4917 SI PD=200MW	07263	2N4917
A9Q6	1855-0082	2	2	TRANSISTOR J-FET P-CHAN D-MODE SI	28480	1855-0082
A9Q7	1854-0215	1	4	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A9Q8	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A9Q9	1855-0081	1	4	TRANSISTOR J-FET N-CHAN D-MODE SI	28480	1855-0081
A9Q10	1855-0081	1		TRANSISTOR J-FET N-CHAN D-MODE SI	28480	1855-0081
A9Q11	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A9Q12	1855-0082	2		TRANSISTOR J-FET P-CHAN D-MODE SI	28480	1855-0082
A9Q13	1853-0448	0	3	TRANSISTOR PNP SI TO-92 PD=625MW	04713	MPSH81
A9Q14	1853-0448	0		TRANSISTOR PNP SI TO-92 PD=625MW	04713	MPSH81
A9Q15	1854-0345	8	1	TRANSISTOR NPN 2N5179 SI TO-72 PD=200MW	04713	2N5179
A9Q16	1853-0448	0		TRANSISTOR PNP SI TO-92 PD=625MW	04713	MPSH81
A9Q17	1855-0049	1	1	TRANSISTOR J-FET DUAL N-CHAN D-MODE SI	28480	1855-0049
A9Q18	1853-0089	5		TRANSISTOR PNP 2N4917 SI PD=200MW	07263	2N4917
A9Q19	1854-0296	8	9	TRANSISTOR NPN SI TO-92 PD=310MW	28480	1854-0296
A9Q20	1854-0296	8		TRANSISTOR NPN SI TO-92 PD=310MW	28480	1854-0296

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7Q21	1854-0296	B		TRANSISTOR NPN SI TO-92 PD=310MW	28480	1854-0296
A7Q22	1853-0099	D		TRANSISTOR PNP 2N4917 SI PD=200MW	07263	2N4917
A7Q23	1854-0296	B		TRANSISTOR NPN SI TO-92 PD=310MW	28480	1854-0296
A7Q24	1855-0001	E		TRANSISTOR J-FET N-CHAN D-MODE SI	28480	1855-0001
A7Q25	1855-0001	E		TRANSISTOR J-FET N-CHAN D-MODE SI	28480	1855-0001
A7Q26	1854-0296	B		TRANSISTOR NPN SI TO-92 PD=310MW	28480	1854-0296
A7Q27	1853-0099	D		TRANSISTOR PNP 2N4917 SI PD=200MW	07263	2N4917
A7Q28	1854-0296	B		TRANSISTOR NPN SI TO-92 PD=310MW	28480	1854-0296
A7Q29	1853-0099	D		TRANSISTOR PNP 2N4917 SI PD=200MW	07263	2N4917
A7Q30	1854-0215	E		TRANSISTOR NPN SI PD=310MW FT=300MHZ	04713	2N3904
A7Q31	1854-0296	B		TRANSISTOR NPN SI TO-92 PD=310MW	28480	1854-0296
A7Q32	1853-0099	D		TRANSISTOR PNP 2N4917 SI PD=200MW	07263	2N4917
A7Q33	1854-0296	B		TRANSISTOR NPN SI TO-92 PD=310MW	28480	1854-0296
A7Q34	1854-0296	B		TRANSISTOR NPN SI TO-92 PD=310MW	28480	1854-0296
A7R1	2100-0552	E	1	RESISTOR 1MEG 5% 10% C SPNL ADJ 1-TRN	28480	2100-0552
A7R2	0698-0084	F	4	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4 1/8-TO-2151-F
A7R3	0698-0084	F		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4 1/8-TO-2151-F
A7R4	0757-0440	F	1	RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4 1/8-TO-7501-F
A7R5	0757-0500	F	1	RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4 1/8-TO-5621-F
A7R6	0757-0438	F	2	RESISTOR 619 1% .125W F TC=0+-100	24546	C4 1/8-TO-6190-F
A7R7	0757-0438	F		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4 1/8-TO-5111-F
A7R8	0757-0401	E	1	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4 1/8-TO-2001-F
A7R9	0757-0438	F		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4 1/8-TO-5111-F
A7R10	0757-0442	F	4	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1002-F
A7R11	0698-4037	D	12	RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4 1/8-TO-46R4-F
A7R12	0757-0401	E		RESISTOR 100 1% .125W F TC=0+-100	24546	C4 1/8-TO-101-F
A7R13	0698-0561	F	1	RESISTOR 787K 1% .125W F TC=0+-100	28480	0698-0561
A7R14	0698-0084	F		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4 1/8-TO-2151-F
A7R15	0699-0053	D	1	RESISTOR 10M 5% .125W F TC=0+-150	28480	0699-0053
A7R16	0757-0726	F	2	RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1781-F
A7R17	0757-0419	D	2	RESISTOR 681 1% .125W F TC=0+-100	24546	C4 1/8-TO-6810-F
A7R18	0698-4037	D		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4 1/8-TO-46R4-F
A7R19	0757-0444	F	2	RESISTOR 12.1K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1212-F
A7R20	0698-4037	D		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4 1/8-TO-46R4-F
A7R21	2100-3611	E	1	RESISTOR TRMR 50K 10% C SPNL ADJ 17-TRN	32997	3299P-1-503
A7R22	0757-0726	F		RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1781-F
A7R23	0757-1054	F	1	RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1471-F
A7R24	0698-3152	D	1	RESISTOR 3.48K 1% .125W F TC=0+-100	24546	C4 1/8-TO-3481-F
A7R25	0757-0442	F		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1002-F
A7R26	2100-3552	E	1	RESISTOR TRMR 1K 10% C SPNL ADJ 17-TRN	28480	2100-3552
A7R27	1810-0094	A	1	NETWORK RESISTOR 16-PIN DIP, RES	28480	1810-0094
A7R28	0698-3153	F	1	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4 1/8-TO-5111-F
A7R29	0757-0438	F		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1001-F
A7R30	0698-3153	F		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4 1/8-TO-5111-F
A7R31	0757-0438	F		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1001-F
A7R32	0698-6063	D	2	RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1961-F
A7R33	0698-6063	D		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1961-F
A7R34	0698-0083	D		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1961-F
A7R35	0757-0438	F		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1001-F
A7R36	0698-3153	F		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4 1/8-TO-5111-F
A7R37	0757-0419	D		RESISTOR 681 1% .125W F TC=0+-100	24546	C4 1/8-TO-6810-F
A7R38	0698-4037	D		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4 1/8-TO-46R4-F
A7R39	0757-0397	C	1	RESISTOR 324 1% .125W F TC=0+-100	19701	MF4C 1/8 TO 3240-F
A7R40	0757-0421	A	1	RESISTOR 825 1% .125W F TC=0+-100	24546	C4 1/8-TO-8250-F
A7R41	0698-3440	F	1	RESISTOR 17K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1702-F
A7R42	0698-4037	D		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4 1/8-TO-46R4-F
A7R43	0698-3015	F	1	RESISTOR 464 1% .125W F TC=0+-100	24546	C4 1/8-TO-4640-F
A7R44	0757-0479	D	2	RESISTOR 5.36K 1% .125W F TC=0+-100	24546	C4 1/8-TO-5361-F
A7R45	0757-0254	D	1	RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1211-F
A7R46	0698-4037	D		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4 1/8-TO-46R4-F
A7R47	0757-0417	F	2	RESISTOR 1.33K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1331-F
A7R48	0698-4037	D		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4 1/8-TO-46R4-F
A7R49	0757-0419	D		RESISTOR 681 1% .125W F TC=0+-100	24546	C4 1/8-TO-6810-F
A7R50	0698-0082	F		RESISTOR 464 1% .125W F TC=0+-100	24546	C4 1/8-TO-4640-F
A7R51	0757-0395	C	2	RESISTOR 274 1% .125W F TC=0+-100	24546	C4 1/8-TO-274R-F
A7R52	0698-3440	F	2	RESISTOR 21.5K 1% .125W F TC=0+-100	03508	PME55 1/8 TO 2152-F
A7R53	0698-4037	D		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4 1/8-TO-46R4-F
A7R54	0757-0417	F		RESISTOR 1.33K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1331-F
A7R55	0698-3443	D	1	RESISTOR 287 1% .125W F TC=0+-100	24546	C4 1/8-TO-287R-F
A7R56	0757-0419	D		RESISTOR 681 1% .125W F TC=0+-100	24546	C4 1/8-TO-6810-F
A7R57	0757-0438	F		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4 1/8-TO-5111-F
A7R58	0698-3450	F	1	RESISTOR 42.2K 1% .125W F TC=0+-100	24546	C4 1/8-TO-4222-F
A7R59	0757-0869	D	1	RESISTOR 15K 1% .125W F TC=0+-100	24546	C4 1/8-TO-1502-F
A7R60	0757-0395	C		RESISTOR 274 1% .125W F TC=0+-100	24546	C4 1/8-TO-274R-F

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A9R61	0698-3156	2	2	RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A9R62	0698-3157	3	1	RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A9R63	0698-3160	8	1	RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
A9R64	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A9R65	0757-0419	0		RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A9R66	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A9R67	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A9R68	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
A9R69	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A9R70	0757-0444	1		RESISTOR 12.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1212-F
A9R71	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A9R72	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A9R73	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A9R74	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A9R75	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A9R76	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A9R77	0757-0438	7	1	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A9R78	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A9R79	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A9R80	0698-3150	4	1	RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
A9R81	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A9R82	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A9R83	0757-0199	3	1	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A9R84	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A9R85	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A9R86	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A9R87	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A9R88	0757-0416	7	2	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A9R89	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A9R90	0757-0421	4		RESISTOR 825 1% .125W F TC=0+-100	24546	C4-1/8-T0-825R-F
A9R91	0757-0439	4	1	RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A9R92	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A9R93	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A9R94	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A9R95	0757-0421	4		RESISTOR 825 1% .125W F TC=0+-100	24546	C4-1/8-T0-825R-F
A9R96	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A9R97	0698-3136	8	1	RESISTOR 17.8K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1782-F
A9R98	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A9R99	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A9R100	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
A9R101	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A9R102	0698-3151	7	1	RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F
A9R103	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A9TP1	0360-1682	0	3	TERMINAL STUD SGL-TUR PRESS-MTG	28480	0360-1682
A9TP2	0360-1682	0		TERMINAL STUD SGL-TUR PRESS-MTG	28480	0360-1682
A9TP3	0360-1682	0		TERMINAL STUD SGL-TUR PRESS-MTG	28480	0360-1682
A9U1	1820-1196	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A9U2	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A9U3	1820-0817	6	1	IC FF ECL D-M/S DUAL	04713	MC10231P
A9U4	1826-0143	4	1	IC OP AMP GP TO-99 PKG	3L585	CA3130T
A9U5	1858-0001	4	1	TRANSISTOR ARRAY 14-PIN PLSTC DIP	3L585	CA3046
A9U6	1826-0493	6	1	IC OP AMP LP 8-DIP-P PKG	27014	LM308N
A9U7	1826-0088	3	1	IC OP AMP GP 8-DIP-P PKG	27014	LM301AN
A9W1	8159-0005	0	1	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
				A9 MISCELLANEOUS PARTS		
	5000-9043	6	1	PIN:P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6843	4	1	PC BOARD EXTRACTOR, WHITE	28480	5040-6843

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10	05344-60010	9	1	DIGITAL ASSEMBLY (SERIES 2140)	28480	05344-60010
A10C1	0160-4557	0	9	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A10C2	0180-1746	5	1	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A10C3	0140-0191	0	1	CAPACITOR-FXD 56PF +-5% 300VDC MICA	72136	DM15E560J0300WV1CR
A10C4	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A10C5	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A10C6	0160-4554	7	5	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A10C7	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A10C8	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A10C9	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A10C10	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A10C11	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A10C12	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A10C13	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A10C14	0180-0229	7	1	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A10C15	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A10C16	0140-0210	2	1	CAPACITOR-FXD 270PF +-5% 300VDC MICA	72136	DM15F271J0300WV1CR
A10C17	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A10C18	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A10C19	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A10C20	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A10CR1	1902-3030	2	1	DIODE-ZNR 3.01V 5% DO-7 PD=.4W TC=-.062%	28480	1902-3030
A10CR2	1902-3040	2	1	DIODE-ZNR 3.48V 5% DO-35 PD=.4W	28480	1902-3040
A10E1	9170-0029	3	1	CORE-SHIELDING BEAD	28480	9170-0029
A10L1	9100-1788	6	2	CHOKE-WIDE BAND ZMAX=680 OHM@ 180 MHZ	02114	VK200 20/4B
A10L2	9100-1788	6		CHOKE-WIDE BAND ZMAX=680 OHM@ 180 MHZ	02114	VK200 20/4B
A10L3	9100-3139	5	1	INDUCTOR 25UH 15% .5DX.925LG	28480	9100-3139
A10L4	9100-3559	3	1	INDUCTOR RF-CH-MLD 5.1UH 5% .166DX.385LG	28480	9100-3559
A10Q1	1853-0440	0	1	TRANSISTOR PNP SI TO-92 PD=625MW	04713	MPS3640
A10Q2	1854-0071	7	1	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A10R1	0757-0442	9	12	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A10R2	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A10R3	0757-0280	3	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A10R4	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A10R5	0698-3442	7	1	RESISTOR 237 1% .125W F TC=0+-100	03888	PME55-1/8-T0-237R-F
A10R6	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A10R7	0757-0350	4	1	RESISTOR 25 1% .125W F TC=0+-100	24546	C4-1/8-T0-25R0-F
A10R8	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A10R9	0757-0338	2	1	RESISTOR 1K 1% .25W F TC=0+-100	24546	C5-1/4-T0-1001-F
A10R10	1810-0251	9	1	NETWORK-RES 8-SIP2.2K OHM X 7	91121	208A222
A10R11	0698-0084	9	2	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A10R12	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A10R13	0757-0444	1	1	RESISTOR 12.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1212-F
A10R14	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A10R15	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A10R16	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A10R17	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A10R18	0757-0279	0	1	RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A10R19	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A10R20	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A10R21	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A10R22	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A10R23	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A10TP1	0360-1682	0	8	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A10TP2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A10TP3	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A10TP4	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A10TP5	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A10TP6	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A10TP7	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A10TP8	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A10U1	1820-0629	0	8	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
A10U2	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
A10U3	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
A10U4	1820-0693	8	2	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A10U5	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A10U6	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
A10U7	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
A10U8	1820-2004	9	1	IC MISC NMOS	28480	1820-2004
A10U9	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
A10U10	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10U11	1820-0801	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
A10U12	1820-1279	8	2	IC CNTR TTL LS DECD UP/DOWN SYNCHRO	01295	SN74LS190N
A10U13	1820-1196	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A10U14	1820-1641	8	1	IC DRVR TTL LS BUS DRVR HEX 1-INP	01295	SN74LS365AN
A10U15	1820-0681	4	4	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A10U16	1820-1279	8		IC CNTR TTL LS DECD UP/DOWN SYNCHRO	01295	SN74LS190N
A10U17	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A10U18	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A10U19	1820-0627	8		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
A10U20	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
A10U21	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A10U22	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A10W1	8159-0005	0	1	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
A10XU8	1200-0545	5	1	SOCKET-IC 28-CONT DIP SLDR	28480	1200-0545
				A10 MISCELLANEOUS PARTS		
	5000-9043	6	1	PIN:P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6042	[illegible]	1	EXTRACTOR, P.C BOARD-BLACK	28480	5040-6042

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11	05344-60011	0	1	MAIN ROM/FILTER ASSEMBLY (SERIES 2144)	28480	05344-60011
A11C1	0160-2150	5	2	CAPACITOR-FXD 33PF +-5% 300VDC MICA	28480	0160-2150
A11C2	0160-2150	5		CAPACITOR-FXD 33PF +-5% 300VDC MICA	28480	0160-2150
A11C3	0160-3879	7	14	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C6	0180-0210	6	1	CAPACITOR-FXD 3.3UF+-20% 15VDC TA	56289	150D335X0015A2
A11C7	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C8	0180-2929	8	1	CAPACITOR-FXD 68UF+-10% 15VDC TA	28480	0180-2929
A11C9	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C10	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C11	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C12	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C13	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C14	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C15	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C16	0160-3875	3	1	CAPACITOR-FXD 22PF +-5% 200VDC CER 0+-30	28480	0160-3875
A11C17	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C18	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C19	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11CR1	1901-0047	8	3	DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A11CR2	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A11CR3	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A11L1	9100-1788	6	1	CHOKE-WIDE BAND ZMAX=680 OHM@ 180 MHZ	02114	VK200 20/4B
A11R1	0757-0439	4	2	RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A11R2	0757-0439	4		RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A11R3	0757-1100	6	1	RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301-F
A11R4	0698-3452	1	1	RESISTOR 147K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1473-F
A11R5	1810-0301	4	16	NETWORK-RES 16-DIP51.0 OHM X 8	01121	316A510
A11R6	1810-0301	4		NETWORK-RES 16-DIP51.0 OHM X 8	01121	316A510
A11R7	1810-0301	4		NETWORK-RES 16-DIP51.0 OHM X 8	01121	316A510
A11R8	1810-0301	4		NETWORK-RES 16-DIP51.0 OHM X 8	01121	316A510
A11R9	1810-0301	4		NETWORK-RES 16-DIP51.0 OHM X 8	01121	316A510
A11R10	1810-0301	4		NETWORK-RES 16-DIP51.0 OHM X 8	01121	316A510
A11R11	1810-0301	4		NETWORK-RES 16-DIP51.0 OHM X 8	01121	316A510
A11R12	1810-0301	4		NETWORK-RES 16-DIP51.0 OHM X 8	01121	316A510
A11R13	1810-0322	9	2	NETWORK-RES 10-SIP220.0 OHM X 9	01121	210A221
A11R14	0757-0394	0	3	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A11R15	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A11R16	1810-0301	4		NETWORK-RES 16-DIP51.0 OHM X 8	01121	316A510
A11R17	1810-0301	4		NETWORK-RES 16-DIP51.0 OHM X 8	01121	316A510
A11R18	1810-0301	4		NETWORK-RES 16-DIP51.0 OHM X 8	01121	316A510
A11R19	1810-0301	4		NETWORK-RES 16-DIP51.0 OHM X 8	01121	316A510
A11R20	1810-0301	4		NETWORK-RES 16-DIP51.0 OHM X 8	01121	316A510
A11R21	1810-0301	4		NETWORK-RES 16-DIP51.0 OHM X 8	01121	316A510
A11R22	1810-0301	4		NETWORK-RES 16-DIP51.0 OHM X 8	01121	316A510
A11R23	1810-0301	4		NETWORK-RES 16-DIP51.0 OHM X 8	01121	316A510
A11R24	1810-0322	9		NETWORK-RES 10-SIP220.0 OHM X 9	01121	210A221
A11R25	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A11R26	0698-3155	1	1	RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A11R27	0757-0199	3	3	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A11R28	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A11R29	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A11TP1	0360-1682	0	11	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A11TP2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A11TP3	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A11TP4	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A11TP5	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A11TP6	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A11TP7	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A11TP8	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A11TP9	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A11TP10	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A11TP11	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A11U1	05344-80005	4	1	PROGRAMMED PROM	28480	05344-80005
A11U2	1820-1437	0	1	IC MV TTL LS MONOSTBL DUAL	01295	SN74LS221N
A11U3	1820-1416	5	2	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A11U4	05344-80002	1	1	PROGRAMMED PROM	28480	05344-80002
A11U5	1820-2024	3	1	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11U6	05344-80003	2	1	PREPROGRAMMED PROM	28480	05344-80003
A11U7	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A11U8	05344-80004	7	1	PREPROGRAMMED PROM	28480	05344-80004
A11U9	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A11U10	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A11U11	1820-2075	4	1	IC MISC TTL LS	01295	SN74LS245N
A11U12	1820-[illegible]	5	1	IC INV TTL LS HEX	01295	SN74LS04N
A11U13	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A11U14	1820-1245	0	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS155N
A11U15	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
A11W1	0159-0005	0	2	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0159-0005
A11W2	0159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0159-0005
A11XU1	1200-0541	1	4	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A11XU4	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A11XU6	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A11XU8	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
				A11 MISCELLANEOUS PARTS		
	5000-9043	6	1	PIN:P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6053	A	1	EXTRACTOR, BROWN	28480	5040-6053

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A12	[illegible]	1	1	POWER SUPPLY ASSEMBLY [illegible]	[illegible]	[illegible]
A12C1	[illegible]	6	[illegible]	[illegible]	[illegible]	[illegible]
A12C2	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
A12C3	[illegible]	6		[illegible]	[illegible]	[illegible]
A12C4	[illegible]	1	[illegible]	[illegible]	[illegible]	[illegible]
A12C5	[illegible]	1		[illegible]	[illegible]	[illegible]
A12C6	[illegible]	4	1	[illegible]	[illegible]	[illegible]
A12C7	[illegible]	7	1	[illegible]	[illegible]	[illegible]
A12C8	[illegible]	4	1	[illegible]	[illegible]	[illegible]
A12C9	[illegible]	2		[illegible]	[illegible]	[illegible]
A12C10	[illegible]	1		[illegible]	[illegible]	[illegible]
A12C11	[illegible]	1		[illegible]	[illegible]	[illegible]
A12C12	[illegible]	6		[illegible]	[illegible]	[illegible]
A12C13	[illegible]	1		[illegible]	[illegible]	[illegible]
A12C14	[illegible]	2		[illegible]	[illegible]	[illegible]
A12CR1	[illegible]	6	1	[illegible]	[illegible]	[illegible]
A12F1	[illegible]	1	1	[illegible]	[illegible]	[illegible]
A12Q1	[illegible]	4	1	[illegible]	[illegible]	[illegible]
A12Q2	[illegible]	7	1	[illegible]	[illegible]	[illegible]
A12R1	[illegible]	0	[illegible]	[illegible]	[illegible]	[illegible]
A12R2	[illegible]	0	4	[illegible]	[illegible]	[illegible]
A12R3	[illegible]	9	4	[illegible]	[illegible]	[illegible]
A12R4	[illegible]	0		[illegible]	[illegible]	[illegible]
A12R5	[illegible]	1		[illegible]	[illegible]	[illegible]
A12R6	[illegible]	1	1	[illegible]	[illegible]	[illegible]
A12R7	[illegible]	0	1	[illegible]	[illegible]	[illegible]
A12R8	[illegible]	5	1	[illegible]	[illegible]	[illegible]
A12R9	[illegible]	9		[illegible]	[illegible]	[illegible]
A12R10	[illegible]	7	1	[illegible]	[illegible]	[illegible]
A12R11	[illegible]	1		[illegible]	[illegible]	[illegible]
A12R12	[illegible]	2	1	[illegible]	[illegible]	[illegible]
A12R13	[illegible]	1	1	[illegible]	[illegible]	[illegible]
A12R14	[illegible]	4	1	[illegible]	[illegible]	[illegible]
A12R15	[illegible]	2	1	[illegible]	[illegible]	[illegible]
A12R16	[illegible]	0		[illegible]	[illegible]	[illegible]
A12R17	[illegible]	9		[illegible]	[illegible]	[illegible]
A12R18	[illegible]	1	1	[illegible]	[illegible]	[illegible]
A12R19	[illegible]	9		[illegible]	[illegible]	[illegible]
A12U1	[illegible]	0	1	[illegible]	[illegible]	[illegible]
A12U2	[illegible]	7	1	[illegible]	[illegible]	[illegible]
A12U3	[illegible]	1	1	[illegible]	[illegible]	[illegible]
A12U4	[illegible]	1	1	[illegible]	[illegible]	[illegible]
				A12 MISCELLANEOUS PARTS		
	[illegible]	1	1	HEAT SINK [illegible]	[illegible]	[illegible]
	[illegible]	8	10	[illegible]	[illegible]	[illegible]
	[illegible]	2	1	HEAT SINK	[illegible]	[illegible]
	[illegible]	0	4	TERMINAL [illegible]	[illegible]	[illegible]
	[illegible]	6	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	7	10	[illegible]	[illegible]	[illegible]
	[illegible]	6	[illegible]	[illegible]	[illegible]	[illegible]

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A13	05344-60013	2	1	MOTHERBOARD ASSEMBLY (SERIES 2136)	28480	05344-60013
A13C1	0180-2541	0	2	CAPACITOR-FXD 10000UF+75-10% 40VDC AL	28480	0180-2541
A13C2	0180-2908	1	1	CAPACITOR-FXD [illegible] 20VDC AL	28480	0180-2908
A13C3	0180-0574	5	1	CAPACITOR-FXD 40000UF+75-10% 20VDC AL	28480	0180-0574
A13C4	0180-2541	0		CAPACITOR-FXD 10000UF+75-10% 40VDC AL	28480	0180-2541
A13C5	0180-0374	3	1	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A13CR1	1906-0096	7	3	DIODE-FW BRDG 200V 2A	04713	MDA202
A13CR2	1901-0731	7	3	DIODE-PWR RECT 400V 1A	28480	1901-0731
A13CR3	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A13CR4	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A13CR5	1906-0096	7		DIODE-FW BRDG 200V 2A	04713	MDA202
A13CR6	1906-0096	7		DIODE-FW BRDG 200V 2A	04713	MDA202
A13CR7	1902-1268	3	1	DIODE-ZNR 1N5350B 13V 5% PD=5W TC=+[illegible]	04713	1N5350B
A13J1	1250-0836	2	3	CONNECTOR-RF SMC M PC 50-OHM	28480	1250-0836
A13J2	1200-0541	1	1	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A13J3	1250-0836	2		CONNECTOR-RF SMC M PC 50-OHM	28480	1250-0836
A13J4	1250-0836	2		CONNECTOR-RF SMC M PC 50-OHM	28480	1250-0836
A13Q1	1884-0024	3	1	THYRISTOR-SCR VRRM=200	28480	1884-0024
A13Q2	1884-0266	5	1	THYRISTOR-SCR 2N6400 TO-220AB VRRM=50	04505	2N6400
A13R1	0757-0904	4	1	RESISTOR 10 1% .5W F TC=0+-100	28480	0757-0904
A13R2	0811-1202	7	1	RESISTOR .50 5% 3W PW TC=0+-90	28480	0811-1202
A13T1	9100-4224	1	1	TRANSFORMER-POWER	28480	9100-4224
A13W1	05344-60105	3	1	CABLE ASSEMBLY Z INPUT	28480	05344-60105
A13W2	05344-60106	4	1	CABLE ASSEMBLY SWEEP OUTPUT	28480	05344-60106
A13W3	05344-60113	1	1	CABLE ASSEMBLY Z OUTPUT	28480	05344-60113
A13W4	05344-60107	5	1	CABLE ASSEMBLY SWEEP TRIGGER	28480	05344-60107
A13W5	05344-60114	2	1	CABLE ASSEMBLY SWEEP INPUT	28480	05344-60114
A13W6	05344-60100	6	1	CABLE ASSEMBLY FM OUTPUT	28480	05344-60100
A13W7	05344-60109	7	1	CABLE ASSEMBLY 10 MHZ INPUT	28480	05344-60109
A13W8	8120-3436	6	1	CABLE ASSEMBLY HP INTERFACE	28480	8120-3436
A13W9	05344-60112	2	1	CABLE ASSEMBLY IF INPUT	28480	05344-60112
A13W10	05344-60111	3	1	CABLE ASSEMBLY [illegible]	28480	05344-60111
A13XA3A	1251-2026	8	11	CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS	28480	1251-2026
A13XA3B	1251-2026	8		CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS	28480	1251-2026
A13XA4A	1251-2026	8		CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS	28480	1251-2026
A13XA4B	1251-2026	8		CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS	28480	1251-2026
A13XA5A	1251-2026	8		CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS	28480	1251-2026
A13XA5B	1251-2026	8		CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS	28480	1251-2026
A13XA6	1251-1365	6	3	CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A13XA7	1251-2034	8	1	CONNECTOR-PC EDGE 10-CONT/ROW 2-ROWS	28480	1251-2034
A13XA8A	1251-2026	8		CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS	28480	1251-2026
A13XA8B	1251-2026	8		CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS	28480	1251-2026
A13XA9	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A13XA10	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A13XA11A	1251-2026	8		CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS	28480	1251-2026
A13XA11B	1251-2026	8		CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS	28480	1251-2026
A13XA12	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
				A13 MISCELLANEOUS PARTS		
	0380-0992	5	4	STANDOFF-HEX .25-IN-LG 6-32THD	00000	ORDER BY DESCRIPTION
	1251-1115	4	1	POLARIZING KEY-PC EDGE CONN	28480	1251-1115
	2190-0010	7	1	WASHER-LK EXT T NO. 8 .17-IN-ID	28480	2190-0010
	2190-0012	9	8	WASHER-LK EXT T NO. 10 .195-IN-ID	28480	2190-0012
	2360-0115	4	4	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	2420-0003	7	1	NUT-HEX-DBL-CHAM 6-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
	2510-0053	8	1	SCREW-MACH 8-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	2510-0135	7	1	SCREW-MACH 8-32 2.25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	2680-0129	0	8	SCREW-MACH 10-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	3050-0226	2	8	WASHER-FL MTLC NO. 10 .203-IN-ID	28480	3050-0226
A14	0960-0443	1	1	POWER MODULE-FILTERED	28480	0960-0443

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				CHASSIS PARTS		
B1	3160-0209	4		FAN-TRAX 32-CFM 105-125V 50/60-Hz	23936	8500D
RPG1	5060-0329	9	1	ROTARY PULSE GENERATOR	28480	5060-0329
S1	3103-0056	0	1	SWITCH-THRM FXD +167F 15A OPN-ON-RISE	28480	3103-0056
S2	3101-0163	5	2	SWITCH-TGL SUBMIN SPDT 5A 115VAC	28480	3103-0163
S3	3101-0163	5		SWITCH-TGL SUBMIN SPDT 5A 115VAC	28480	3103-0163
W1	8120-3435	5	1	CABLE ASSEMBLY-EXTERNAL INTERFACE	28480	8120-3435
W2	05344-60101	9	1	CABLE ASSEMBLY-POWER	28480	05344 60101
				MISCELLANEOUS PARTS		
	0050-0515	7	4	LINK LOCK FRONT	28480	0050-0515
	0362-0227	1	4	CONNECTOR-SGL CONT SKT 1.14 MM BSC SZ	28480	0362-0227
	0362-0265	7	9	CONNECTOR-SGL CONT SKT 1.14 MM BSC SZ	28480	0362-0265
	0370-1303	3	1	KNOB BASE 1-1/2	28480	0370-1303
	1250-0083	1	4	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50 OHM	28480	1250-0083
	1400-0015	0	2	CLAMP-CABLE .25 DIA .375 WD STL	28480	1400-0015
	1400-0617	0	5	CLAMP-CABLE .312 DIA .325 WD NYL	28480	1400-0617
	1400-0082	9	1	CLAMP-CABLE .125 DIA .375 WD NYL	28480	1400-0082
	1400-0249	0	1	CABLE TIE .062-.625-DIA .091 WD NYL	06383	PLT1M-8
	1460-1345	5	2	TILT STAND SST	28480	1460-1345
	1901-1001	6	1	DIODE PACKAGE	28480	1901-1001
F1	2110-0305	5	1	FUSE 1.25A 250V TD 1.25X.25 UL	75915	313 1.25
F1	2110-0424	2		FUSE .25A 250V TD 1.25X.25 UL	75915	313.250
	7101-0606	5	1	PANEL 5344A	28480	7101-0606
	7120-1254	1	1	PLATE HP LOGO	28480	7120-1254
	7120-6629	4	1	LABEL "REMOTE ET"	28480	7120-6629
	7121-2507	1	1	LABEL-POWER MOD	28480	7121-2507
	7121-2600	3	1	LABEL OPERATING INSTRUCTIONS	28480	7121-2600
	8120-1378	1	1	CABLE ASSY 18AWG 3-CNDCT JGK-JKT	28480	8120-1378
	8120-4320	7	2	CABLE ASSEMBLY 10"	28480	8120-4320
	5001-0423	0	1	TOP COVER	28480	5001-0423
	5001-0439	8	2	TRIM STRIP SIDE	28480	5001-0439
	5020-8815	0	1	FRAME FRONT	28480	5020-8815
	5020-8816	1	1	FRAME REAR	28480	5020-8816
	5020-8837	6	2	STRUT CORNER	28480	5020-8837
	5020-8896	7	2	HANDLE TRIM FRONT	28480	5020-8896
	5040-7201	8	4	FOOT	28480	5040-7201
	5040-7203	0	1	TRIM TOP 1/2	28480	5040-7203
	5040-7219	8	1	STRAP HANDLE CAP, FRONT	28480	5040-7219
	5040-7220	1	1	STRAP HANDLE CAP, REAR	28480	5040-7220
	5060-9804	3	1	STRAP HANDLE ASSEMBLY	28480	5060-9804
	5060-9859	6	2	STRAP SYSTEM II	28480	5060-9859
	5061-1240	4	1	COVER BOTTOM	28480	5061-1240
	05344-00001	2	1	HEAT SINK	28480	05344 00001
	05344-00002	3	1	BRACKET MOTHERBOARD	28480	05344-00002
	05344-00003	4	1	RFI SHIELD	28480	05344 00003
	05344-00004	5	1	PANEL SUB	28480	05344 00004
	05344-00005	6	1	PANEL REAR	28480	05344 00005
	05344-00006	7	1	SHIELD HP INTERFACE	28480	05344 00006
	05344-00007	8	1	COVER REAR CAST	28480	05344 00007
	05344-00008	9	1	COVER FRONT CAST	28480	05344 00008
	05344-00009	0	1	CLAMP HP CABLE	28480	05344-00009
	05344-00010	3	1	SUPPORT DIODE	28480	05344-00010
	05344-00011	4	1	INSULATOR POWER SUPPLY HEAT SINK	28480	05344 00011
	05344-20201	6	1	HOUSING MAIN	28480	05344 20201
				OPTION KITS		
	5061-0077	6	2	KIT RACK FLANGE (OPTION 908)	28480	5061-0077
	5061-0089	0	1	KIT FRONT HANDLE (OPTION 1412)	28480	5061 0089
	5061-2071	4	1	RACK-FLANGE (OPTION 913)	28480	5061 2071
	05344-60114	4		CABLE ASSEMBLY ID (OPTION 142)	28480	05344 60114
	5061-0077	6		KIT RACK FLANGE (OPTION 908)	28480	5061 0077

Table 6-3. Manufacturers Code List

Mfr. No.	Manufacturer Name	Address	Zip Code
00000	Any Satisfactory Supplier		
01121	Allen-Bradley Company, Milwaukee, WI		53204
01295	Texas Instrument, Inc., Semiconductor Component Division, Dallas, TX		75222
02111	Spectrol Electronics Corporation, City of Indiana, CA		91745
02114	Ferroxcube Corporation, Saugerties, NY		12477
03888	K.D.I. Pyrofilm Corporation, Whippany, NJ		07981
04713	Motorola Semiconductor Products, Phoenix, AZ		85008
06383	Panduit Corporation, Tinley Park, IL		60477
07263	Fairchild Semiconductor Division, Mountain View, CA		94042
16299	Corning Glass Works, Component Division, Raleigh, NC		27604
16546	U.S. Capacitor Corporation, Burbank, CA		91504
18324	Signetics Corporation, Sunnyvale, CA		94086
19701	Mepco/Electra Corporation, Mineral Wells, TX		76067
23936	Pamotor Division, William I. Purdy, Burlingame, CA		94010
24046	Transitron Electronic Corporation, Wakefield, MA		01880
24355	Analog Devices, Incorporated, Norwood, MA		02062
24546	Corning Glass Works (Bradford), Bradford, PA		16701
25088	Siemens Corporation, Iselin, NJ		08830
27014	National Semiconductor Corporation, Santa Clara, CA		95051
28480	Hewlett-Packard Company, Corporate Headquarters, Palo Alto, CA		94304
3L585	RCA Corporation, Solid State Division, Somerville, NJ		
32997	Bourns Incorporated, Trimpot Product Division, Riverside, CA		92507
34649	Intel Corporation, Mountain View, CA		95051
50088	Mostek Corporation, Carrollton, TX		75006
56289	Sprague Electric Company, North Adams, MA		01247
71400	Bussman Manufacturing Division of McGraw-Edison Company, St. Louis, MO		63107
72136	Electro Motive Corporation, Florence, SC		06226
75915	Littelfuse, Incorporated, Des Plaines, IL		60016
84411	TRW Capacitor Division, Ogallala, NE		69153
91506	Augat, Incorporated, Attleboro, MA		02703

SECTION VII
MANUAL CHANGES

7-1. INTRODUCTION

7-2. This section contains information necessary to adapt the manual to apply to older instruments.

7-3. MANUAL CHANGES

7-4. This manual applies directly to Model 5344S Microwave Source Synchronizers with serial number prefix 2314A and below.

7-5. As engineering changes are made, newer instruments may have serial prefix numbers higher than those listed on the title page of this manual. The manuals for these instruments will be supplied with MANUAL CHANGES sheets containing the required information. Replace affected pages or modify existing manual information as directed in the MANUAL CHANGES pages. Contact the nearest Hewlett-Packard Sales and Support Office (listed at the back of this manual), if the change information is missing.

7-6. OLDER INSTRUMENTS

7-7. To adapt this manual to older instruments having a serial number prefix of 2140A or lower, make the changes listed under CHANGE 1. This applies to all instruments except the following:

2140A00126	2140A00135
2140A00129	2140A00137
2140A00130	2140A00138
2140A00133	2140A00139
2140A00134	2140A00140

CHANGE 1

Page 8-103, Figure 8-27, A4 Schematic Diagram:
In upper left of diagram, delete +5V connected to U9A(2) and U9B(11). Connect both of these pins to the junction of resistor R45 and U8(11).

SECTION VIII
SERVICE

8-1. INTRODUCTION

8-2. This section provides service information that includes descriptions of symbols and reference designators, pc board identification and location, safety considerations, disassembly and reassembly, troubleshooting information, theory of operation, block diagrams and schematic diagrams.

8-3. SCHEMATIC DIAGRAM SYMBOLS AND REFERENCE DESIGNATORS

8-4. *Figure 8-1* shows various common symbols used on the schematic diagrams. In addition, the identification system for reference designations, assemblies and subassemblies is shown. Logic symbols used on the schematic diagrams in this manual conform to the American National Standard ANSI Y32.14-1973 (IEEE Std.91-1973). This standard supersedes MIL-STD-806B.

8-5. Reference designators are assigned to indicate the class and the location of printed-circuit assemblies (boards), subassemblies (if any) and all of the component parts, as shown in the example in *Figure 8-1*. Assemblies are assigned numbers in sequence, A1,A2, etc. Component parts are numbered in sequence, from left to right, top to bottom, according to the physical location on the board. As shown in *Figure 8-1*, sub-assemblies within an assembly are given a subordinate A number. For example, rectifier assembly A1 has the complete designator of A25A1. For individual components, the complete designator is determined by adding the assembly number and subassembly number, if any. For example, CR1 an the rectifier assembly is designated A25A1CR1.

8-6. IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS

8-7. Hewlett-Packard printed circuit boards (see *Figure 8-1)* have four identification numbers: an assembly part number, a series number, a revision letter, and a production code.

8-8. The assembly part number has 10 digits (such as 05344-60001) and is the primary identification. All assemblies with the same part number are interchangeable. When a production change is made on an assembly that makes it incompatible with previous assemblies, a change in part number is required. The series number (such as 2202) is used to document minor electrical changes. As changes are made, the series number is incremented. When replacement boards are ordered, you may receive a replacement with a different series number. If there is a difference between the series number marked on the board and the schematic in this manual, a minor electrical difference exists. If the number on the printed circuit board is lower than that on the schematic, refer to Section VII for backdating information. If it is higher, refer to the looseleaf manual change sheets for this manual. If the manual change sheets are missing, contact your local Hewlett-Packard Sales and Support Office. See the listing inside the back cover of this manual.

8-9. Revision letters (A,B,etc.) denote changes in printed circuit layout. For example, if a capacitor type is changed (electrical value may remain the same) and requires different spacing for its leads, the printed circuit board layout is changed and the revision letter is incremented to the next letter. When a revision letter changes, the series number is also usually changed. The production code is the four-digit seven-segment number used for production purposes.

SYMBOLS

DANGEROUS VOLTAGE, EXCEEDS 1000 VOLTS

FRONT PANEL LABEL

REAR PANEL LABEL

INTERIOR AND PC BOARDS LABEL

WIPER MOVES TOWARD 'CW' WHEN CONTROL IS ROTATED CLOCKWISE

PROTECTIVE CONDUCTOR TERMINAL

CIRCUIT COMMON

IDENTIFIED COMMON

CHASSIS TERMINAL

KNOB CONTROL

SCREWDRIVER ADJUST

MAIN SIGNAL PATH

FEEDBACK PATH

TEST POINT

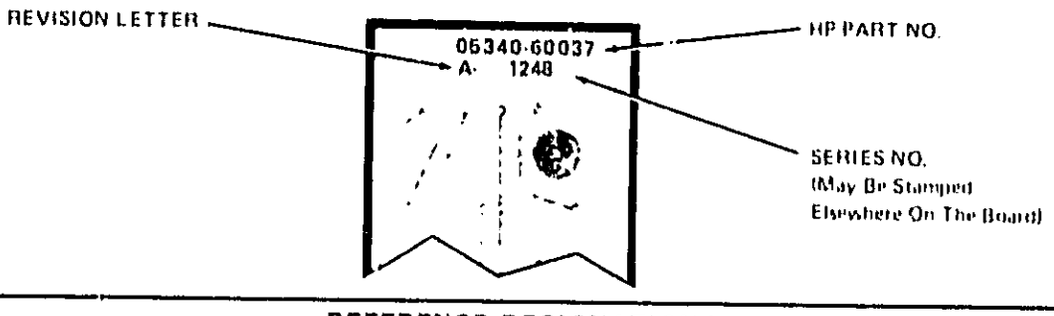
INSTRUCTION MANUAL REFERENCE

ALTERNATING CURRENT

DIRECT CURRENT

ALTERNATING OR DIRECT CURRENT

PRINTED CIRCUIT BOARD IDENTIFICATION



REFERENCE DESIGNATIONS

REFERENCE DESIGNATIONS WITHIN ASSEMBLIES ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION. JACKS ARE THE STATIONARY CONNECTORS AND PLUGS ARE THE MORE MOVEABLE OF TWO CONNECTORS.

ASSEMBLY	ABBREVIATION	COMPLETE DESCRIPTION
A25	C1	A25C1
A25A1	CR1	A25A1CR1
NO PREFIX	J3	J3

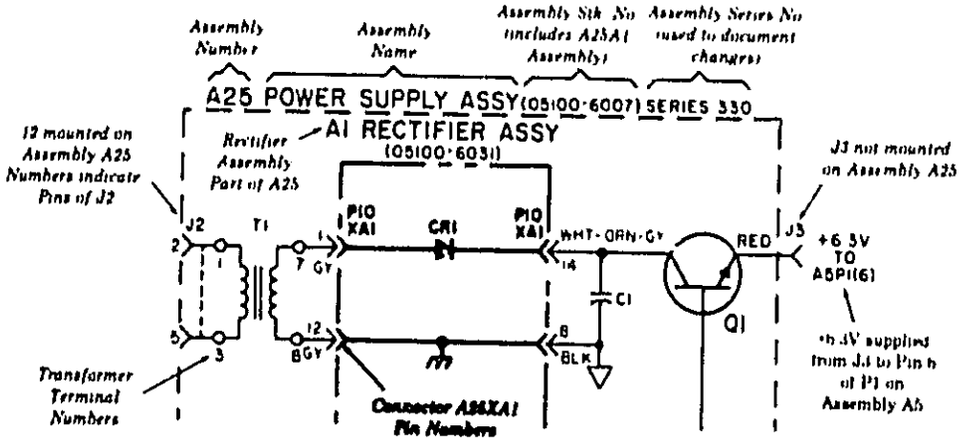


Figure 8-1. Schematic Diagram Notes

8-10. ASSEMBLY IDENTIFICATION

8-11. The assembly number, name, and HP part number of printed circuit assemblies (boards) in the 5344A are listed in *Table 8-1*.

8-12. ASSEMBLY LOCATIONS

8-13. Front, rear, top, and bottom views of the 5344A are shown in *Figures 8-2* through *8-6*. These views identify parts, such as panel control switches, connectors and indicators, in addition to locations of assemblies and adjustments.

Table 8-1. Assembly Identification

Assembly	Name	HP Part No.
A1	Keyboard/Display	05344-60001
A2	Connector	05342-60029
A3	Keyboard/Display Interrupt	05344-60003
A4	HP-IB Interface	5344-60004
A5	R/W Memory/Decoder	05344-60005
A6	Main Loop	05344-60006
A7	VCO	05344-60007
A8	10V Ramp/Timebase	05344-60008
A9	Analog	05344-60009
A10	Digital	05344-60010
A11	Main ROM/Buffer	05344-60011
A12	Power Supply	05344-60012
A13	Motherboard	05344-60013
A14	Power Module	0960-0443

8-14. SAFETY CONSIDERATIONS

8-15. Although the instrument has been designed in accordance with international safety standards, this manual contains information, cautions and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition. Service and adjustments should be performed only by service-trained personnel.

WARNING

ANY INTERRUPTION OF THE PROTECTIVE (GROUNDING) CONDUCTOR (INSIDE OR OUTSDE THE INSTRUMENT) OR DISCONNECTION OF THE PROTECTIVE EARTH TERMINAL IS LIKELY TO MAKE THE INSTRUMENT DANGEROUS. INTENTIONAL INTERRUPTION IS PROHIBITED.

8-16. Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

WARNING

WHEN THIS INSTRUMENT IS CONNECTED TO THE POWER MAINS, DANGEROUS VOLTAGES ARE ALWAYS PRESENT INSIDE THE INSTRUMENT. TROUBLESHOOTING PROCEDURES SHOULD BE PERFORMED ONLY BY SERVICE-TRAINED PERSONNEL WHO ARE AWARE OF THE HAZARDS INVOLVED.

8-17. Capacitors inside the instrument may still be charged even if the instrument has been disconnected from the power source.

8-18. Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the short-circuiting of fuseholders must be avoided.

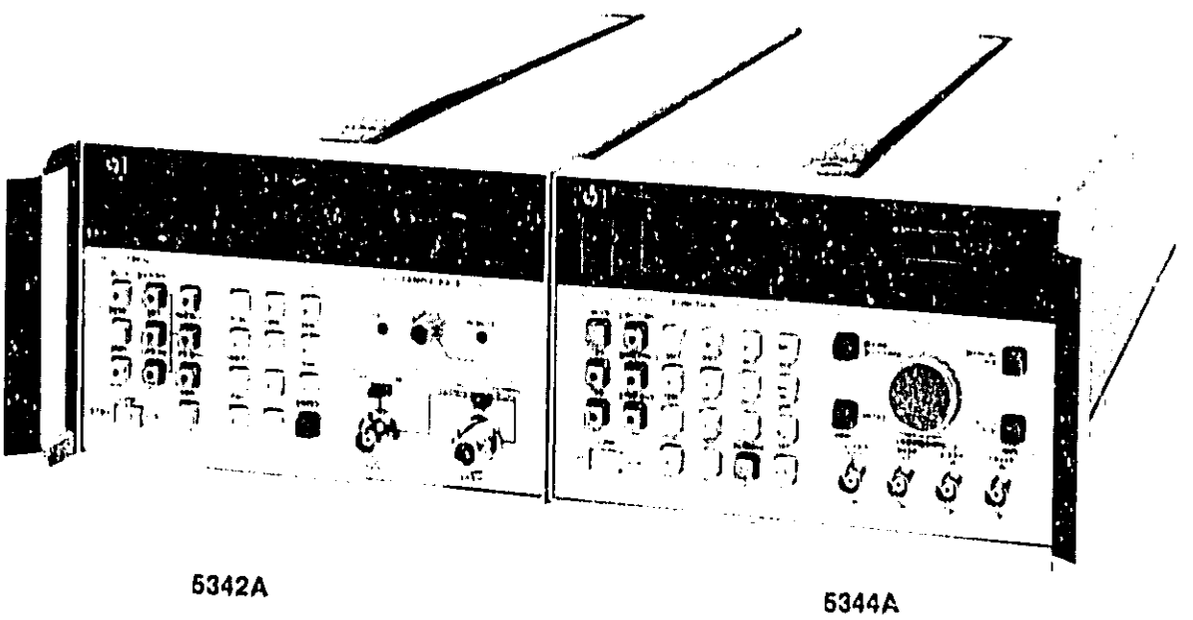


Figure 8-2. 5344A/5342A Front View

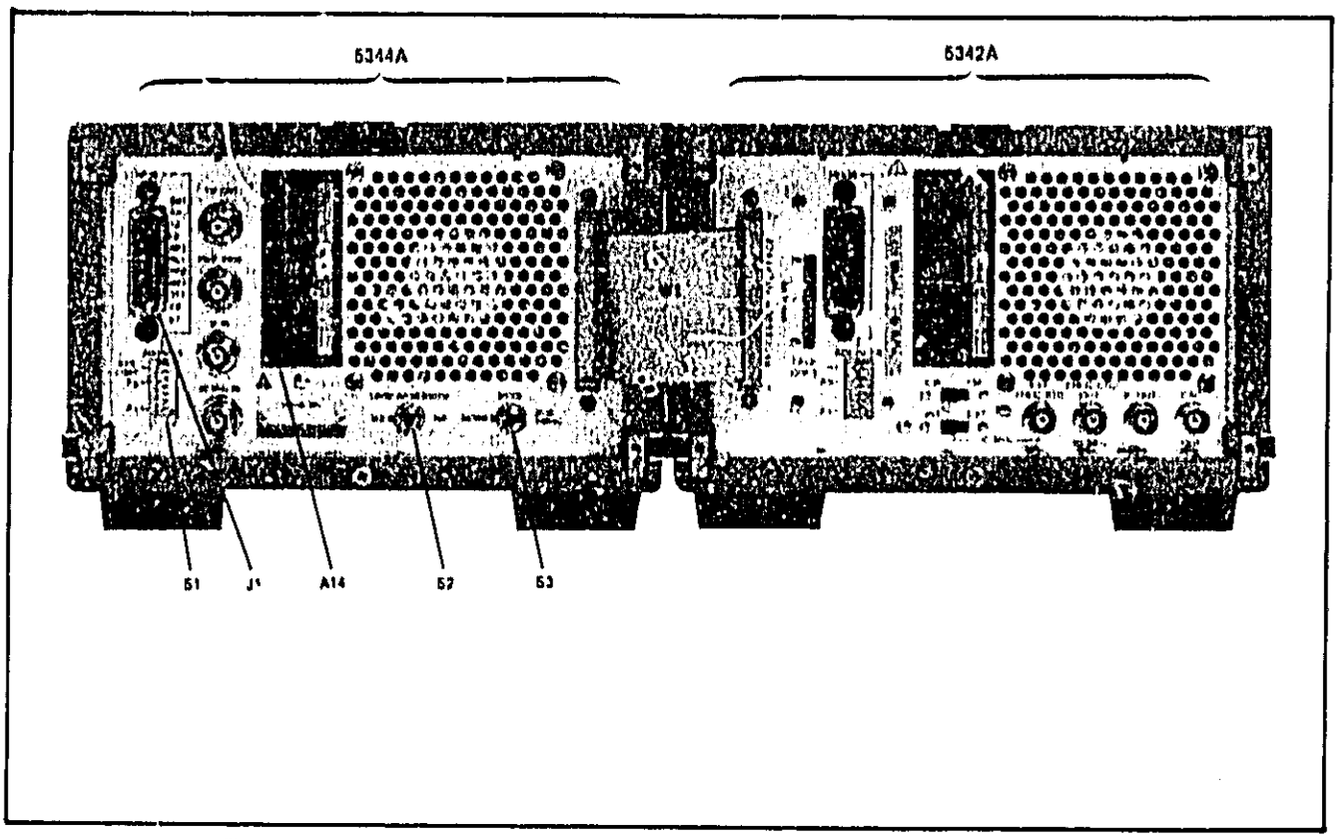


Figure 8-3. 5344A/5342A Rear View With Processor Interface Cable W1 Exposed

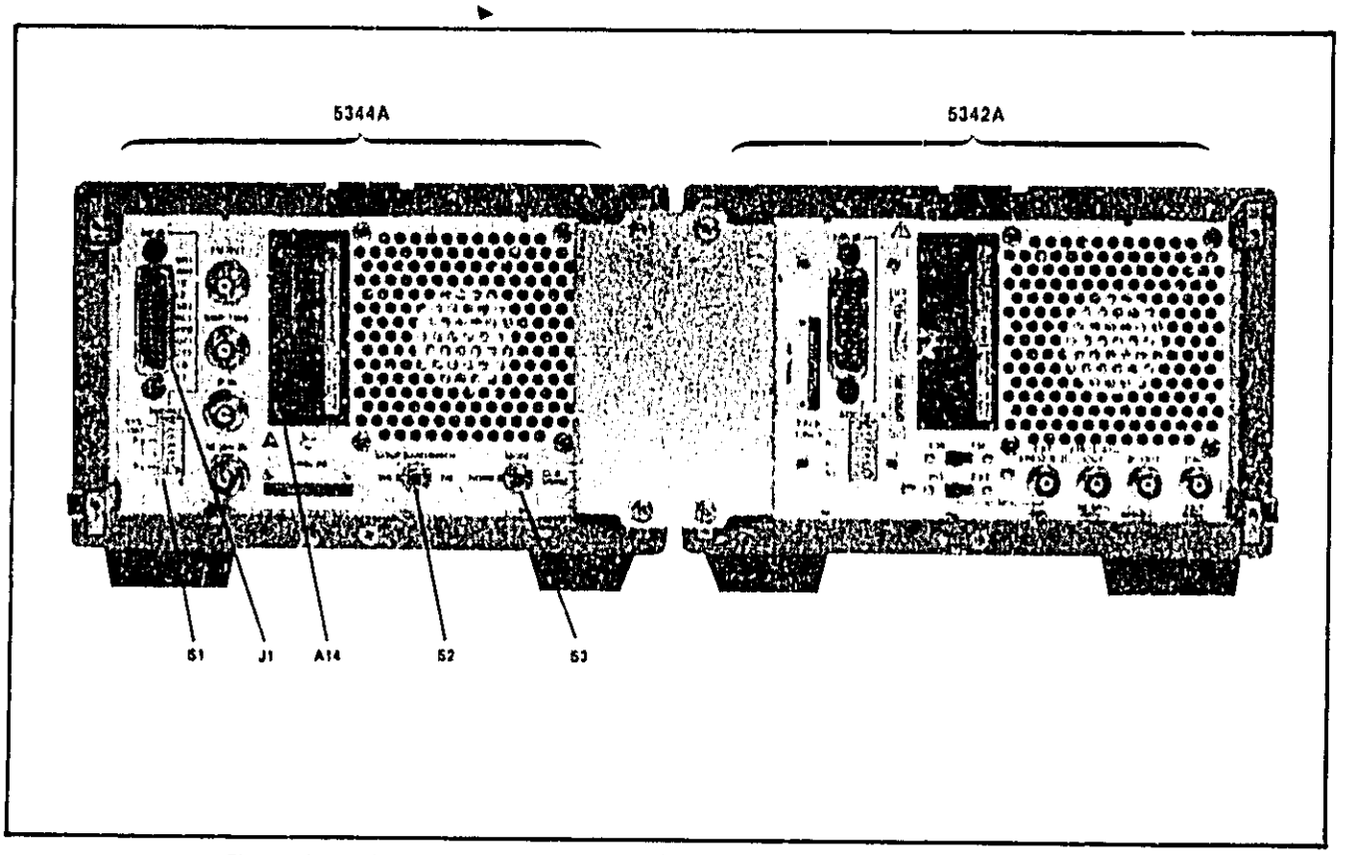


Figure 8-4. 5344A/5342A Rear View With Processor Interface Cable W1 Shielded

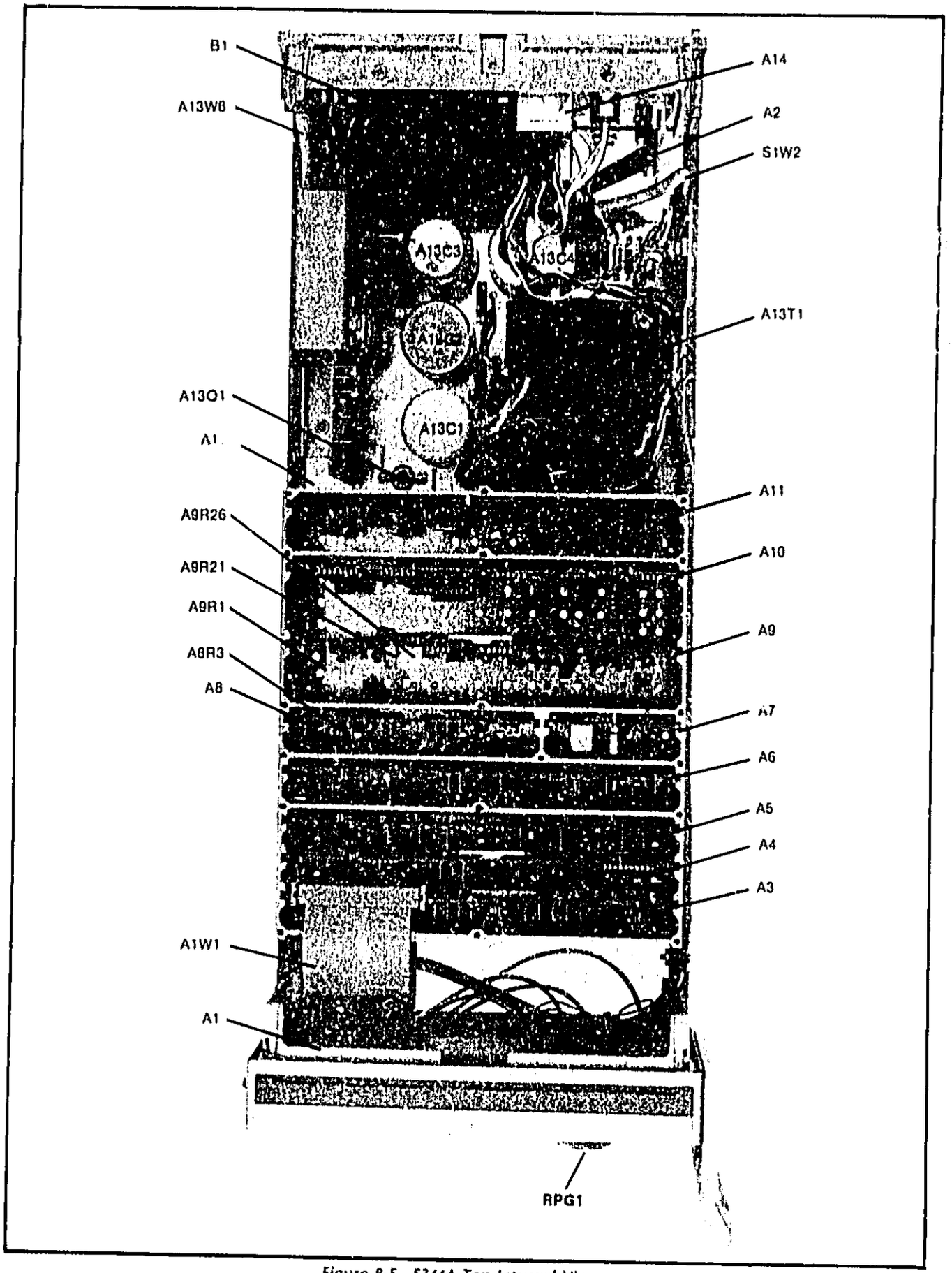


Figure 8-5. 5344A Top Internal View

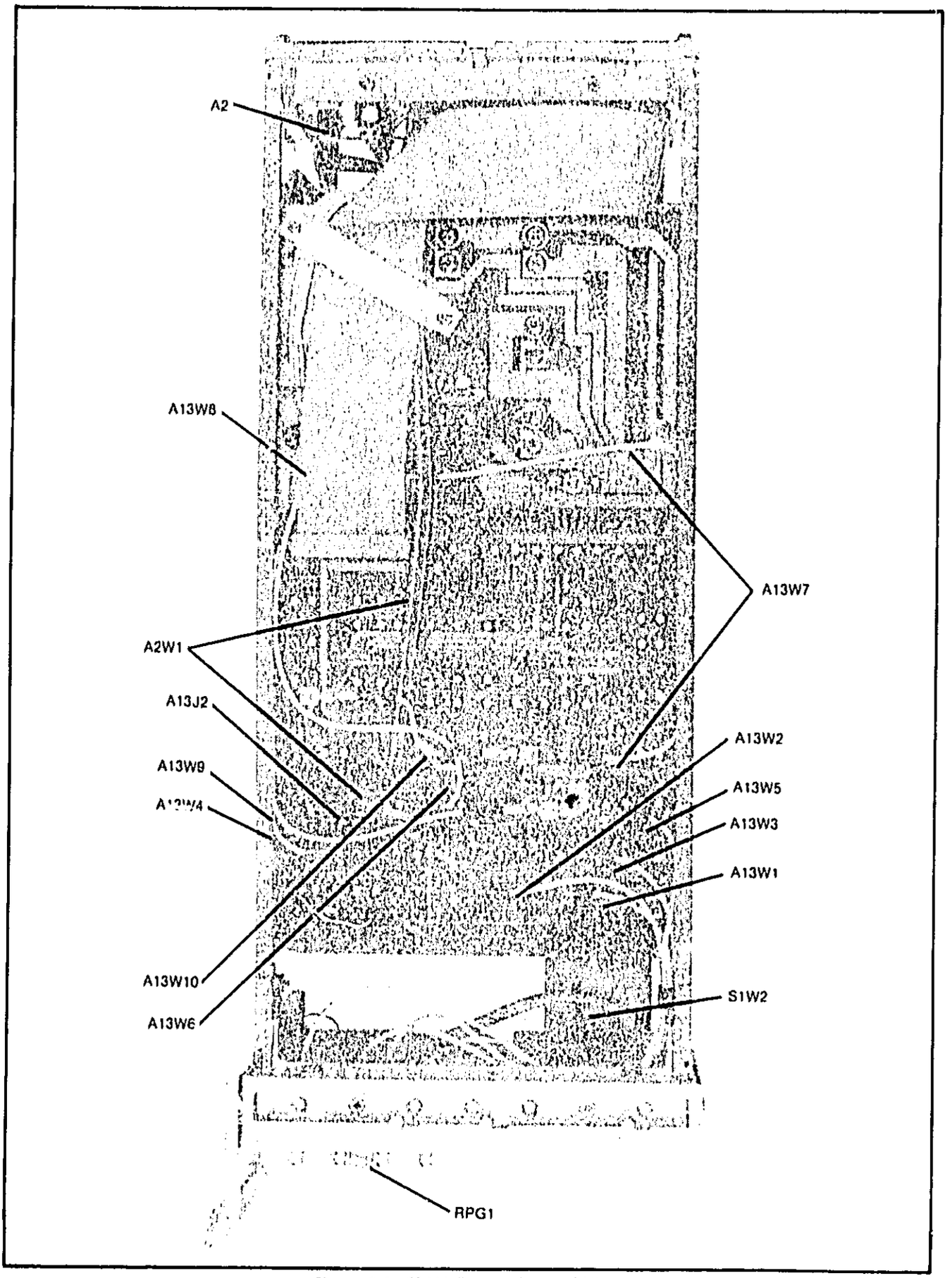


Figure 8-6. 5344A Bottom Internal View

NOTE

Prior to disassembly of the 5344A, the instrument should be separated from the 5342A (or 5343A) if attached. See *Figure 2-3* for details.

8-19. DISASSEMBLY AND REASSEMBLY

8-20. Before performing any of the disassembly or reassembly procedures, perform the following steps:

a. Set LINE ON-OFF switch to OFF position.

b. Remove line power cable from Input Power Module (A14).

8-21. Top Cover Removal

8-22. To remove the top cover, proceed as follows:

a. Place 5344A with top cover facing up.

b. At top rear of instrument, remove pozidrive screw from rear cap retainer and remove retainer.

c. Slide top cover back until free from frame and lift off.

d. To gain access to pc assemblies remove screws from top plate and remove plate.

8-23. Bottom Cover Removal

8-24. To remove the bottom cover, proceed as follows:

a. Place 5344A with bottom cover facing up.

CAUTION

IN THE FOLLOWING STEP, THE TWO FRONT PLASTIC FEET MUST BE REMOVED FROM THE BOTTOM PANEL TO AVOID DAMAGE TO INTERNAL WIRING.

b. Remove each of the two front plastic feet from bottom cover as follows: While lifting up on the tabs at the back edge of the plastic foot, push back on front edge of the plastic foot and pull the foot free from the bottom cover.

c. Loosen captive pozidrive screw at rear edge of bottom cover.

d. Slide bottom cover back until it clears the frame.

e. To replace the bottom cover, reverse the above procedures.

8-25. Front Frame and A1 Keyboard/Display Assembly Removal

8-26. To remove the front frame from the main housing of the instrument, proceed as follows:

a. Remove top and bottom covers as described in the preceding paragraphs.

b. Refer to the exploded view of the 5344A in *Figure 8-7* to remove the front frame, A1 Keyboard/Display board, and chassis parts.

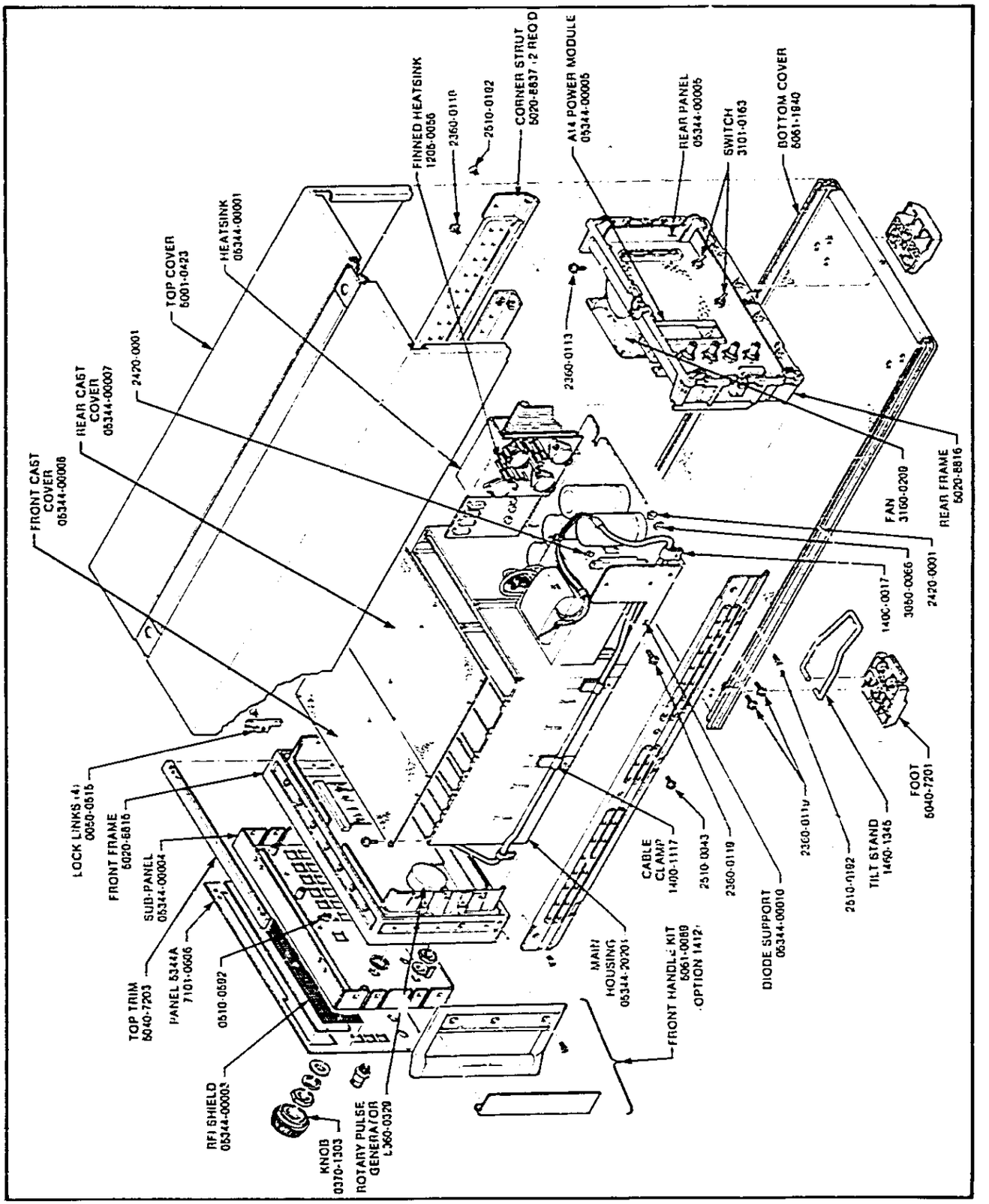


Figure 8-7. 5344A Exploded View

8-27. THEORY OF OPERATION

8-28. The HP 5344S Microwave Source Synchronizer improves the stability and frequency accuracy of a continuous wave (CW) or a swept microwave source. Compatible sources for use with the 5344S are listed in *Table 3-7.*

8-29. The 5344S is comprised of the 5344A Source Synchronizer and 5342A (18 GHz) Microwave Frequency Counter with an Option 001 Timebase and Option 011 HP-IB Interface. The 5344A and the 5342A are electrically and mechanically connected together at the factory before shipment. Refer to *Figure 2-3.* The 5344S Option 043 replace the 5342A with the 5343A (26.5GHz) Microwave Frequency Counter.

8-30. *Figure 8-8* is a simplified block diagram that shows the basic function of the 5344S. The RF output of the signal source is sent to the 5342A (or 5343A) where it is counted and down converted to an intermediate frequency (IF). The IF signal is supplied to the 5344A Source Synchronizer where it is divided by 2 and compared to a synthesizer generated signal which represents the source "lock" frequency. Any difference in phase between the two signals is applied to the source as an FM signal to correct for any difference from the desired phase, and lock the frequency in place.

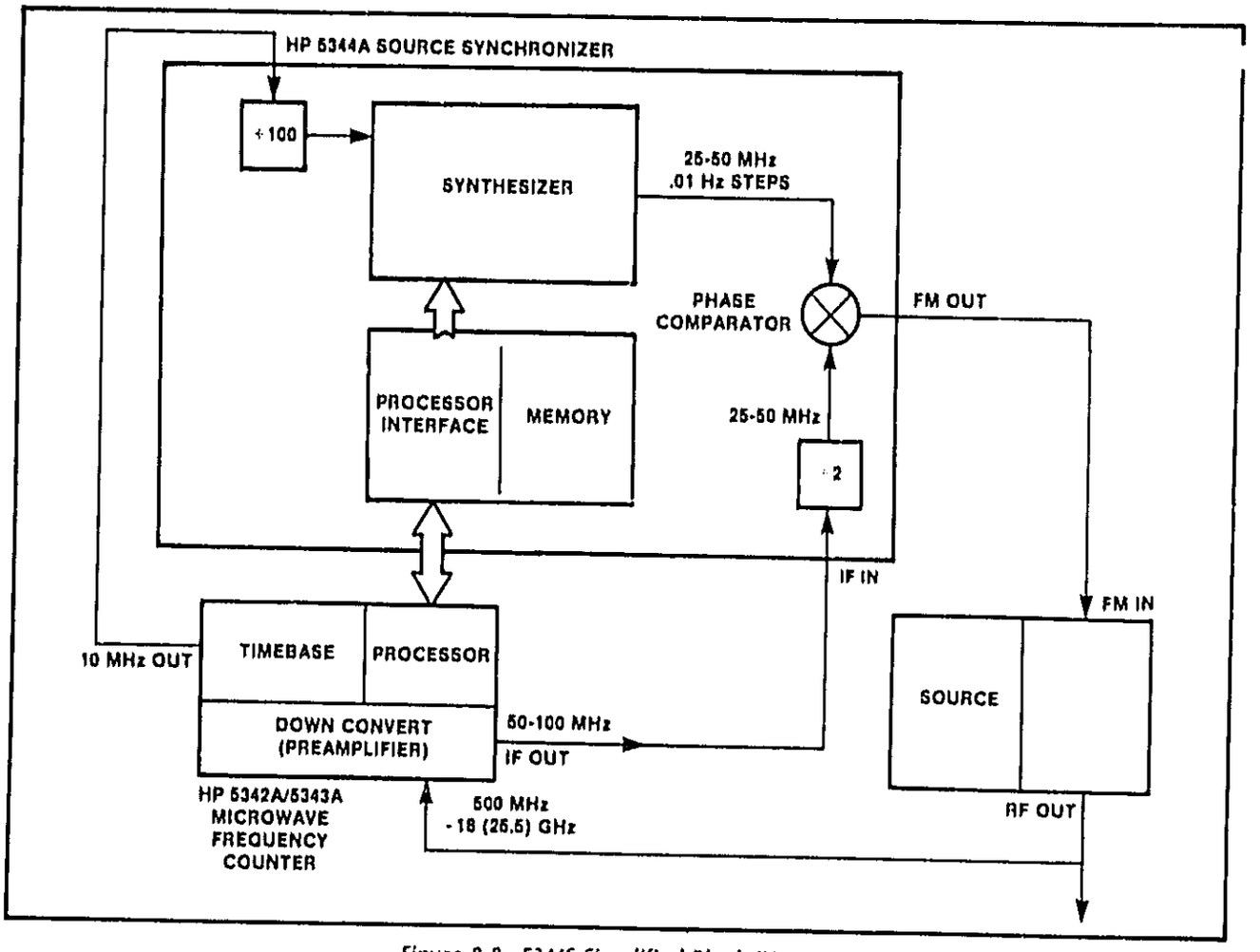


Figure 8-8. 5344S Simplified Block Diagram

8-31. The microprocessor in the 5342A (or 5343A) is used to control the 5344S and the program that controls the 5344A is contained in the ROM in the 5344A. The interface between instruments is provided by a 40-line ribbon cable connected between the rear panels. The 5344A receives the 10 MHz reference signal from the 5342A (or 5343A).

8-32. The IF output of the 5342A (or 5343A) is from 50 to 100 MHz. Since many different values of input frequency may cause an IF in this range, the 5344A calculates what the IF should be (based on the signal source frequency commanded), as well as which harmonic number (N) and synthesizer frequency will be used within the 5342A (or 5343A) to produce this IF. Refer to the theory of operation in the 5342A (or 5343A) manual for a description of harmonic heterodyne techniques. The IF output of the counter is a down-converted replica of the signal source output. This IF is sent to the 5344A where it is divided by 2 and sent to the phase comparator as shown in the functional block diagram, *Figure 8-9*. The comparator is operating at frequencies between 25 and 50 MHz.

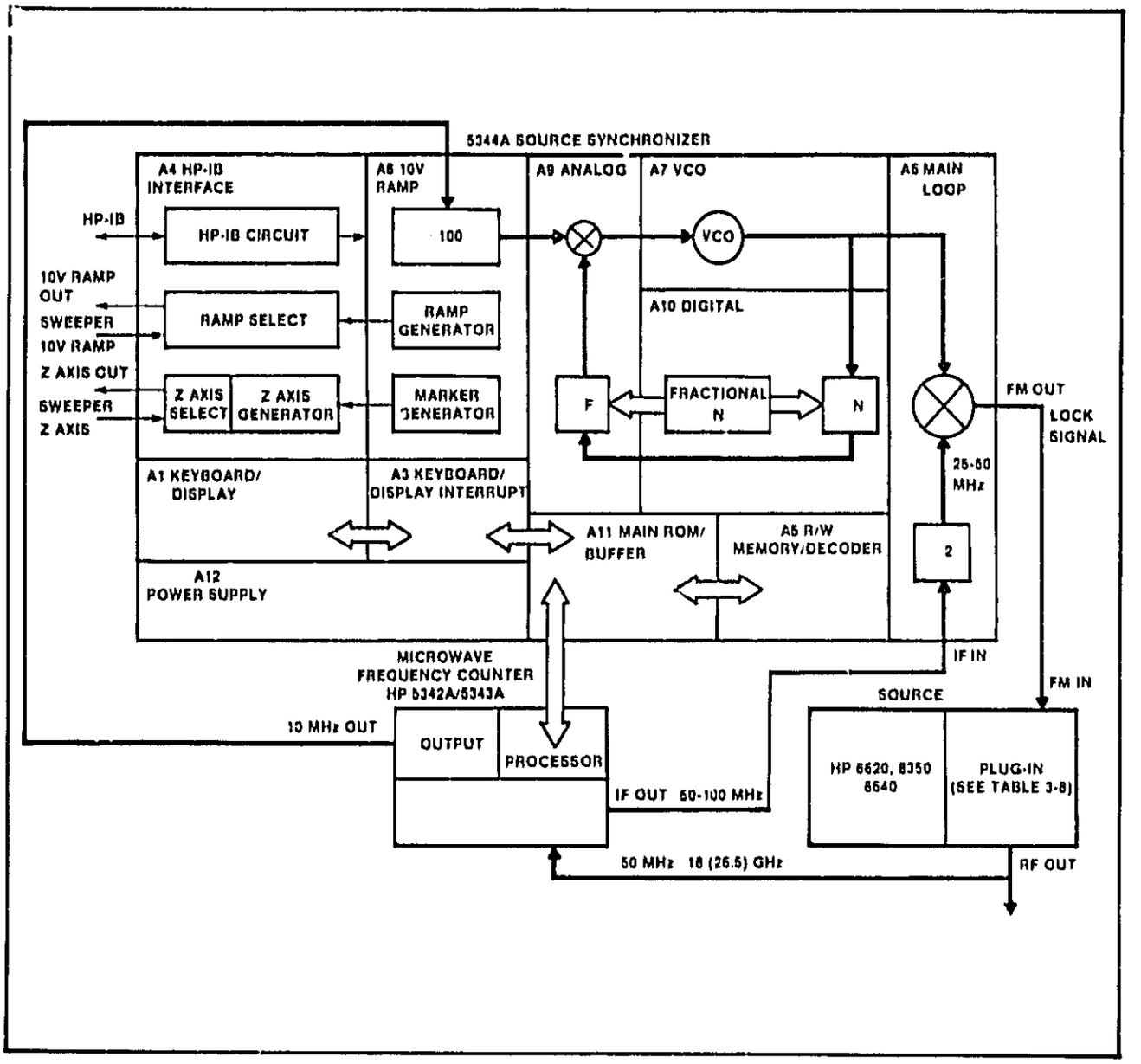


Figure 8-9. 5344S Functional Block Diagram

8-33. The reference signal to the phase comparator is the output of the fractional N synthesizer. As shown in the diagram, the fractional N synthesizer is contained on the A7 VCO, A9 Analog, and A10 Digital assemblies. Since this reference is a synthesizer capable of different frequencies, various functions may be controlled by the 5344A as described in the following paragraphs.

8-34. 5344A FUNCTIONS

8-35. The analog function performed by the phase lock loop described in the preceding paragraphs is controlled by the 5344A. The digital circuits receive front panel commands from the operator and provide information to the 5344A and the 5342A (or 5343A) to perform the required function. The digital circuits in the 5344A are extensions of the 5342A (or 5343A) and the interconnections are made via a 40-line bus cable connected between the rear panels as described in the preceding paragraphs.

8-36. Locked CW Output

8-37. The 5344A front panel is used to command the signal source to the desired frequency. The 5342A (or 5343A) performs an automatic measurement to determine the frequency of the source. From the frequency commanded, the 5344A calculates the value of N, the LO, the sideband, and the IF of the 5342A (or 5343A). The 5344A then sets the fractional N synthesizer to the frequency that represents the IF output of the counter when the signal source is present at the input and is exactly on frequency. When the output frequency of the signal source (which is tuned by the operator in the MANUAL MODE or by the 5344A HP-IB AUTO MODE) approaches the commanded frequency, the comparator in the A6 Main Loop Assembly is comparing the IF to the reference to generate the control voltage to lock the source right on frequency. (This output is labeled FM OUT as it is sent to FM IN of the source.)

8-38. Locked Sweep

8-39. In addition to generating CW signals with synthesizer accuracy, the 5344S adds the capability of phase locked (and phase continuous) sweeps of up to 40 MHz. Locked sweep commands the fractional N synthesizer to rapidly change its frequency, locking to the new frequency upon every change, to cause the entire phase lock loop to follow. Its output frequency may be swept across its full range while phase locked. As this frequency is swept, the phase detector applies a correction voltage to the source in an attempt to force it to follow in frequency and keep the phase error at zero. Since the locked sweep range is limited to the width of the 5342A (or 5343A) IF, only locked sweeps of 40 MHz or less may be implemented.

8-40. Lock and Roll Sweep

8-41. The 5344A establishes an accurate starting point for the signal source by using its locked CW capability. The source is then released to perform its sweep as commanded by the operator. When the source informs the 5344A of sweep completed, a relock to the start point is done, and the process repeats. During this mode of operation, the source provides the sweep ramp to drive a display or other device. The sweep width in this mode is limited only by the source capability.

8-42. HP-IB Interface

8-43. In addition to the functions described in the preceding paragraphs, the 5344A contains HP-IB interface circuits for operation on the Hewlett-Packard Interface Bus, in either of two functions, as follows:

a. System operation. The 5344 is connected to a controller (and possibly other devices) via HP-IB and the front panel controls are programmed remotely.

b. Standalone operation. The 5344 is connected to the source via HP-IB and acts as a controller. This mode accomplishes AUTO LOCK (available when 5344S is used with HP 8350A or 8620C, Option 011).

8-44. Block Diagram Description

8-45. The block diagram in *Figure 8-10* shows the assemblies (boards) of the 5344A and interconnecting lines and buses. In addition, all input and output signals and interface lines are shown.

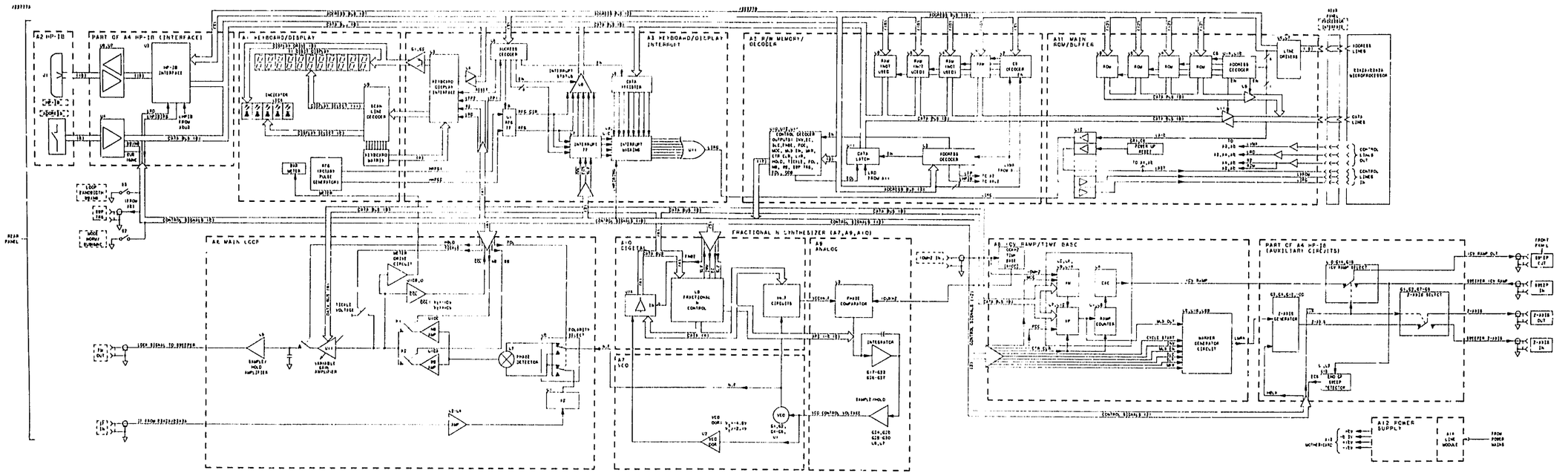


Figure 8-10. Detailed Block Diagram

8-46. The A1 Keyboard/Display board contains controls, indicators and associated circuits. The scan lines from the A3 Keyboard/Display Interrupt board are decoded on A1 for the display. The keyboard matrix drive lines are decoded and applied to the A3 board. The A1 board also contains the bar graph meter and rotary pulse generator which connects to the Interrupt Status Circuits on A3.

8-47. The A2 HP-IB board contains the HP-IB connector and switches which are connected via A13 Motherboard to A4 HP-IB Interface board.

8-48. The A3 Keyboard/Display Interrupt board contains display scan control circuits and interrupt circuits. The display strobing and keyboard scanning circuits are connected to the decoding circuits on the A1 board. An interrupt mask register is used to tell the microprocessor (in the 5342A or 5343A) what caused the interrupt. Causes for interrupts are HP-IB, keyboard, rotary pulse generator (RPG), timer, out-of-lock, sweep limit flag, and end-of-sweep. The timer and RPG circuits are also on this board.

8-49. The A4 HP-IB Interface board contains HP-IB circuits and auxiliary circuits required for z-axis select, ramp select, and z-axis generator. The HP-IB circuits process all handshake and data transfer functions between the HP-IB and the 5344A. The HP-IB address switch data (positions) are processed by the HP-IB circuits. The control and data lines to the external bus are connected via transceivers on A4 board. The z-axis select circuits select the output of the internal marker generator or the Z-AXIS IN connector. (The source instrument supplies the markers in lock and roll mode.) The ramp select circuits determine which ramp is sent to the SWEEP OUT connector. For locked sweep, the ramp from the generator on A8 is selected, and for lock and roll sweep, the source instrument is connected to the SWEEP OUT connector. The end-of-sweep detector circuit on A4 is used in lock and roll mode to signify that the sweep has ended. This action informs the 5344A to lock to the start frequency and initiate another sweep roll.

8-50. The A5 R/W Memory Decoder provides read/write memory and decoding. The decoding circuits provide all the control signals used within the 5344A. Address and data lines are connected from A11 Main ROM Buffer board to A5 and other boards as shown in the detailed block diagram, *Figure 8-10.*

8-51. The A6 Main Loop board receives the IF signal from the 5342A (or 5343A) via a rear panel connector. The IF is amplified, divided by two and phase compared with the synthesizer frequency (N.F) from A7 Voltage Controlled Oscillator (VCO) board. The resulting output is sent through a variable gain amplifier on A6 to provide the tuning voltage (FM OUT). The FM OUT signal is a dc correction voltage which is applied to the FM IN connector of the signal source being locked (tuned to the correct frequency).

8-52. The A7 Voltage Controlled Oscillator receives the fractional N synthesizer tuning voltage output from the A9 Analog board and develops the synthesizer frequency (N.F) which is sent to the divide-by-N circuit on A10 Digital board and the phase comparator circuit on A6 Main Loop board.

8-53. The A8 10V Ramp board generates a ramp to drive an external display. The ramp is sent to the ramp select circuit on the A4 board. The ramp is generated from the 10 MHz input from the rear panel connector. The 10 MHz input is also divided by 100 to provide the 100 kHz reference signal for the fractional N synthesizer.

8-54. The A9 Analog board compares the VCO ÷ N.F signal with the 100 kHz reference signal in a phase comparator. The output is sent through an integrator circuit and a Sample/Hold amplifier to provide the tuning by voltage for A7 VCO. symbol.

8-55. The A10 Digital board contains the Fractional N Control IC and the Divide-by-N Counter. The Fractional N Control IC calculates the divide-by-N data for the phase lock loop in the frequency synthesizer circuits. In addition, this IC increments or decrements the output frequency during a sweep function, outputs a Sweep Limit Flag when the start or stop frequency is reached, and outputs

a Sweep Limit Flag at the marker frequency during a sweep up. The Divide-by-N Counter is a presettable counter which divides the VCO frequency by N to provide the VCO ÷ N.F output to the phase comparator on A9 Analog board.

8-56. The A11 Main ROM/Buffer board buffers the 40-line bus signals to and from the 5342A (or 5343A). The ROMs on this board are connected to data bus drivers to allow separation of the data bus within the 5344A. The ROMs can be providing program information to the 5342A (or 5343A) while the 5344A data bus is in use for the functions occurring within the 5344A.

8-57. The A12 Power Supply board receives inputs from the power mains via A14 Power Line Module and the rectifiers on A13 Motherboard. This board provides regulated +5V,-5.2V, -5.2V, +15V, and -15V to the other boards in the 5344A.

8-58. DETAILED CIRCUIT THEORY

8-59. The following paragraphs cover the theory of operation of each of the assemblies (pc boards) in the instrument. A block diagram and a schematic diagram is provided for each assembly and the descriptions are listed in numerical order of the assembly reference designations, with the exception of assemblies, A1/A3 and A2/A4. These assemblies have interrelated functions and are described in functional order.

8-60. A1 Keyboard/Display

8-61. The keyboard and the display on A1 Keyboard/Display are controlled by A3 Keyboard/Display Interrupt board. As shown in the block diagram, *Figure 8-11*, the A1U9 Scan Line Decoder receives the scan lines HSL0-HSL2 and decodes these lines for the Display Drivers and the Keyboard. The Keyboard connects the return lines to A3U3 Keyboard Interface Display chip. A3U3 provides the display data via output lines HB0-HB3 and HA0-HA3. This data is supplied to the digit segments and to the annunciators, and is synchronized to the scan lines.

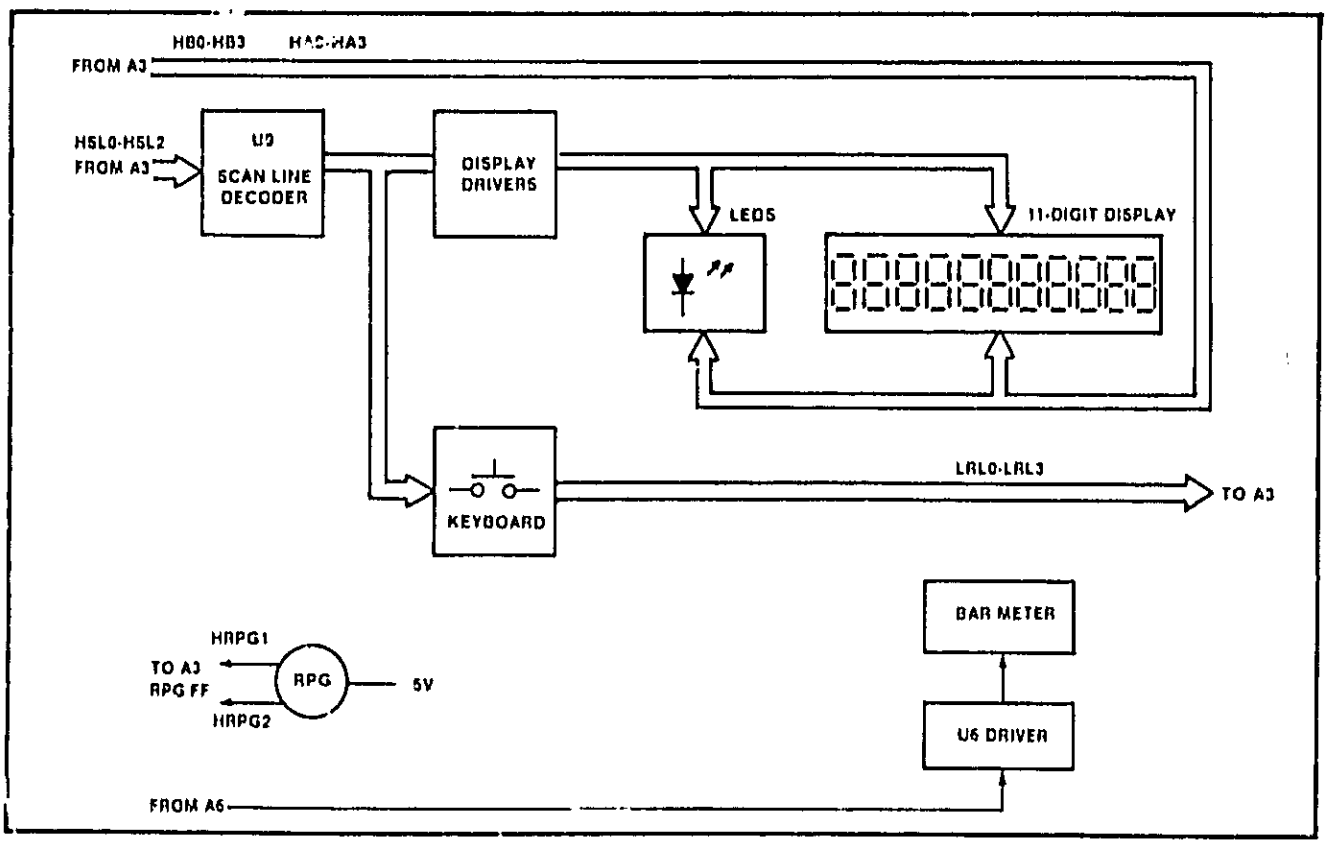


Figure 8-11. A1 Keyboard/Display Block Diagram

8-62. The return lines LRL0-LRL3 are connected through the keys of the keyboard to the scan lines. The pullup resistors to ±5V keep the lines high until a key is closed (pressed) to pull the line low. This action signals the microprocessor via A3U3 and the Data Bus. Refer to the schematic diagram, *Figure 8-25.*

8-63. The 10-segment, center scale bar graph meter mounted on this board indicates the frequency correction signal being applied to the source. The meter is driven by U6 Driver which is connected to the meter drive circuit on A6 Main Loop board.

8-64. The rotary pulse generator (RPG) is a tuning control that is used to adjust all 5344A parameters except the FREQUENCY MULTIPLIER. The RPG connects to the RPG flip-flop on A3 Keyboard/Display Interrupt board. The RPG flip-flop sends outputs via the interrupt and interrupt status circuits to the data bus for the microprocessor (in the counter) which controls the parameters of the 5344A.

8-65. A3 Keyboard/Display Interrupt

8-66. The A3 Keyboard/Display Interrupt board controls the A1 Keyboard/Display and contains circuits for the interrupt function. The Keyboard/Display Interface circuits are contained on one IC (U3) which controls display strobing and keyboard scanning. This IC also performs buffering and temporary storage to stack keyboard entries and to hold data for display. As shown in *Figure 8-12*, this board contains an Address Decoder, an Interrupt FF, Interrupt Mask, Interrupt Status Register, and an RPG FF. The circuits are described in detail in the following paragraphs.

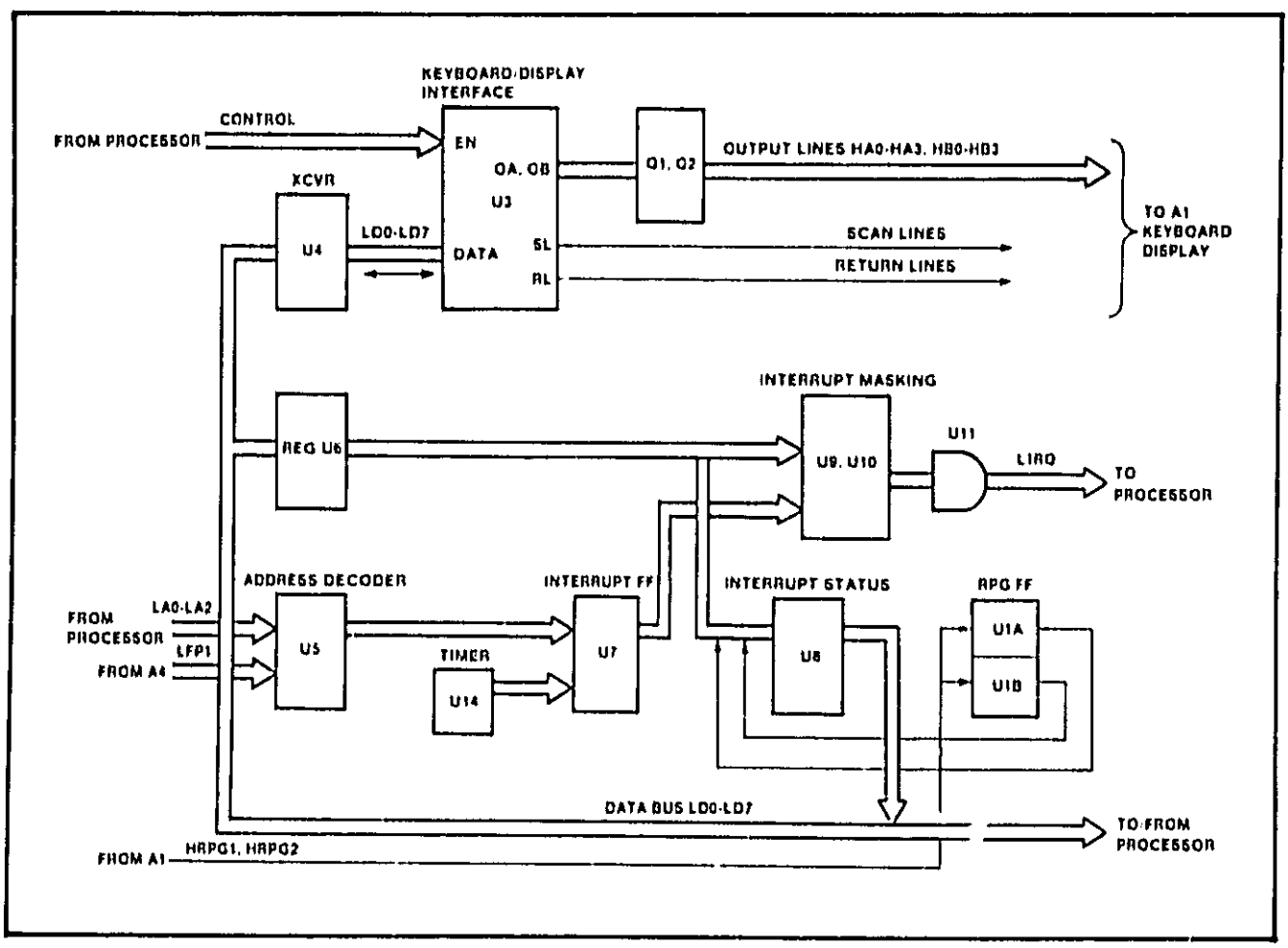


Figure 8-12. A3 Keyboard/Display Interrupt Block Diagram

8-67. KEYBOARD DISPLAY INTERFACE U3. As shown in the schematic diagram, *Figure 8-26*, this IC receives control signals from the microprocessor (in the 5342A or 5343A) via A11 Main ROM/Buffer assembly and the 5344A motherboard. Refer to A13 Motherboard Interconnect Diagram, *Figure 8-36*. (This diagram shows the connections of the 40-pin ribbon cable from the rear panel and the interconnections between assembly connectors on the motherboard.)

8-68. The control signals to A3U3 are the Chip Select, A0, Read, Write, and a Clock signal. The CS line enables the IC and is derived from the LFP2 (Low Front Panel 2) signal from the A5 board address decoder. The A0 line identifies the type of IC information. A logic zero is for data and a logic one is for command or status information. The Read and Write lines determine the direction of data flow. The IC will input with a low CS and low WR and will output with a low CS and low RD. The Clock signal is the Phase 2 clock from the processor.

8-69. The HB0-HB3 and HA0-HA3 outputs of A3U3 are sent through transistor arrays Q1 and Q2 to provide data to the display and the annunciators. The data is synchronized to scan lines SL0-SL3 which scan the display. The return lines (RL0-RL3) are connected to the scan lines on A1 through the keys on the keyboard to identify key closures for the processor.

8-70. The A3U3 Data Lines (D0-D7) connect through transceiver U4 to the data bus and through register U6 to Interrupt Masking U9 and U10, in addition to the Interrupt Status circuit U8.

8-71. Address Decoder U5 decodes Address Lines LA0-LA2 and is enabled by the output of Clock Generator U12 and LFP1 (Low Front Panel 1) signals. The outputs reset the Interrupt flip-flops in U7, reset A3U3, and clock U6.

8-72. Interrupt Flip-Flop U7 contains four flip-flops. The FFs are set by Timer U14, the Out-of-Lock (OOL) signal from A6 Main Loop board, End-of-Sweep (EOS) signal from the sweep detect circuit on A4, and the Sweep Limit Flag (SLF) from A10 Digital board, respectively. The U7 outputs are processed by U9, U10, and U11 to provide the Low Interrupt Request (LIRQ) to the microprocessor. The Timer interrupts act as a system clock for the 5344A, to allow the microprocessor to periodically check for switch settings and other instrument functions at 30 ms intervals.

3-73. Interrupt Status register U8 interfaces each type of interrupt to the data bus. This register informs the processor of the type of interrupt that is occurring. The rotary pulse generator (RPG) flip-flop (controlled by the knob on the front panel) sends outputs to U10 Interrupt Gating and U8 Interrupt Status, in the same manner as the other flip-flops.

8-74. A2 HP-IB Connector

8-75. The A2 HP-IB Connector board is mounted inside the rear panel and contains the HP-IB connector and address switch. Both of these components protude through the rear panel for access. The circuit traces on the board connect to jack J2 which is connected by cable strap A2W1 to J2 on A13 Motherboard. This board interfaces the HP Interface Bus and the address switches with the 5344A, as shown in the block diagram, *Figure 8-13*, and the schematic diagram, *Figure 8-27*.

8-76. A4 HP-IB Interface

8-77. The A4 HP-IB Interface board contains interface control circuits for HP-IB remote control of front panel functions of the 5344A. In addition, this board provides auxiliary circuits, such as Z-axis, Z-axis Select, 10V Ramp Select, and End-of-Sweep Detect, as shown in the block diagram, *Figure 8-13*.

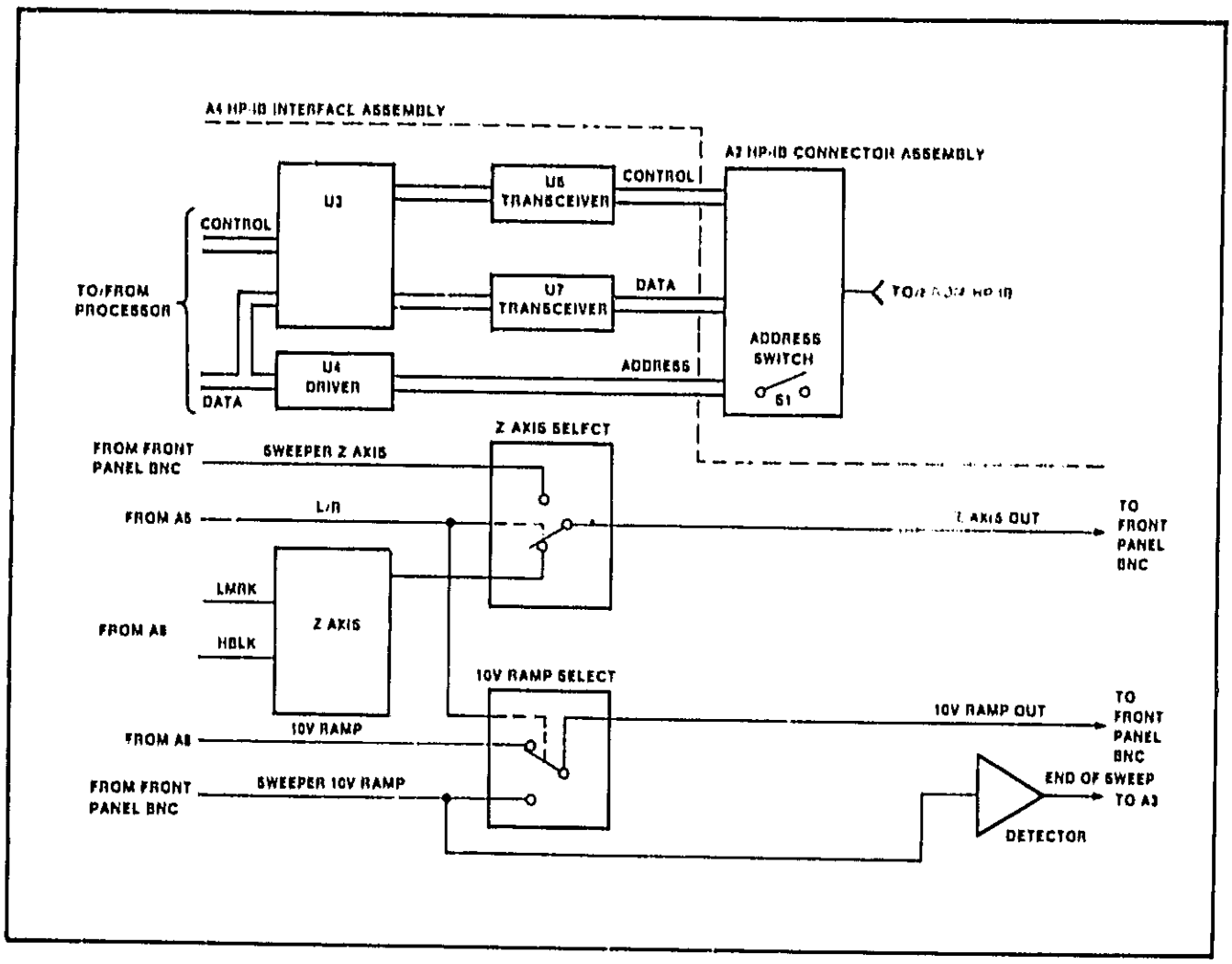


Figure 8-13. A4 HP-IB Interface/A2 HP-IB Connector Block Diagram

8-78. The address switches on the rear panel are connected via cable A2W1, A13 Motherboard and line drivers A4U4 to the data bus. This allows the processor to read the switch settings to determine the address of the 5344A. The HP-IB control lines and data lines are connected from rear panel HP-IB connector J1 via cable A2W1, A13 Motherboard and transceivers U6 and U7, respectively, to HP-IB Interface A4U3. The LHPIBIRQ signal is sent from A4U3 via the interrupt circuits on A3 to interrupt the processor (LIRQ).

8-79. The enable, reset, data flow directional control, and the phase 2 clock signals are sent from the processor through A11 Main ROM/Buffer assembly and A13 Motherboard to A4U3 as control signals. In addition, the LHPIB signal from the A5 board address decoder circuit serves as a chip enable. The signals from the processor may be traced by reference to the A13 Motherboard Wiring Diagram, *Figure 8-36.*

8-80. AUXILIARY CIRCUITS. In addition to the HP-IB circuits, the A4 board contains z-axis, z-axis select, ramp select, and end-of-sweep detect circuits. As shown in the schematic diagram, *Figure 8-27,* the Z-AXIS circuit receives the Low Marker (LMRK) signal and the High Blank (HBLK) signal from A8 board. The HBLK signal turns on transistor Q15 which turns off transistor Q4 to apply +5V to the non-inverting input of op amp U2D. This results in a +5V signal at the output of U2D when LMRK is inactive (High). The LMRK signal turns off transistor Q3 causing a -5.5V signal to be generated at the output of U2D when HBLK is inactive (Low). The output of this op amp is sent to the Z-axis select circuit. The Z-axis select and ramp select circuits are analog switches which are controlled by the state

of the Lock and Roll Select (L/R) signal input. When L/R is high, the 5344A Z AXIS OUT and 10V RAMP OUT are selected, and when L/R is low, the sweeper Z AXIS and 10V RAMP OUT are selected. The positive voltage output of U2D, when selected by analog switch JFET Q5, results in blanking of retrace lines and band switching transients. When LMRK is low, the negative voltage output of op amp U2D results in an intensified marker. The End-of-Sweep-Detect circuit consists of op amps U1A and B, U2A, B, and C, transistor Q16 and associated circuits. The op amps receive the SWEEPER 10V RAMP signal and detect the end of the retrace. This determines that the end of the sweep (in lock and roll mode) has been reached. The 5344A locks to the start frequency and initiates another roll. The End-of-Sweep (EOS) signal is sent to A3 board Interrupt FF.

8-81. A5 R/W Memory/Decoder

8-82. The A5 board contains a 1K read/write memory (RAM) circuit for the 5344A as shown in the block diagram, *Figure 8-14*. The A5 board also contains three different decoder circuits. The Control Decoders decode three of the address lines from the processor (in the counter) to provide all the command signals for operation of the other circuit boards in the 5344A. The Chip Select Decoder provides enable signals to the RAM. The Address Decoder decodes three lines from the address bus to provide enable signals to the Control Decoders and to the Data Latch. Unused positions are provided on the A5 board for the addition of RAM circuits.

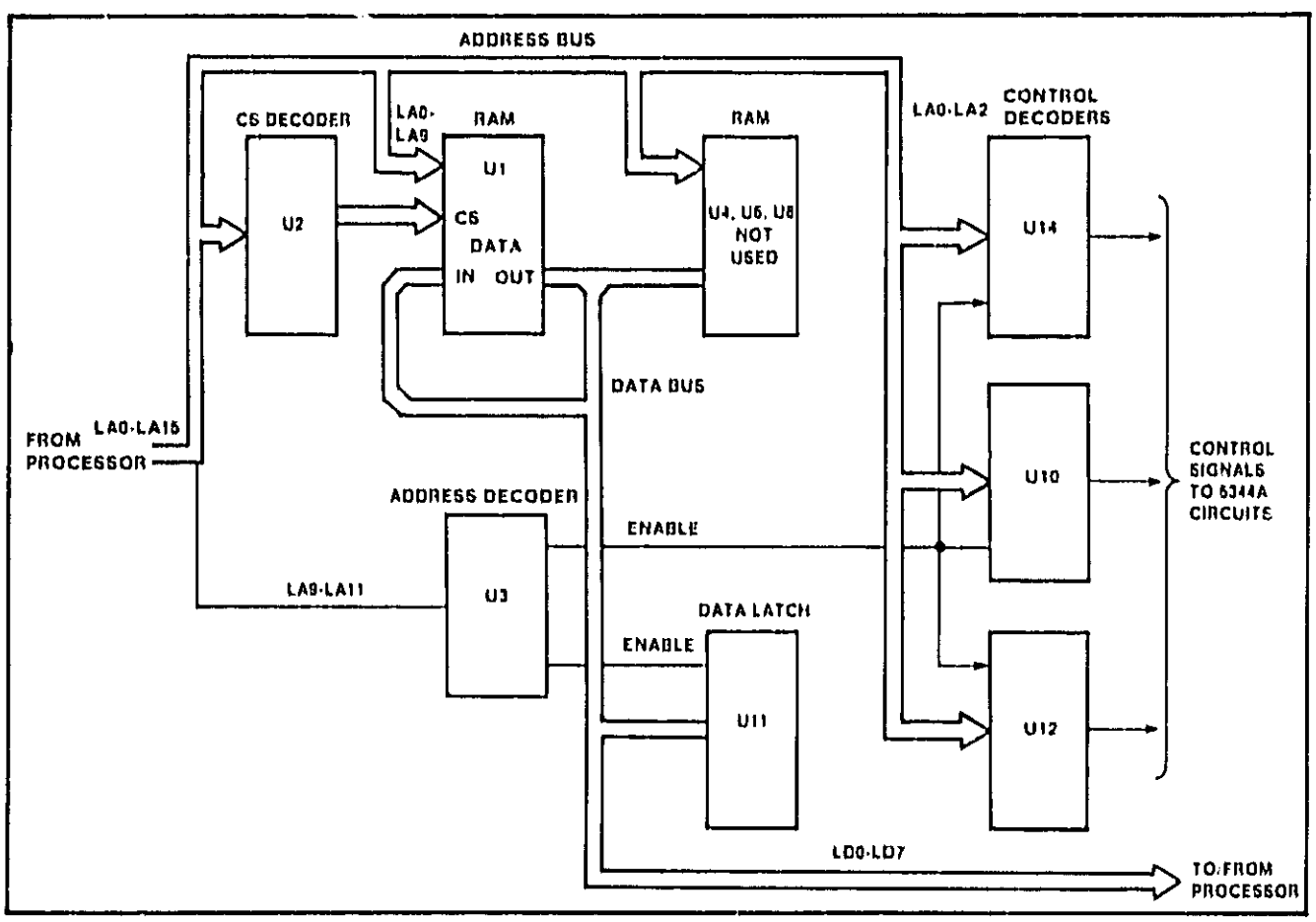


Figure 8-14. A5 R/W Memory/Decoder Block Diagram

8-83. The address lines LA0-LA15 (Low Address 0 to Low Address 15) from the processor are connected via A11 Main ROM/Buffer board and the traces on A13 Motherboard to A5 board inputs circuits. The LA0-LA9 lines are used for address location selection by the RAM, as shown in the schematic diagram, *Figure 8-28*.

8-84. The chip select lines for the RAM circuits are developed by Decoder U2 which is enabled by LA11 and LA12 lines. Combined input lines LA13-LA15 and LVMA are decoded to provide CS0,CS1,CS2, and CS3 select lines. The combined input lines LA13-LA15 and LVMA are also used to enable decoder U3. The address lines LA9-LA11 are decoded by U3 to provide the Low Front Panel 1 and Low Front Panel 2 control signals (LFP1 and LFP2) for the A3 Keyboard/Display Interrupt board and provide LHPIB to the A4 HP-IB Interface circuit. The functions of these signals are explained in the descriptions of the A4 and A5 boards. The four remaining outputs of decoder U3 are used to enable Control Decoders U10, U12, and U14. The Control Decoders receive address lines LA0-LA2 from the address bus and decode the binary weighted inputs to provide the command signals to control the circuits of the 5344A.

8-85. The Low Read (LRD) and phase 2 (Ø2) signals from the processor are received via A11 Main ROM /Buffer board to enable the RAM and Control Decoder circuits. The LRD signal is effective on the read cycle (read is in reference to the processor operation).

8-86. A6 Main Loop

8-87. The main function of A6 Main Loop assembly is to generate the correction voltage (FM OUT) which is applied to the tuning port of the source to maintain phase lock. This correction voltage is derived by comparing the phase of the IF signal from the 5342A (or 5343A) to a synthesized signal generated in the 5344A (N.F). Refer to the block diagram, *Figure 8-15*, and the schematic diagram, *Figure 8-29*.

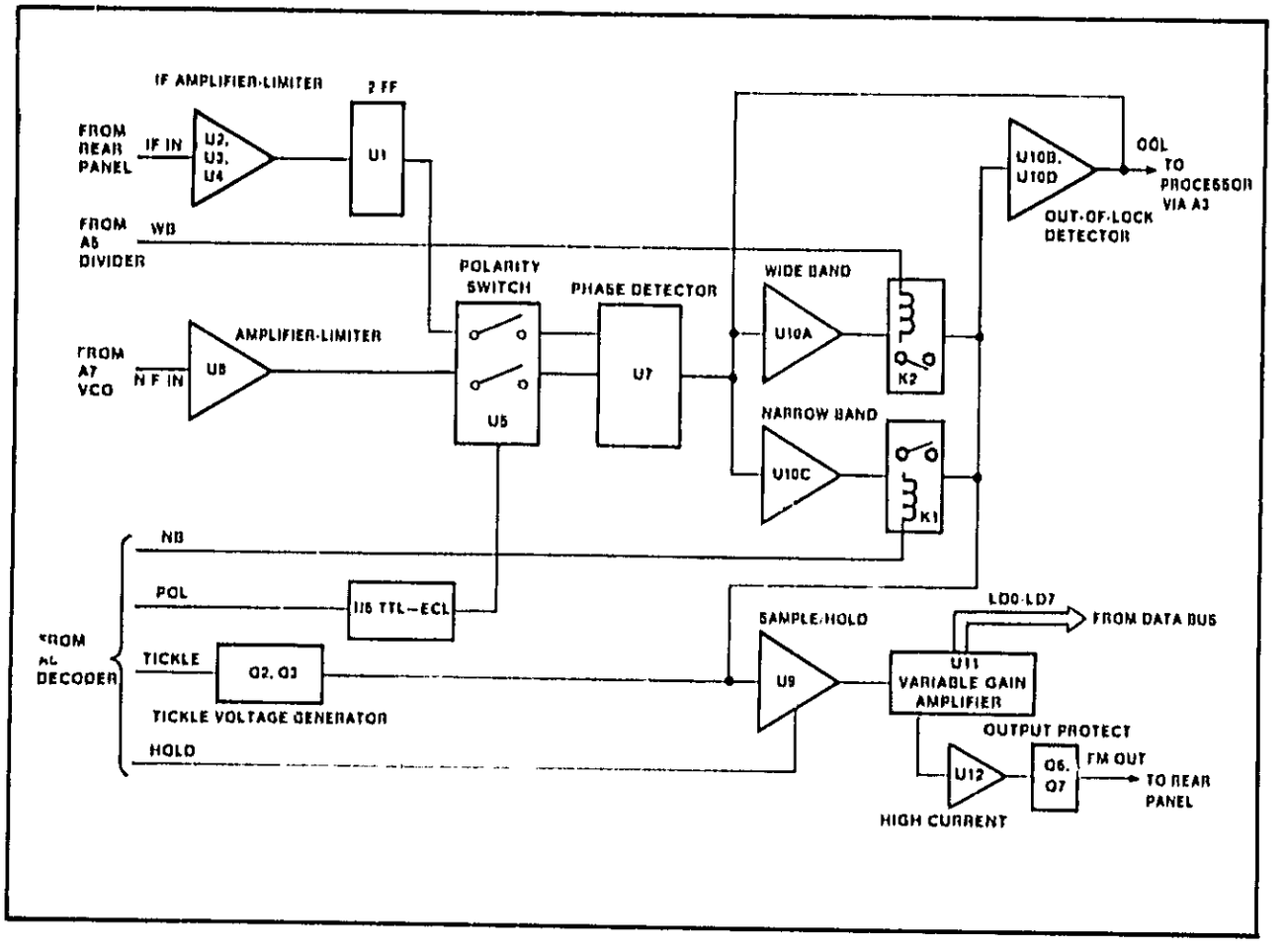


Figure 8-15. A6 Main Loop Block Diagram

8-88. The IF IN signal is amplified by three stages of gain (U2,U3,and U4). The IF is then divided by 2 in ECL FF U1 to match the frequency range with that of the N.F synthesizer input. The N.F IN signal is amplified and limited by U8. The signals are sent from U1 and U8 to quad ECL gate U5 which acts as a polarity switch, under control of the POLARITY (POL) signal. The POL signal from the A5 decoder circuits causes U5 to interchange the IF or N.F signal depending upon whether the counter is using upper or lower sideband and upon the polarity of the source response to the tuning voltage (positive or negative). POL is converted to differential ECL level by U6 and resistors R12-R17. The signal may be monitored at test point TP2. The outputs of polarity switch U5 are sent to the V and R inputs of Phase Detector U7. These signals are monitored at test points TP1 and TP3.

8-89. The output of Phase Detector U7 drives Wide Band Amplifier U10A and Narrow Band Amplifier U10C. The output of one or the other amplifier is selected by relays K1 or K2, depending upon the loop bandwidth desired. The relays are controlled by the processor in reponse to the setting of the rear panel LOOP BANDWIDTH (WB/NB) switch.

8-90. The loop amplifier output selected by the relay drives Sample/Hold Amplifier U9. When the HOLD signal is low, U9 acts as a gain of one, non-inverting amplifier. When the HOLD signal goes high, the output voltage is held constant until the HOLD voltage again goes low. This function is used in the lock and roll mode where the sweeper is locked at the start frequency then released for a wide sweep with the tuning voltage held constant. The output of the Sample/Hold Amplifier (-10 to +10 volts) is offset and scaled (0 to +4 volts) then sent to the meter on the front panel. The Sample/Hold input is monitored at test point TP5 and the output at TP6.

8-91. The output stage consists of digital-to-analog converter U11, (which is used as a variable gain amplifier), high current output amplifier U12, Q6 and Q7, and overvoltage protection circuit diodes CR6 and CR7. Variable gain amplifier U11 is connected to the processor bus which allows the gain to be set to any value between 10/256 and 255/256. This setting is used to compensate for the different tuning sensitivities of sources, which can vary from 1 MHz/volt to 50 MHz/volt. The output of U11 is a current from pin 1 which is at virtual ground (cannot be easily monitored on an oscilloscope). The high current output stage consists of op amp U12 and transistors Q6 and Q7. The output of this stage supplies feedback for U11. Fuse F1 and zener diodes CR6 and CR7 protect the output from the application of high voltages. The output (FM OUT) is the tuning voltage that is applied to the signal source being locked.

8-92. The output of the loop amplifiers (U10A and U10C) is monitored before input to the Sample/Hold amplifier by the Out-of-Lock Detector circuit, U10B and U10D. When the output of the loop amplifiers tries to exceed 10 volts in either direction, the detector output supplies a negative feedback to the inputs of the loop amplifiers to prevent any increase. In addition, transistor Q1 is turned on, sending Out-of-Lock (OOL) low to inform the processor that the loop is out of lock.

8-93. When the Tickle signal from A5 decoder is TTL high, transistor Q2 and Q3 are turned on to supply a known voltage (-190 mV) to FM OUT. This voltage is used to measure the tuning sensitivity of the source being locked.

8-94. A7 Voltage Controlled Oscillator (VCO)

8-95. The A7 VCO operates in conjunction with A9 Analog and A10 Digital boards to form a phase-locked loop synthesizer, as shown in the overall block diagram, *Figure 8-10*, and described in paragraph 8-113.

8-96. The VCO Control Voltage from the Sample and Hold amplifier on A9 Analog board is applied to the input of the VCO, as shown in the block diagram, *Figure 8-16*, and the schematic diagram, *Figure 8-30*. This voltage controls the VCO frequency by changing the capacitance of the varactors (voltage variable capacitors) CR1 and CR2. The varactors are part of the tuning circuit of the VCO, which is comprised of transistor Q1, Q2 and associated circuits. Variable inductor L1 is used to adjust the frequency of the VCO.

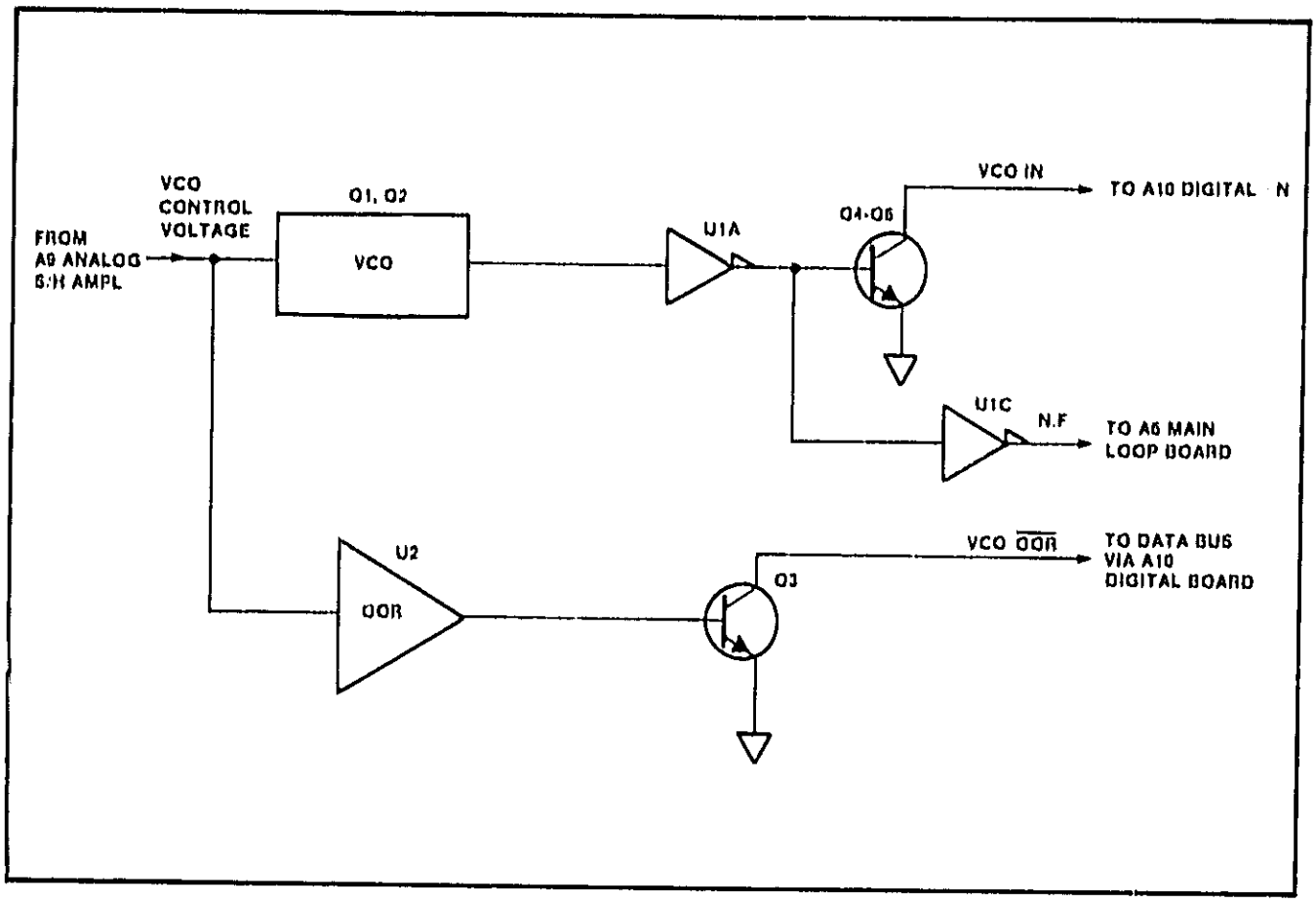


Figure 8-16. A7 VCO Block Diagram

8-97. The output of transistors Q1,Q2 is buffered by U1A and U1C to provide the N.F signal to the polarity select circuit on A6 Main Loop board. The output of U1A is sent through U1B and transistors Q4, Q5, and Q6 to provide the VCO IN signal to the divide-by-N circuit on the A10 Digital board.

8-98. The VCO Control Voltage input to the VCO is also supplied to op amps U2A and U2B which act as a comparator to determine changes in the VCO frequency that are out of the allowable range (25 to 50 MHz). When the VCO goes below 25 MHz (control voltage goes below -4.8V) the output of U2B is sent to transistor Q3, and when the VCO goes above 50 MHz (control voltage goes above +12.1V) the output of U2A is sent to transistor Q3. In either case, transistor Q3 is turned on to provide the Out of Range (OOR) signal to the data bus via A10 Digital board.

8-99. A8 10V Ramp/Timebase

8-100. The A8 10V Ramp/Timebase assembly generates a 0 to 10-volt ramp of from 10 milliseconds to 100 seconds in length. The ramp is used to drive an external display, only for locked sweeps (refer to paragraph 8-38 for a description of locked sweeps). For lock and roll sweeps, the source provides the sweep ramp for the display.

8-101. The 10-volt ramp is generated from the 10 MHz signal from the rear panel input which is also used to generate the 100 kHz Reference signal for the phase comparator on A9 Analog board (in the fractional N synthesizer). Refer to the overall block diagram, *Figure 8-10*, the A8 10V Ramp/Timebase block diagram, *Figure 8-17*, and the schematic diagram, *Figure 8-31*.

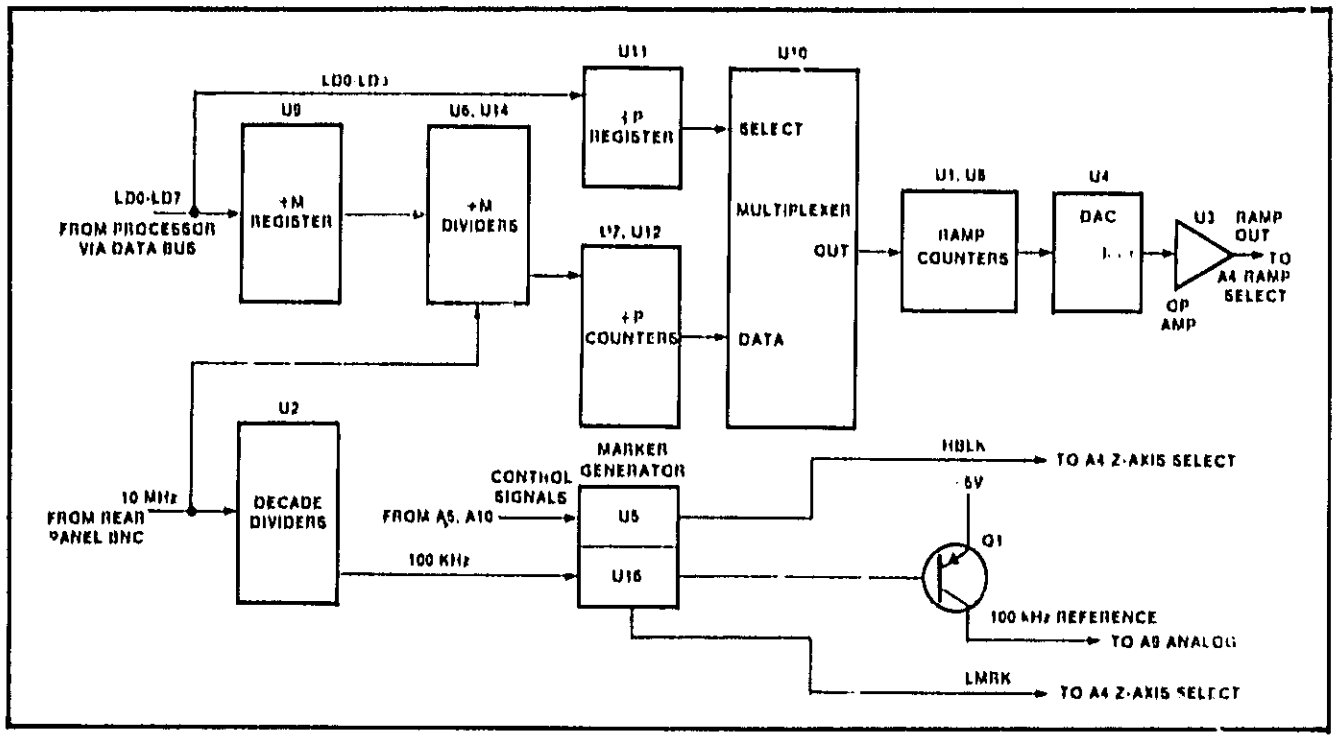


Figure 8-17. A8 10V Ramp/Timebase Block Diagram

8-102. RAMP GENERATOR. The ramp generator consists of four main circuits. Two of the circuits are divider circuits that are labeled Divide-by-M and Divide-by-P. The other two circuits are the Ramp Counters and a DAC circuit. The Divide-by-M circuit consists of programmed Register U9 and Divide-by-M counters U6 and U14. Register U9 is programmed by the LD0-LD7 data lines from the processor and controls the Divide-by-M counters U14 and U6, to divide by 100 or 200. The carry outputs of U6 and U14 are combined in nand gate U13A to clock Divide-by-P Counter U7A. Each flip-flop element in the Divide-by-P Counters (U7A,B and U12A,B) divides by 2, which allows a total division by up to 2 to the thirteenth power, since the division is cumulative.

8-103. The outputs of the Divide-by-P counters are sent to the data inputs of Multiplexer U10. One of these inputs is selected by the binary weighted select line inputs of U10 that come from the Divide-by-P latch U11, which is programmed by the processor via data lines LD0-LD3.

8-104. The M Data Clock (MDC) to U9 and the P Data Clock (PDC) to U11 come from the Control Decoders on A5 R/W Memory/Decoder. Data is clocked into U9 or U11 on the positive edge of the clock.

8-105. The clock input to the Divide-by-M Counters U6 and U14 is the 10 MHz input from the rear panel. Let's assume that the Divide-by-M circuit is programmed by the processor to divide by 100. The 100 kHz output from U13A will be applied to U7A and to the 0 data input of Multiplexer U10. Each flip-flop element of U7A,B and U12A,B will be the output of the preceding flip-flop divided by two, which will result in a different frequency applied to each data input (1 to 15) of U10. Each data input will be a different frequency that may be selected for output by the select inputs. For example, if the select input 2 at pin 14 of U10 is set high by the output of U11, data input 2 at pin 6 of U10 (25 kHz) will be selected for output and will be applied to the count input (pin 13) of counter U1B. The resulting accumulation of pulses by Ramp Counters U1B, U1A, and U8A are applied to the 1 to 10 inputs of Digital-to-Analog Converter (DAC) U4 whose output current is converted into a voltage by op amp U3. The output voltage is proportional to the number of pulses accumulated by the Ramp Counters. When they have accumulated 1000 pulses the DAC current is at a level that converts to 10 volts. Therefore, the ramp time is the time

required for 1000 pulses to arrive at the counter input. In the example, a 25 kHz input will generate a 40 ms ramp. The ramp is sent to the auxiliary circuits of the A4 assembly for ramp select. Refer to the overall detailed block diagram, *Figure 8-10.*

8-106. MULTIPLEXER ENABLE (MUX EN). The Mux Enable signal (from the Control Decoders on A5 board) goes Low to start the ramp, as shown in *Figure 8-18.* The ramp must be stopped (Mux En High) whenever the VCO is not sweeping, i.e., when the stop frequency is reached, or when in CW mode. After the ramp is reset at the end of a sweep, it will restart from zero when Mux En goes Low. This signal is also used to generate the HBLK signal for the Z-axis circuit on A8 board.

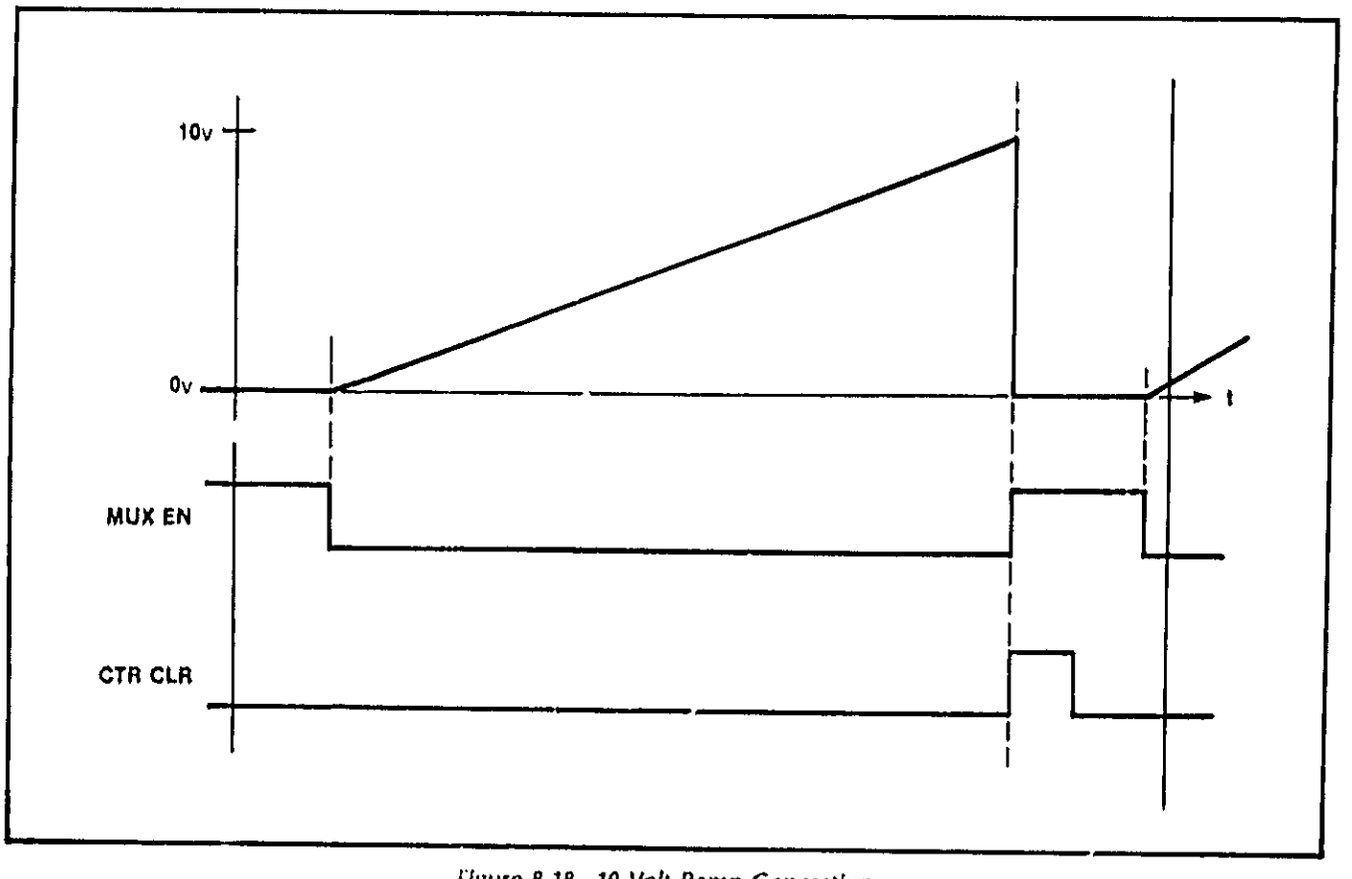


Figure 8-18. 10-Volt Ramp Generation

8-107. COUNTER CLEAR (CTR CLR). The Ctr Clr signal (from the Control Decoders on A5 board) goes high to reset the ramp by clearing the Ramp Counters as shown in *Figure 8-18.* The Ctr Clr signal must return to the Low state before the ramp can be restarted.

8-108. SWEEP LIMIT FLAG (SLF). The SLF is generated on the A10 Digital board by the Fractional N Control circuit. A negative-going edge on SLF indicates that a marker frequency or stop frequency has been reached. The SLF signal is supplied to the Marker Generator flip-flop U5 and the Mux En flip-flop U16.

8-109. SWEEP LIMIT CONTROL (SLC). The SLC signal (from the Control Decoders on A5 board) is used along with SLF to halt the 10V ramp at the stop frequency. The SLC signal goes High to enable SLF when the stop frequency is reached, but remains Low near a marker frequency so the ramp is not checked.

8-110. LOW MARKER (LMRK). The LMRK signal is a Low output from the marker generator circuit that indicates a marker frequency. The LMRK signal goes to the A4 board Z-axis auxiliary circuit. The LMRK signal is generated from the SLF and Multiplexer U10 output signals, and is enabled by MKR (Marker Control, from the Control Decoders on A5 board).

8-111. A9 Analog

8-112. GENERAL. The A9 Analog board operates with A10 Digital and A7 VCO boards to form the fractional N synthesizer circuit. This circuit provides the reference frequency for the phase locked loop that is used to control the frequency of a source. The circuits on the A9 board are designed to develop output frequencies that are other than whole number multiples (fractional parts) of the N.F synthesizer frequency. The overall block diagram, *Figure 8-10*, shows the function of the A9 board within the circuit.

8-113. As shown in the block diagram of the A9 board, *Figure 8-19*, the VCO/(N.F) signal from A10 is compared with the 100 kHz reference signal from A8 board in a phase comparator. The output of the comparator is sent through an integrator circuit to a sample and hold amplifier to develop the VCO Control Voltage. This voltage reflects any phase change between the two input signals. If the VCO frequency changes, the comparator output changes to correct the VCO, as part of a phase locked loop.

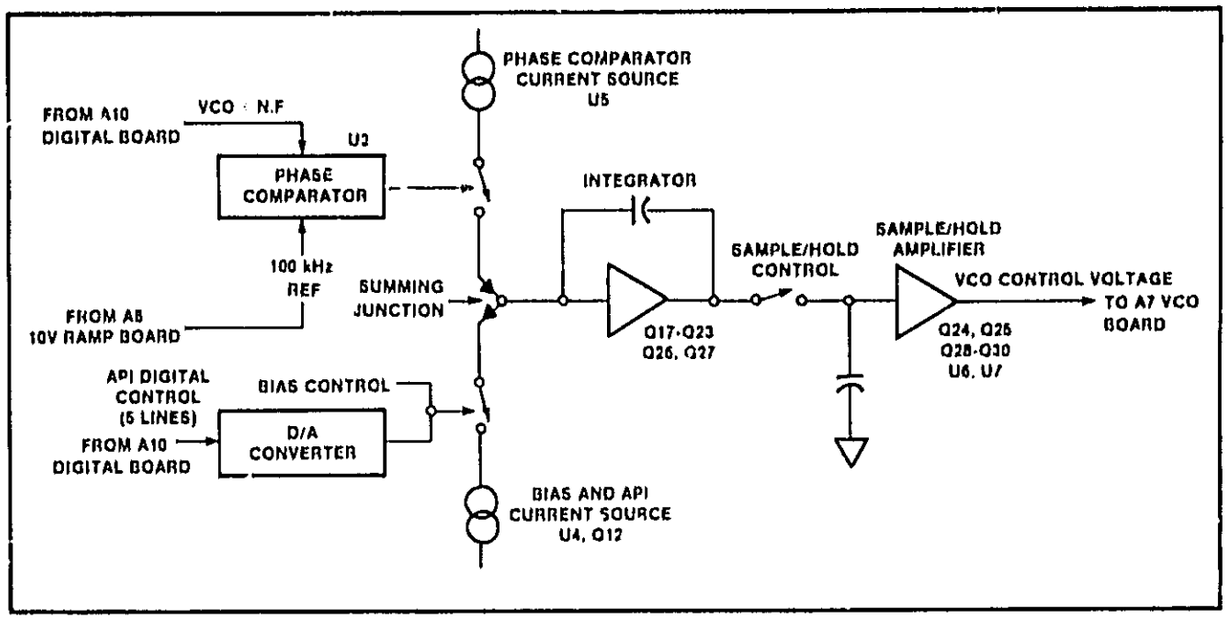


Figure 8-19. A9 Analog Block Diagram

8-114. DETAILED DESCRIPTION. As shown in the schematic diagram, *Figure 8-32*, the output of the A9 circuit is the VCO Control Voltage. This is the voltage captured by the Sample/Hold circuit and buffered by op amps U6 and U7. This circuit samples the output of the integrator circuit comprised of transistors Q17 through Q23, Q26, Q27 and associated components. Sampling of the integrator output is performed at the proper time and at regular intervals under the control of the Sample/Hold signal from Fractional N Control chip U8 on the A10 board. This signal turns on FETs Q24 and Q25 which act as a switch to connect the integrator output to the hold capacitors C29 and C25.

8-115. Ideally, the VCO Control Voltage output of the Sample/Hold circuit would be exactly the same at each sampling time and the VCO frequency would remain constant. Let's assume that this is true. In this case, the output of the phase comparator U3 would be a series of pulses of equal width. Each pulse causes current source U5, through FET Q9, to sink current from the integrator circuit. This causes a given amount of charge to be placed on integrator capacitor C24. At a specified time this voltage is stored on Sample/Hold capacitors C25 and C29. The integrator output waveform is shown in *Figure 8-20*. The up ramp represents the phase comparator charge, the flat top of the curve represents the Sample/Hold output (VCO Control Voltage), and the down ramp (discharge slope) represents the bias current which compensates for the the phase comparator portion.

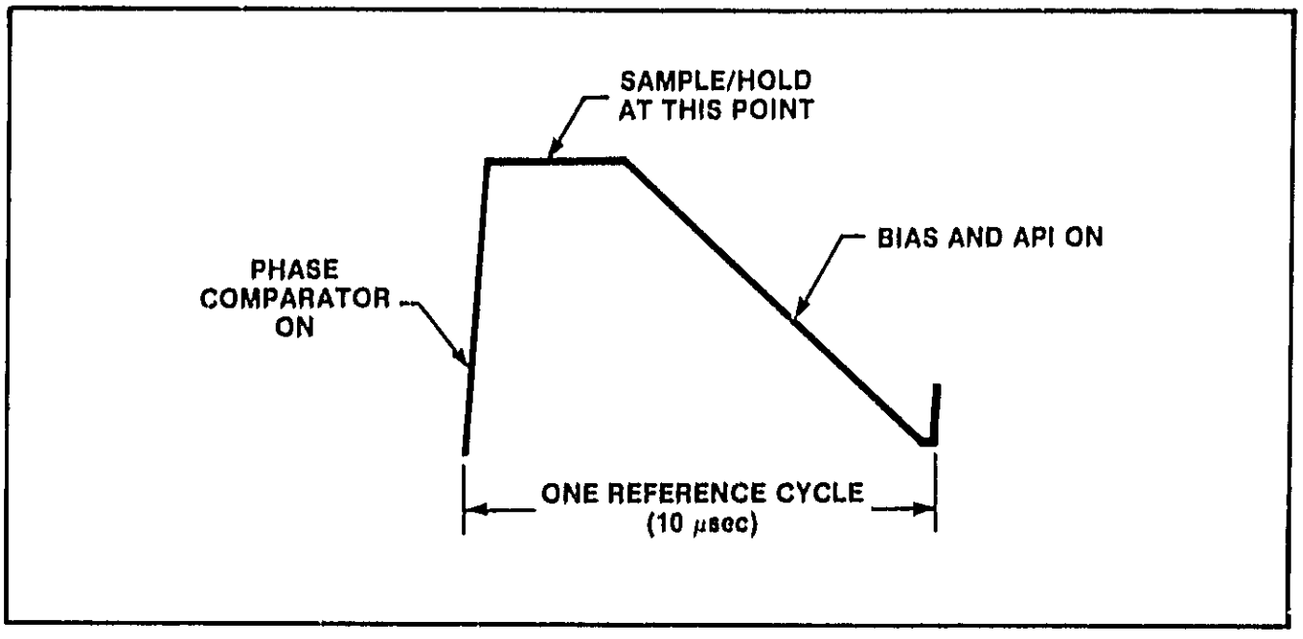


Figure 8-[illegible] Integrator Output Waveform

8-116. Immediately after a sample, the bias current source is turned on to discharge the integrator capacitor to the level it held before the phase comparator current was allowed to charge it. If this were not done, the charge would continue to accumulate to the limit permitted by the power supplies and remain at that level (nullifying the phase lock scheme). The bias current is controlled by a pulse from the fractional N control chip on A10 board. The charge slope increases the level and the discharge slope decreases the level of the output voltage. The charge slope is much greater than the discharge slope because the phase comparator current source has approximately ten times the magnitude of the bias current source.

8-117. BIAS CURRENT SOURCE. The bias current source for the integrator discharge current is comprised of op amp U4, FET Q12, and associated components. When the Bias signal from A9U1 is High, the transistor switch circuit Q3-Q5 turns off diode CR2, turns on FET Q10 and diode CR9. This connects the current source to the integrator through FET Q6, which is part of a current summing amplifier circuit. The summing amplifier consists of transistors Q1 Q2, Q6 and associated components. Thus, when the Bias signal is High, the integrator output curve will ramp down. When the Bias signal is Low, diode CR2 is on, FET Q10 and diode CR9 are off, and the integrator output curve does not ramp down.

8-118. The VCO operates over a range of 25 to 50 MHz. When the VCO output is processed by the divider circuits on A10 Digital board, the frequency is divided by a three-digit number which is referred to as the divide-by-N number. The divided signal is sent to Phase Comparator A9U3. For example, if the VCO frequency is 40 MHz, the divide-by-N number would be 400 to result in a 100 kHz input to the phase comparator (to be compared with the 100 kHz reference frequency, as described in paragraph 8-113). If it is necessary to change the VCO frequency by a fractional amount to become, for example, 40.04 MHz, the divided signal to the phase comparator would be 100.1 kHz to be compared with the reference. This would result in an increasing phase comparator charge current to the integrator. To compensate for this increased charge, the discharge current from the bias source is adjusted by means of Analog Phase Interpolation (API) information from the fractional N control IC A10U8. The phase difference between 40.04 MHz and 40.00 MHz is accumulated digitally in the control IC and applied through five lines to register A9U1. This register and associated circuits comprise a digital-to-analog converter (DAC). The DAC output current is subtracted from the bias current to discharge the integrator to the proper level during each sampling period, effectively cancelling the increased charge from the phase comparator.

8-119. ANALOG PHASE INTERPOLATION (API). The phase difference caused by the fractional frequency deviation of the VCO frequency is accumulated digitally in the fractional N control chip A10U8. Each of the five output lines (API1-API5) connects through API register A9U1 (API2-API5) or FF A9U2 (API1) to a current source. The API1, API2, and API3 lines each use a transistor as a switch to turn on a diode to connect a current source within U5 to the summing amplifier FET Q6. The API4 and API5 lines connect through resistive dividers to the power supply as the current source. Each of the API current sources connects into the current path between the bias current source (U4,Q12) and the summing amplifier (Q6) to the integrator circuit. For example, in the API3 line, the transistor Q8 turns on diode CR5 and connects the current source, U5, pin 11 through the 600 Kohm resistor in R27A to FET Q6 in the summing amplifier. The API1, API2, and API4 circuits contain variable resistors R21, R26, and R1, respectively, to allow adjustment of the current applied to the compensation circuit. Adjustment procedures are given in Section V.

8-120. The compensation problem is not completely solved, however, by the technique described in paragraph 8-119. If the phase locked loop were to continue to operate in this manner, the phase comparator output would continue to increase beyond practical limits. To prevent this, a "pulse remove" technique is used, as explained in the A10 Digital board circuit description, in paragraph 8-121.

8-121. A10 Digital

8-122. As described above in the A9 Analog board description, the A10 Digital board is part of the fractional N synthesizer phase locked loop. As shown in the block diagram, *Figure 8-21*, and the schematic diagram, *Figure 8-33*, the A10 Digital board contains the divide-by-N counters and the fractional N control circuits. The output of the VCO is controlled by changing the divide-by-N number which changes the divided VCO input to the phase comparator. The divide-by-N number is determined by control circuits in response to front panel or remote programming.

8-123. The VCO frequency is sent from A7 VCO to the A10 Digital board to be divided by N. If the VCO frequency is 40.04 MHz, for example, the divide-by-N number 400.4 would be referred to as divide by N.F (fractional N). The number 400 is represented by N, and the fraction .4 may be called F. Since the existing phase lock system will not allow divide-by-N to be four digits, some additional circuits are required to make the synthesizer operate at a frequency of 40.04 MHz. These circuits are the digital-to-analog converter (described above in paragraph 8-118) and the pulse remove circuit shown in *Figure 8-21*. To prevent the phase comparator (A9U3) output from increasing beyond practical limits, (as described in paragraph 8-120) the "pulse remove" technique is used. In effect, the accumulated phase difference (in the fractional N control IC A10U8) causes the divide-by-N counter to count one extra cycle (divide-by-401) each time the phase accumulator passes through unity. This has the effect of removing a cycle of VCO frequency and the divided signal to the phase comparator is now an average of 100 kHz.

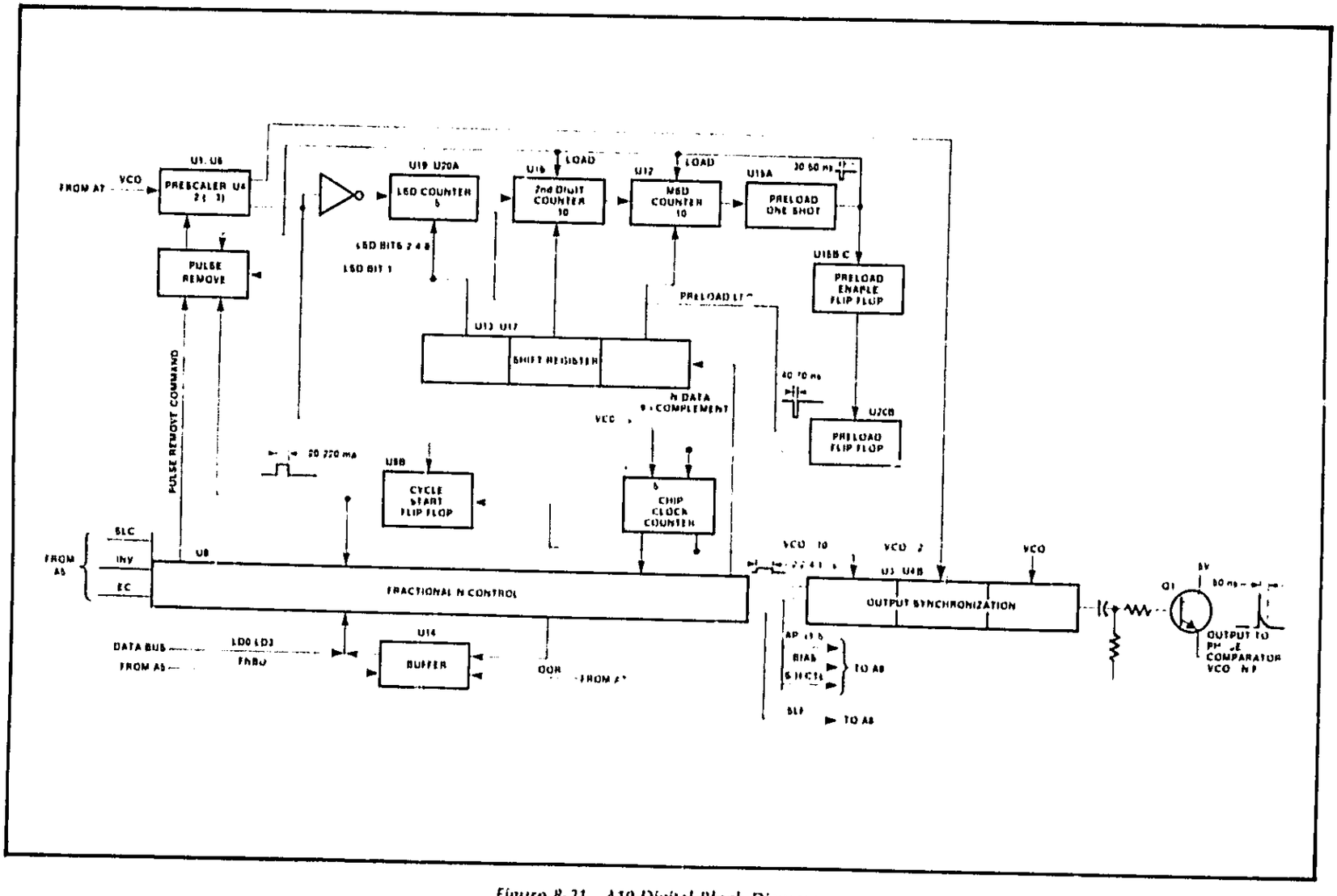


Figure 8-21. A10 Digital Block Diagram

8-124. To accumulate the phase difference within the fractional N control IC (A10U8), the twelve least significant digits in an internal frequency register are added to the twelve digits in a phase accumulator and the sum is stored again in the accumulator. This addition takes place every 10 microseconds (once for each cycle of the 100 kHz reference). *Figure 8-22* shows the process for this example.

8-125. The Frequency Register in *Figure 8-22* shows a divide-by-N number of 400 and a fractional N of .4. If the fractional part was .04, both the phase comparator output and the phase accumulator content would increase at one tenth the previous rate. As another example, if the fractional N was .9, a pulse remove command would be required for every nine out of ten reference cycles. The Frequency Register and the Phase Accumulator (including API Control) is added as illustrated to initiate a pulse remove command to the Pulse Remove circuit shown in the block diagram, *Figure 8-21*.

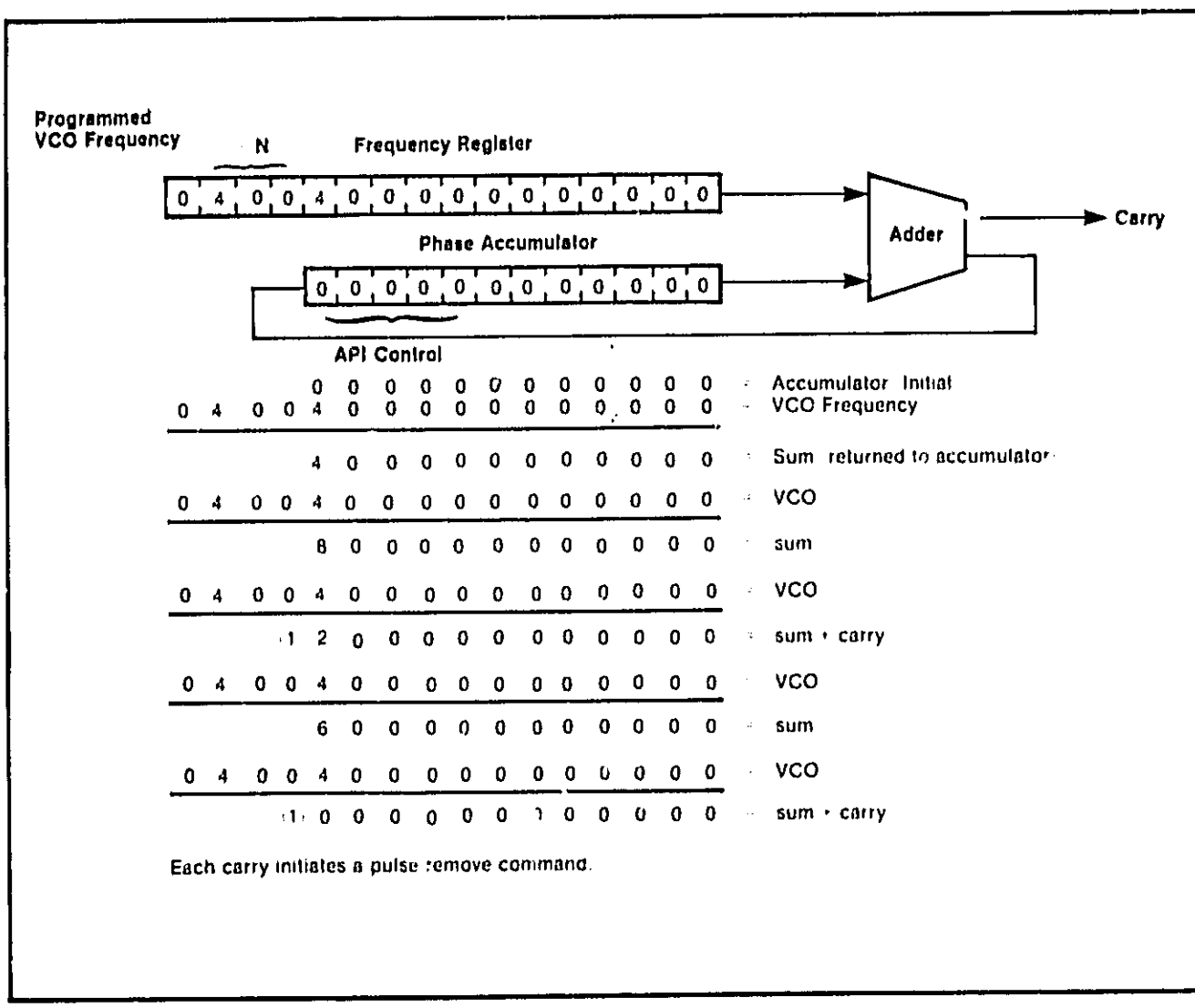


Figure 8-22. Phase Accumulation

8-126. FRACTIONAL N COUNTER. The divide-by-N (Fractional N) counter consists basically of three presettable counters in series, shown in *Figure 8-21*. The counters for the two most significant digits (of the three-digit divide-by-N number) are decade counters. The least significant counter consists of a divide-by-five counter and a divide-by-two prescaler which can be controlled to divide-by-three as necessary. Presettable counters are used because divide-by-N must be variable, as explained in the following paragraph.

8-127. The preset number that is loaded into the counter in BCD (binary coded decimal) form is the nine's complement of the divide-by-N number. Divide-by-N is determined by the first three digits of the VCO frequency. For example:

	Example 1	Example 2
VCO Frequency	40 000 000.0 Hz	30 100 000.0 Hz
Divide-by-N	40 0	30 1
Subtract divide-by-N from 999 (in A10U8) to determine the 9's complement	999	999
Divide-by-N	400	301
9's complement	599	698

8-17 The divide-by-N counter begins at the preset number (599 in example 1), counts to 999 and then reloads the same number unless a new frequency has been programmed. One output pulse occurs for each time the counters reach 999. Consequently, if 400 VCO cycles (599 to 999) are counted for every output pulse, VCO has been divided by 400. The output pulse is derived from the bias pulse issued by fractional N control IC A10U8. To provide the proper stable relationship to the VCO signal, this pulse is clocked first by VCO ÷ 10, then VCO ÷ 2, then finally by VCO.

8-129. In example 2 above, divide-by N is 301, so the counter must count 301 VCO cycles during each reference period. Normally only an even number of cycles could be counted because the least significant divide-by-five counter is counting VCO ÷ 2 from the prescaler. Therefore, to count an odd number, the prescaler is forced to count one additional pulse during each reference period. To accomplish this, the pulse remove circuits are enabled when the least significant (BCD) bit of the least significant digit of the preset number is even, as is the case in example 2 (decimal 8 = binary 1000). Then the negative-going pulse from preload one-shot U15A,D changes the prescaler to divide-by three for one cycle. The pulse remove action associated with fractional N is independent of and in addition to the odd number count.

8-130. Chip Clock Counter U7B divides the prescaler output by five and sends the Chip Clock to fractional N control U8, to clock data in and out of the four internal shift registers. The other output (Q) of U7B clocks the Cycle Start FF and the first section of the output synchronization circuit U4B.

8-131. Cycle Start FF U9B is set by the output of Preload FF U20B and is cleared by the next trailing edge of the Chip Clock signal. A cycle start pulse occurs at the time the divide-by-N least significant digit is preloaded, which is once every reference period. Cycle start is used to initiate operations within fractional N control U8. It is also used to set the pulse remove circuit when divide-by-N is an odd number.

8-132. CONTROL SIGNALS. Several control signals are received by fractional N control U8 and associated output buffer U14. These signals are from the processor via the data bus or A5 Control Decoder circuits. These signals are described as follows:

a. Instruction Valid (INV). INV is from A5 Decoder circuit and is pulsed high when a valid instruction is on the data bus. Data must be valid at the positive edge of INV and is latched in on the negative edge. Execution begins when INV goes low (see *Figure 8-23*).

b. External Clock (EC). EC is from A5 Decoder circuit and is pulsed high when valid data is on the data bus. Data is shifted in on the positive edge. EC must remain Low until it is used to shift in data.

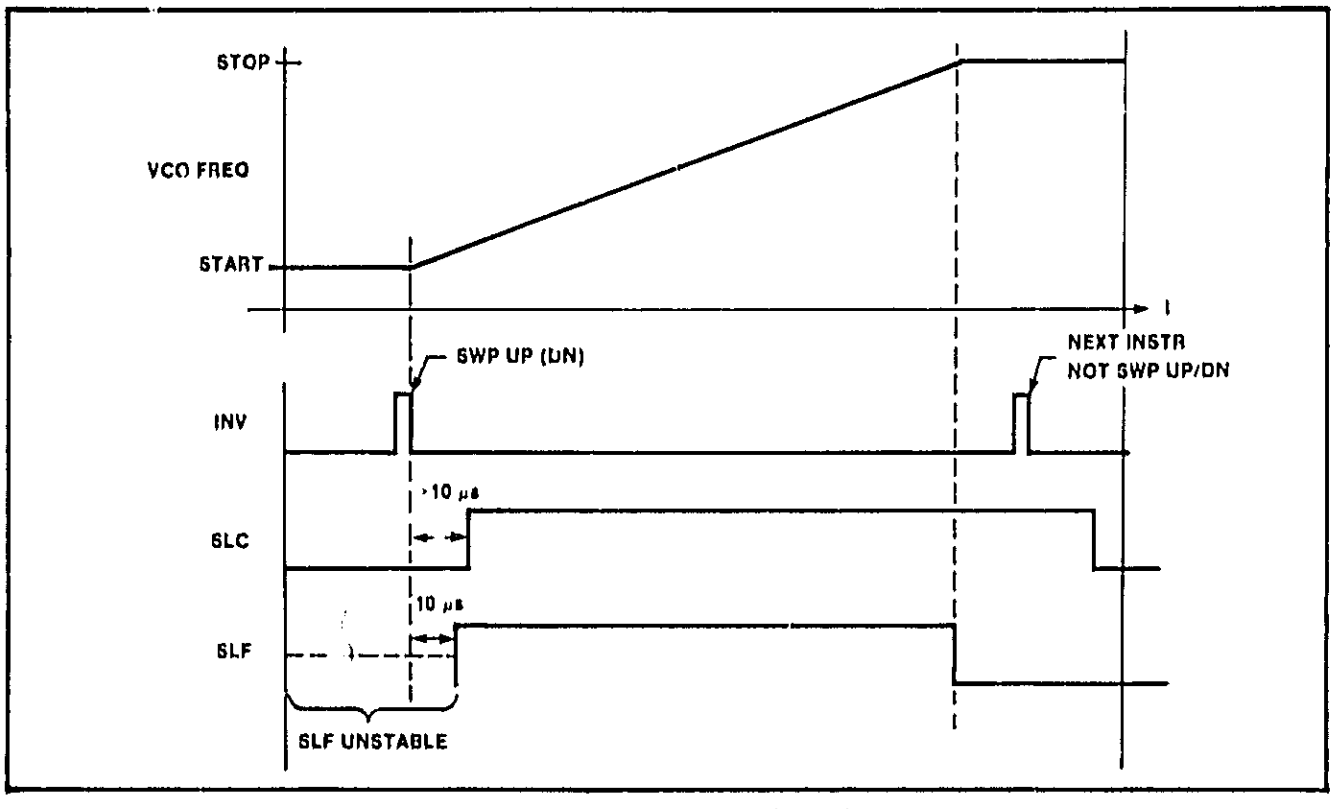


Figure 8-23. A10U8 Control Signals

c. Fractional N Bus Enable (FNBE). A Low FNBE signal enables output buffer A10U14. This buffer drives A10U8 output data bus (LD0–LD3) and provides the VCO Out-of-Range (OOR) signal.

d. Sweep Limit Control (SLC). A High SLC signal enables the sweep width limit capability of fractional N control U8. This causes the N.F synthesizer to stop sweeping and generate a Sweep Limit Flag (SLF) when the Stop frequency is reached. (Refer to the description of SLF under OUTPUT SIGNALS below.) SLC is Low near a marker frequency so an SLF is generated to provide a marker indication but the synthesizer will continue sweeping.

e. Low Data 0 to Low Data 3 (LD0-LD3). The LD0-LD3 data bus connects fractional N control U8 to the processor. Instructions are clocked in by the INV signal, and data is clocked in by the EC signal. The data bus lines also serve as data outputs when data is required by the processor. Output buffer U14 is enabled by FNBE.

8-133. OUTPUT SIGNALS. The fractional N control U8 provides a Sweep Limit Flag to generate an interrupt and a VCO Out-of-Range signal via the data bus to the processor.

a. Sweep Limit Flag (SLF). The fractional N control U8 generates a High to Low transition when a specified frequency is reached while sweeping. This frequency can be used for a marker, the sweep stop, or the sweep-retrace stop. The SLF signal is sent to A8 10V Ramp board Marker Generator and to A3 Keyboard/Display Interrupt circuits to initiate the interrupt to the processor. SLF is in an indeterminant state until one chip reference cycle (10 microseconds) after the Sweep Up (Down) instruction. This signal must be disregarded before this time.

b. Voltage Controlled Oscillator Out-of-Range (VCO OOR). The VCO OOR signal is generated on the A7 VCO board. This signal is sent through buffer A10U14 to the data bus on I D4. The signal goes High whenever the tuning voltage from A9 Analog to A7 VCO is ouside the range -4.8V to 12.1V. The signal is output on the data bus when the FNBE signal to A10U14 is Low.

8-134. A11 Main ROM/Buffer

8-135. As shown in the block diagram, *Figure 8-24*, and the schematic diagram, *Figure 8-34*, the A11 Main ROM/Buffer assembly contains four 4K ROMs that provide memory for the microprocessor which is located in the 5342A (or 5343A). The memory map is divided into two sections, half is in the 5342A (or 5343A) and half is in the 5344A. The logic state of address line LA15 is used to control which half is being used, as described below in paragraph 8-139. A separate set of data bus drivers is used between the ROMs and the 5342A (or 5343A) to provide separation of the data bus within the 5344A so the ROMs can be providing program information to the 5342A (or 5343A), while the 5344A data bus is in use providing for the functions occurring within the 5344A.

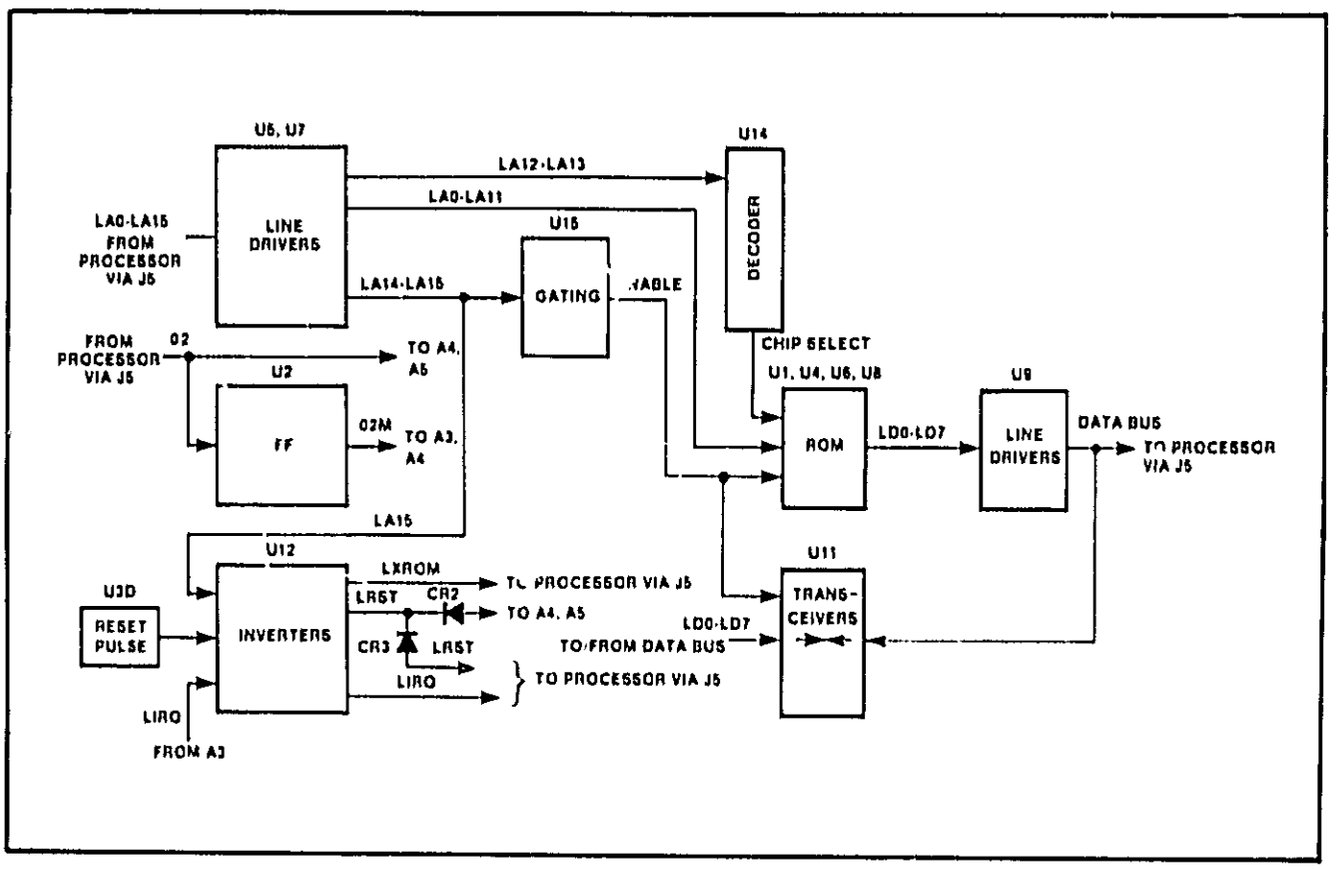


Figure 8-24. A11 Main ROM/Buffer Block Diagram

8-136. ADDRESS LINES (LA0-LA15). The address lines LA0-LA15 from the 5342A (or 5343A) microprocessor are connected to the rear panel PROCESSOR INTERFACE connector on the 5344A via a ribbon cable jumper connected between the instruments. The ribbon cable jumper provides the interface between the instruments and contains address lines, data lines and control lines. The signals are connected from the rear panel via another ribbon cable inside the 5344A to connector J5 on A13 Motherboard, then via traces to connector XA11B, as shown in the motherboard wiring diagram, *Figure 8-36*, and in the bottom view of the instrument, *Figure 8-6*.

8-137. The LA12 and LA13 address lines are decoded by U14 to provide the chip select inputs to the ROMs. The LA14 and LA15 address lines are sent through gate circuits U15, U10C, F, and U13A,B to provide the enable signals to U9 line drivers (to the 5342A or 5343A) or to data bus transceivers U11 (between the 5342A or 5343A and the 5344A). The Phase 2 signal combines with one of the outputs of U15 to enable either U9 line drivers or U11 transceivers to transmit data on the data bus. The data from the ROMs is sent through line drivers U9 to the 5342A (or 5343A) and the data from the 5342A (or 5343A) is sent through transceivers U11 to the decoders on A4 and A5 boards of the 5344A.

8-138. Address line LA15 also goes from U10A to hex inverter U12 to send the Low External ROM (LXROM) signal to the 5342A (or 5343A) processor board. This disables the memory while the 5344A memory is in use. The U12 inverters also process the Low Reset (LRST) and Low Interrupt Request (LIRQ) signals. The LRST is generated from the circuit of A11U3D when power up occurs and is sent to the 5342A (or 5343A) via U12 and diode CR3 and is sent to the 5344A via CR2. The diodes provide isolation between the instruments. A power-up condition from either instrument will generate a reset. The LIRQ signal is generated on the A3 Keyboard/Display Interrupt board and sent via U12 to the processor in the 5342A (or 5343A).

8-139. The Low Valid Memory Address (LVMA) and Low Read (LRD) signals from the processor *(Figure 8-34)*, are sent through inverters U3E,C and U10 D,E, to the A3, A4, and A5 board circuits. The LRD signal is also sent from U10D to transceiver U11 as an enable to control the direction of data flow.

8-140. The Phase 2 signal from the processor is sent to flip-flop A11 U2 to develop Phase 2 M (modified). These signals are supplied as clock signals to the A3, A4, and A5 board circuits.

8-141. A12 Power Supply, A13 Motherboard, and A14 Power Line Module

42. The schematic diagram of the A12, A13, and A14 power supply circuits is shown in *Figure 8-35*. The A14 Power Line Module is mounted on the rear panel of the 5344A and contains a connector for a power cable, a fuse, and a pc card. The pc card can be inserted in any one of four positions to select 100-,120-,200-, or 240-volt ac operation. The power line module is described in detail in paragraph 2-6.

8-143. The output of A14 Power Line Module *(Figure 8-35)* is connected through the LINE OFF/ON switch and S1 thermal switch to the primary of T1 transformer. The output of the secondary of the transformer is connected through diode full-wave rectifiers and filters to voltage regulator circuits. The diode rectifiers are mounted on A13 Motherboard, with the exception of CR1 on the main chassis. The output of CR1 is connected through an overload protection circuit to the 5-volt regulator circuit. The overload protection circuit consists of zener diode CR7 and SCR Q2. If the voltage selector pc card in A14 Power Line Module is not in the proper position when the power mains input is 200 or 240 volts ac, the SCR will fire and blow the protective fuse A14F1.

8-144. +5V REGULATOR. Series pass transistor Q2 receives the unregulated voltage through fuse A12F1. The regulated voltage at the emitter of transistor Q2 is controlled by the +5 volt regulator U1. Transistor Q1 provides current amplification. The output of the regulator is adjusted by variable resistor A12R11, and the output is protected at the level set by zener diode CR1 (5.62V). Above this voltage level SCR Q1 fires to blow protective fuse A12F1

8-145. +15V REGULATOR. The +15V regulator input is rectified by diode bridge CR6, filtered, and applied to +12V regulator U4. The +15V output is adjusted by variable resistor A12R2.

8-146. -15V REGULATOR. The -15V regulator input is rectified by diode bridge CR1, filtered, and applied to -12V regulator U3. The -15V output is adjusted by variable resistor A12R5.

8-147. -5.2V REGULATOR. The -5.2V regulator input is rectified by diode bridge CR5, filtered, and applied to -5V regulator U2. The -5.2V output is adjusted by variable resistor A12R16.

8-148. A13 MOTHERBOARD. In addition to the power supply components described in the preceding paragraphs, A13 Motherboard also contains the XA (assembly number) connectors for the plug-in printed circuit assemblies (cards) and interconnections between the cards. The complete interconnection diagram, including signal mnemonics, is shown in *Figure 8-36*.

8-149. LOGIC SYMBOLS

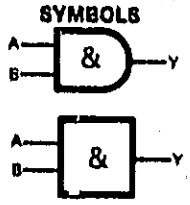
8-150. Logic symbols used in this manual conform to the American National Standard ANSI Y32.14-1973 (IEEE Std. 91-1973). This standard supersedes MIL-STD-806B. In the following paragraphs logic symbols are described.

8-151. Logic Concepts

8-152. The binary numbers 1 and 0 are used in pure logic where 1 represents true, yes, or active and 0 represents false, no, or inactive. These terms should not be confused with the physical quantity (e.g., voltage) that may be used to implement the logic, nor should the term "active" be confused with a level that turns a device on or off. A truth table for a relationship in logic shows (implicitly or explicitly) all the combinations of true and false input conditions and the result (output). There are only two basic logic relationships, AND and OR. The following illustrations assume two inputs (A and B), but these can be generalized to apply to more than two inputs.

AND

EQUIVALENT SYMBOLS



TRUTH TABLE

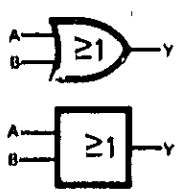
A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

Y is true if and only if A is true and B is true (or more generally, if all inputs are true).

Y = 1 if and only if A = 1 and B = 1.
Y = A • B

OR

EQUIVALENT SYMBOLS



TRUTH TABLE

A	B	Y
1	1	1
1	0	1
0	1	1
0	0	0

Y is true if and only if A is true or B is true (or more generally, if one or more input(s) is (are) true).

Y = 1 if and only if A = 1 or B = 1.
Y = A + B

8-153. Negation

8-154. In logic symbology, the presence of the negation indication symbol ○ provides for the representation of the logic function inputs and outputs in terms *independent* of their physical values; the 0-state of the input and output being the 1-state of the symbol referred to by the symbol description.

NOTE

In this manual the logic negation symbol ○ is NOT used.

EXAMPLE 1

TRUTH TABLE

A	B	Z
1	1	0
1	0	1
0	1	1
0	0	1

Says that Z is not true if A is true and B is true or that Z is true if A and B are not both true. $\overline{Z} = AB$ or $Z = \overline{A} + \overline{B}$. This is frequently referred to as NAND (for NOT AND).

EXAMPLE 2

TRUTH TABLE

A	B	Z
1	1	0
1	0	1
0	1	1
0	0	1

Says that Z is true if A is not true or if B is not true. $Z = \overline{A} + \overline{B}$. Note that this truth table is identical to that of Example 1. This logic equation is merely a DeMorgan's transformation of the equations in Example 1. The symbols are equivalent.

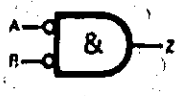
EXAMPLE 3

TRUTH TABLE

A	B	Z
1	1	0
1	0	0
0	1	0
0	0	1

$\overline{Z} = A + B$ or $Z = \overline{AB}$.

EXAMPLE 4



TRUTH TABLE

A	B	Z
1	1	0
1	0	0
0	1	0
0	0	1

$Z = \overline{A} \cdot \overline{B}$, also share common truth table and and are equivalent transformations of each other. The NOT OR form (Example 3) is frequently referred to as NOR.

8-155. Logic Implementation and Polarity Indication

8-156. Devices that can perform the basic logic functions, AND and OR, are called gates . Any device that can perform one of these functions can also be used to perform the other if the relationship of the input and output voltage levels to the logic variables 1 and 0 is redefined suitably.

8-157. In decribing the operation of electronic logic devices, the symbol H is used to represent a "high level," which is a voltage within the more-positive (less-negative) of the two ranges of voltages used to represent the binary variable. L is used to represent a "low level", which is a voltage within the less-positive (more-negative) range.

8-158. A function table for a device shows (implicitly or explicitly) all the combinations of input conditions and the resulting output conditions.

8-159. In graphic symbols, inputs or outputs that are active when at the high level are shown without polarity indication. The polarity indicator symbol denotes that the active (one) state of an input or output with respect to the symbol to which it is attached is low level.

NOTE

The polarity indicator symbo ◺ is used in this manual.

EXAMPLE 5

DEVICE #1 FUNCTION TABLE

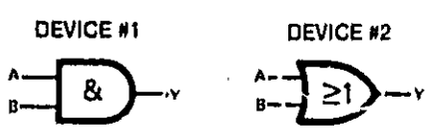
A	B	Y
H	H	H
H	L	L
L	H	L
L	L	L

DEVICE #2 FUNCTION TABLE

A	B	Y
H	H	H
H	L	H
L	H	H
L	L	L

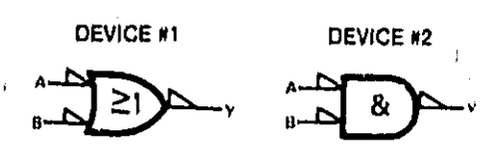
Assume two devices having the following function tables.

POSITIVE LOGIC.



By assigning the relationships H = 1, L = 0 at both input and output, Device #1 can perform the AND function and Device #2 can perform the OR function. Such a consistent assignment is referred to as positive logic.

NEGATIVE LOGIC.



Alternatively, by assigning the relationship H = 0; L = 1 at both input and output, Device #1 can perform the OR function and Device #2 can perform the AND function. Such a consistent assignment is referred to as negative logic.

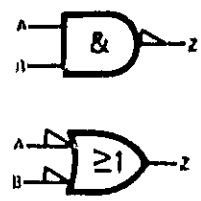
8-160. MIXED LOGIC. The use of the polarity indicator symbol on some inputs (▷) automatically invokes a mixed-logic convention. This is, positive logic is used at the inputs and outputs that have polarity indicators.

EXAMPLE 6

FUNCTION TABLE

A	B	Z
H	H	L
H	L	H
L	H	H
L	L	H

This may be shown either of two ways:



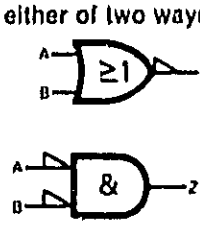
Note the equivalence of these symbols to Examples 1 and 2 and the fact that the function table is a positive-logic translation (H = 1, L = 0) of the NAND truth table, and also note that the function table is the negative-logic translation (H = 0, L = 1) of the NOR truth table, given in Example 3.

EXAMPLE 7

FUNCTION TABLE

A	B	Z
H	H	L
H	L	L
L	H	L
L	L	H

This may be shown either of two ways:



Note the equivalence of these symbols to Examples 3 and 4 and the fact that the function table is a positive-logic translation (H = 1, L = 0) of the NOR truth table, and also note that the function table is the negative-logic translation (H = 0, L = 1) of the NAND truth table, given in Example 1.

8-161. It should be noted that one can easily convert from the symbology of positive-logic merely by substituting a polarity indicator (▷) for each negative indicator (○) while leaving the distinctive shapes alone. To convert from the symbology of negative-logic, a polarity indicator (▷) is substituted for each negation indicator (○) and the OR shape is substituted for the AND shape or vice versa.

8-162. It was shown that any device that can perform OR logic can also perform AND logic and vice versa. DeMorgan's transformation is illustrated in Examples 1 through 7. The rules of the transformation are:

1. At each input or output having a negation (○) or polarity (▷) indicator, delete the indicator.
2. At each input and output not having an indicator, add a negation (○) or polarity (▷) indicator.
3. Substitute the AND symbol (D) for the OR symbol (⊃) or vice versa. These steps do not alter the assumed convention; positive-logic stays positive, negative-logic stays negative, and mixed-logic stays mixed.

8-163. The choice of symbol may be influenced by these considerations:

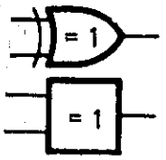
(1) The operation being performed may best be understood as AND or OR. (2) In a function more complex than a basic gate, the inputs will usually be considered as inherently active high or active low (e.g., the J and K inputs of a J-K flip-flop are active high and active low, respectively). (3) In a choice of logic, understanding and the writing of logic equations are often facilitated if active low or negated outputs feed into active low or negated inputs.

8-164. Other Qualifying Symbols

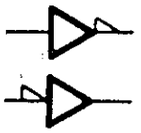
8-165. Other qualifying symbols are required to depict complex logic diagrams. Some of the other symbols are as follows:

Dynamic input activated by transition from a low level to a high level. The opposite transition has no effect at the output.

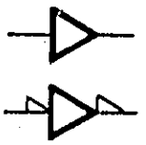
Dynamic input activated by transition from a high level to a low level. The opposite transition has no efect at the output.



Exclusive OR function. The output will assume its indicated active level if and only if one and only one of the inputs assumes its indicated active level.



Inverting function. The output is low if the input is high and it is high if the input is low. The two symbols shown are equivalent.



Noninverting function. The output is high if the input is high and it is low if the input is low. The two symbols shown are equivalent.

OUTPUT DELAY. The output signal is effective when the input signal returns to its opposite state.

EXTENDER. Indicates when a logic function increases (extends) the number of inputs to another logic function.

FLIP-FLOP. A binary sequential element with two stable states: a set (1) state and a reset (0) state. Outputs are shown in the 1-state when the flip-flop is set. In the reset state the outputs will be opposite to the set state.

RESET. A 1 input will reset the flip-flop. A return to 0 will cause no further effect.

SET. A 1 input will set the flip-flop. A return to 0 will cause no further effect.

TOGGLE. A 1 input will cause the flip-flop to change state. A return to 0 will cause no further action.

J INPUT. Similar to the S input except if both J and K (see below) are at 1, the flip-flop changes.

K INPUT. Similar to the R input (see Reset).

D INPUT (Data). Always dependent on another input (usually C). When the C and D inputs are at 1, the flip-flop will be set. When the C is 1 and the D is 0, the flip-flop will reset.

ADDRESS. Address symbol has multiplexing relationship at inputs and demultiplexing relationship at outputs.

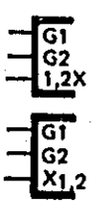
8-166. Dependency Notation "C" "G" "V" "F"

8-167. Dependency notation is a way to simplify symbols for complex IC elements by defining the existence of an AND relationship between inputs, or by the AND conditioning of an output by an input without actually showing all the elements and interconnections involved. The following examples use the letter "C" for control and "G" for gate. The dependent input is labeled with a number that is either prefixed (e.g.,1X) or subscripted (e.g.,X_1). The both mean the same thing. The letter "V" is used to indicate an OR relationship between inputs and outputs with this letter (V). The letter "F" indicates a connect-disconnect relationship. If the "F" (free dependency) inputs and outputs are active (1) the other usual normal conditions apply. If one or more of the "F" inputs are active (0), the related "F" output is disconnected from its normal output condition (it floats).

The input that controls or gates other inputs is labeled with a "C" or a "G", followed by an identifying number. The controlled or gated input or output is labeled with the same number. In this example, "1" is controlled by "G1".

When the controlled or gated input or output already has a functional label (X is used here), that label will be prefixed or subscripted by the identifying number.

If a particular device has only one gating or control input then the identifying number may be eliminated and the relationship shown with a subscript.

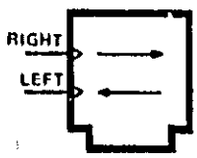


If the input or output is affected by more than one gate or control input, then the identifying numbers of each gate or control input will appear in the prefix or subscript, separated by commas. In this example "X" is controlled by "G1" and "G2".

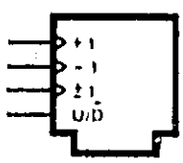
8-168. Control Blocks

8-169. A class of symbols for complex logic are called control blocks. Control blocks are used to show where common control signals are applied to a group of functionally separate units. Examples of types of control blocks follow:

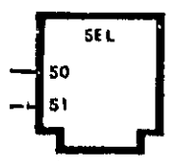
Register control block. This symbol is used with an associated array of flip-flop symbols to provide a point of placement for common function lines, such as a common clear.

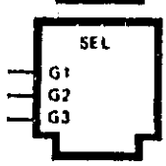


Shift register control block. These symbols are used with any array of flip-flop symbols to form a shift register. An active transition at the inputs causes left or right shifting as indicated.

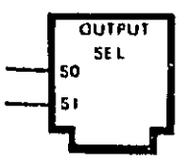


Counter control block. The symbol is used with an array of flip-flops or other circuits serving as a binary or decade counter. An active transition at the +1 or -1 input causes the counter to increment one count upward or downward, respectively. An active transistion at the ± input causes the counter to increment one count upward or downward depending on the input at as up/down control.

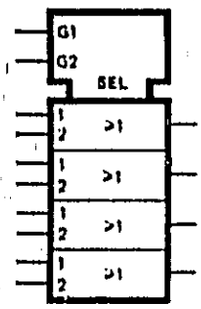




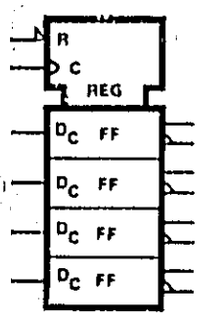
Selector control block. These symbols are used with as array of OR symbols to provide a point of placement for selection (S) or gating (G) lines. The selection lines enable the input designated 0, 1, ...n each OR function by means of a binary code where S0 is the least significant digit. If the 1 level of these lines is low, polarity indicators (◺) will be used. The gating lines have an AND relation with the respective input of each OR function: G1 with the inputs numbered 1, G2 with the inputs numbered 2, and so forth. If the enabling levels of these lines is low, polarity indicators (◺) will be used.



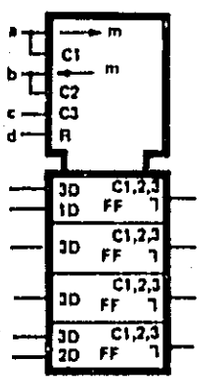
Output selector control block. This symbol is used with a block symbol having multiple outputs to form a decoder. The selection lines enable the output designated 0, 1, ...n each block by means of a binary code where S0 is the least significant digit. If the 1 level of these lines is low polarity indicators (◺) will be used.



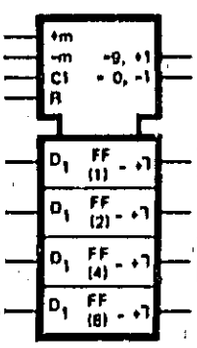
Selector control block used to simplify AND portion of a quad AND-OR select gate. When G1 is high, the data presented at the "1" inputs will be gated through. When G2 is high, the data presented at the "2" inputs will be gated through.



Register control block used to illustrate a quad D-type latch. There is a common active low reset (R), and a common edge triggered control input (C). Since there is only one dependency relationship, the controlling input is not numbered and the controlled functions (D) are subscripted with a C (control). These inputs are sometimes shown as "DC" or "CD".



Shift register control block used to show common inputs to a bidirectional shift register. Notice that "≥m" means shift the contents to the right or down by "m" units. Note: if m=1, it may be omitted. Inputs "a" and "b" are each single IC pins that have two functions. Input "a" enables one of the inputs to the top D-type flip-flop (1D), and also shifts the register contents down one unit. Input "b" enables one of the inputs to the bottom flip-flop (2D), and also shifts the register contents left (up) one unit. Input "c" loads all four flip-flops in parallel (3D). Input "d" is a common reset. The output delay indicator is used because these are master-slave flip-flops.

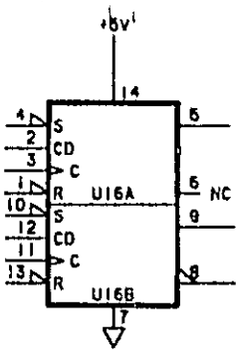


Counter control block used to show common inputs to a Presettable Decade Up/Down Counter. Notice that "+m" means count-up (increment the count) by "m"; "-m" means count down by "m". Note: if m=1, it may be omitted. Since the D-type flip-flops are master-slave, the output delay indicator is used. The "=9", +1, and "=0, -1" notation defines when the carry and borrow outputs are generated. They also define it as a decade counter; a binary counter would have carry indicated with "=15,+1". Flip-flop weighting is indicated in parenthesis.

8-170. Complex Logic Devices

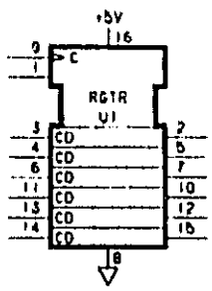
8-171. Logic elements can be combined to produce very complex devices that can perform more difficult functions. A control block symbol can be used to simplify understanding of many complex devices. Several examples of complex devices are given here.

Reference Designations
A3U1, A8U5, A8U16,
A9U2, A10U4
Part Number
1820-1112
SN74LS74N



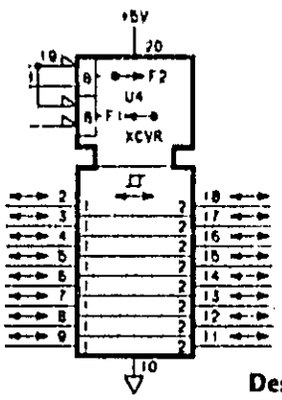
Description: DUAL D-TYPE FLIP-FLOP
The dual D-type flip-flop consists of two independent D-type flip-flops. The information present at the data (DC) input is transferred to the active-high and active-low outputs on a low-to-high transition of the clock (C) input. The data input is then locked out and the outputs do not change again until the next low-to-high transition of the clock input. The set (S) and reset (R) inputs override all other input conditions: when S is low, the active-high output is forced high; when R is low, the active-low output is forced low. Although normally the active-low output is the complement of the active-high output, simultaneous low inputs at the set and reset will force both the active-low and active-high outputs to go high at the same time on some D-type flip-flops. This condition will exist only for the length of time that both set and reset inputs are held low. The flip-flop will return to some indeterminate state when both the set and reset inputs are returned to the high state.

Reference Designations
A9U1, A10U13, A10U17
Part Number
1820-1196
SN74LS174N

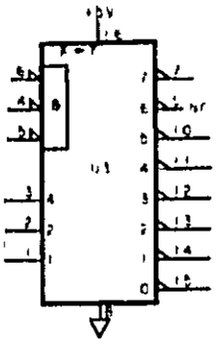


Description: HEX D-TYPE FLIP-FLOPS
Information at the D-inputs is transfered to the outputs on the positive-going edge of the clock pulse (pin 9). Clock triggering occurs at a particular voltage level. The hex flip-flops have single outputs.

Reference Designations
A3U4, A11U11
Part Number
1820-2075
SN74LS245N

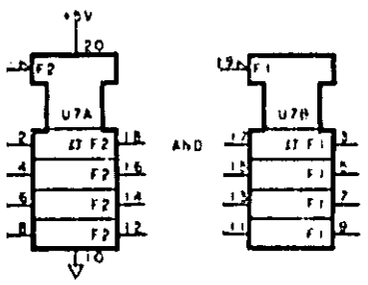


Description: OCTAL BUS TRANSCEIVERS
The octal bus transceivers provide two-way communication between data buses. The direction of data flow depends upon the logic level at pin 1. Pin 19 (HIGH) can disable the flow and isolate the buses.



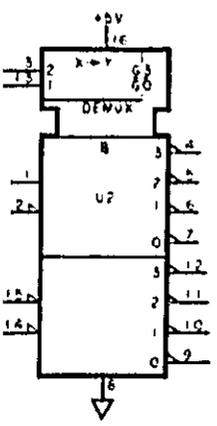
Reference Designations
A3U5, A5U3
Part Number
1820-1216

Description: DECODER/MULTIPLEXER
The binary-weighted inputs (1,2,4) are decoded to provide the output when the enable inputs pins 4 and 5 are LOW and pin 6 is HIGH.



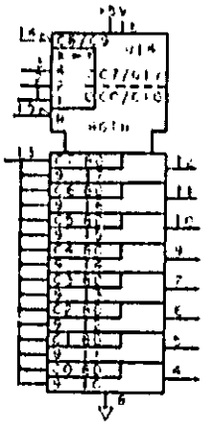
Reference Designations
A3U8, A1U5,
A11U7, A11U9
Part Number
1829-2024
SN74LS244N

Description: OCTAL BUFFER AND LINE DRIVERS
The octal buffers and line drivers are used to improve the performance of the three-state memory address circuits. A LOW on the enable pin (1 or 19) allows each element to transfer input data from the address bus to the output. Hysteresis at the inputs improves noise margins.



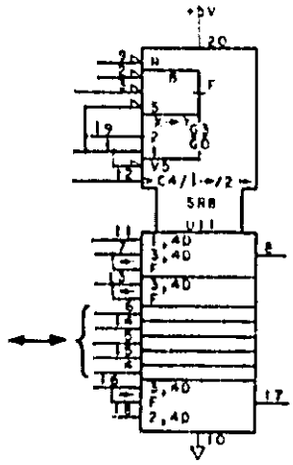
Reference Designations
A5U2, A11U14
Part Number
1820-1216
SN74LS155N

Description: DUAL 2-LINE TO 4-LINE DECODER
The dual 2-line to 4-line decoder allows the binary-weighted input (pins 3 and 13) to select and route input data (pin 1 or 15) to the appropriate output, when enabled by the strobe (pin 2 or 14 LOW.)



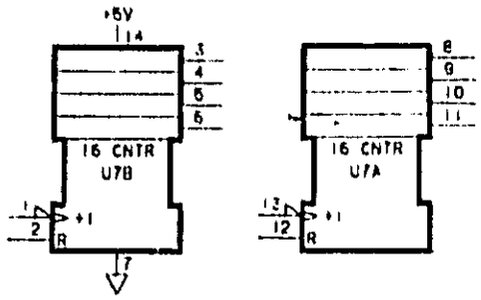
Reference Designations
A5U10, A5U12, A5U14
Part Number
1820-1729
SN74LS259N

The 8-bit addressable latch is used in this application as a 1-of-8 decoder with active-high outputs. The addressed output will follow the level of the D-input with all other outputs LOW. The mode of operation depends upon the logic level at pin 14 (enable) and pin 15 (clear).



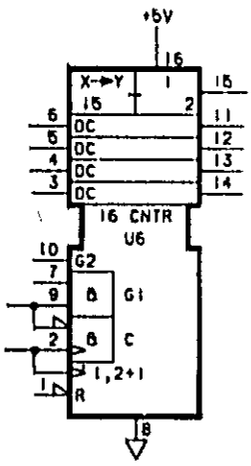
Reference Designation
A5U11
Part Number
1820-1987
SN74LS299

The 8-bit universal register uses multiplexed inputs/outputs to provide 8-bit data handling. Two function-select inputs (pins 1 and 19) and two output-control inputs (pins 2 and 3) choose the mode of operation. When pins 1 and 19 are both HIGH, synchronous parallel loading occurs. This places the three-state outputs (F) in a high-impedance state and permits data on the input/output lines to be clocked in. Reading out can occur when the outputs are enabled in any mode. A LOW on pin 9 clears the register. A HIGH on pin 11 provides a shift right, a HIGH on pin 18 provides a shift left.



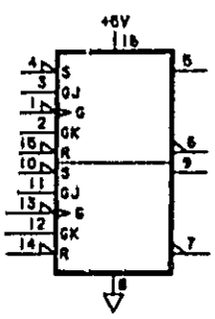
Reference Designations
A8U1, A8U7, A8U8, A8U12
Part Number
1820-2096
SN74LS393N

The two separate 4-bit binary counters each have a clear (pin 2 or 12) input and a clock (pin 1 or 13) input. The clock signal goes LOW to provide a count up (+1) and each stage has parallel outputs so that any submultiple of the input count frequency is available at the output. A HIGH on pin 2 or 12 clears the associated stage.



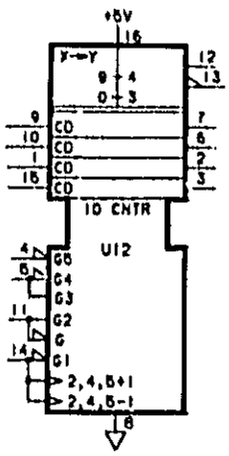
Reference Designations
A8U6, A8U14
Part Number
1820-1430
SN74LS161AN

The synchronous presettable decade counter has four master-slave flip-flops that are triggered on the positive-going edge of the clock pulse (pin 2). A LOW at the load input (pin 9) disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels at the enable inputs (pins 7 and 10). The clear function (pin 1) is asynchronous and a low level clear input sets all outputs low regardless of the levels of the clock, load, or enable inputs. Both count enable inputs (pins 7 and 10) must be HIGH to count and the pin 10 input is fed forward to enable the carry output (pin 15).



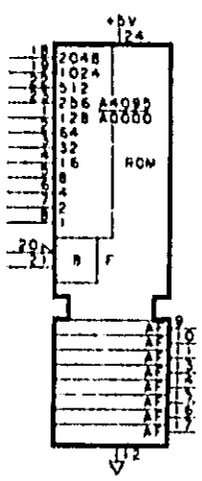
Reference Designations
A10U1, A10U10
Part Number
1820-0629
SN74S112N

The dual J-K clocked flip-flop consists of two identical, separate flip-flop circuits. When preset (pin 4 or 10) and clear (pin 14 ar 15) are HIGH, a HIGH level at the clock (pin 1 or 13) input enables the J and K inputs and data will be accepted. Input data is transferred to the outputs on the negative-going edge of the clock pulse. The preset or clear inputs, when LOW, set or reset the outputs regardless of the levels of the other inputs.



Reference Designations
A10U12, A10U16
Part Number
1820-1279
SN74LS190N

The synchronous, reversible up/down counters have four masterslave flip-flops that are triggered on a low-to-high transition of the clock input (pin 14), if the enable input (pin 4) is LOW. Direction of the count is determined by the logic level of the up/down input (pin 5). Pin 5 LOW causes a count up, pin 5 HIGH causes a count down. The outputs may be preset to either level by placing a LOW on the load input (pin 11), and entering the desired data at the data inputs (pins 9, 10, 1, 15). The ripple clock (pin 13) produces an output pulse when an overflow or underflow condition exists. The maximum/minimum count output (pin 12) is used to accomplish look-ahead operation.



Reference Designations
A11U1, A11U4, A11U6, A11U8
Part Number
05344-8000X

Read-only memory with 4096 addresses. Address selection is determined by the 12-bit address input in the upper left corner of the control block. A HIGH on pin 21 and a LOW on pin 20 enables the three-state (F) outputs for the addressed memory location.

8-172. TROUBLESHOOTING

8-173. Troubleshooting procedures are provided in *Tables 8-2* through *8-17* as listed below. The tables start with procedures to isolate a problem to the 5342A (or 5343A) counter or the 5344A when the instruments are connected to form the 5344S. The next table contains troubleshooting for the 5344A and the tables that follow contain procedures for each of the assemblies of the 5344A. The tables are in the following order:

Table 8-2. 5344S Overall Troubleshooting
Table 8-3. 5344A Troubleshooting
Table 8-4. Kernel Troubleshooting
Table 8-5. A11 Main ROM/Buffer Assembly Troubleshooting
Table 8-6. A5 R/W Memory/Decoder Assembly Troubleshooting
Table 8-7. A3 Keyboard/Display Interrupt Assembly Troubleshooting
Table 8-8. A1 Keyboard/Display Assembly Troubleshooting
Table 8-9. Diagnostics
Table 8-10. Phase Lock Loop Overall Troubleshooting
Table 8-11. A4 HP-IB Interface/Ramp and Z-Axis Assembly Troubleshooting
Table 8-12. A6 Main Loop Assembly Troubleshooting
Table 8-13. A7 VCO Assembly Troubleshooting
Table 8-14. A8 10 Volt Ramp/Timebase Assembly Troubleshooting
Table 8-15. A9 Analog Assembly Troubleshooting
Table 8-16. A10 Digital Assembly Troubleshooting
Table 8-17. A12 Power Supply Assembly Troubleshooting

WARNING

TROUBLESHOOTING PROCEDURES REQUIRE INTERNAL ACCESS TO THE INSTRUMENT WITH THE PROTECTIVE COVERS REMOVED. THESE PROCEDURES SHOULD BE PERFORMED ONLY BY SERVICE-TRAINED PERSONNEL WHO ARE AWARE OF THE HAZARDS INVOLVED.

NOTE

Whenever repairs or adjustments are made, the instrument should be checked for proper performance. Refer to the Adjustments in Section V and the Performance Tests in Section IV.

CAUTION

Integrated circuits can be damaged by electrostatic discharge. Use the following precautions:

DO NOT wear clothing subject to static charge buildup, such as wool or synthetic materials.

DO NOT handle integrated circuits in carpeted areas.

DO NOT remove the circuit from its conductive foam pad until you are ready to install it.

AVOID touching the circuit leads. Handle by the plastic package only.

ENSURE that static sensitive devices or assemblies are serviced at static safe work stations, and are stored in static shielding containers.

Table 8-2. 5344S Overall Troubleshooting

Isolate the fault to the 5342A/5343A or the 5344A, as follows:

1. Power up the counter:
   a. If the counter does not power up properly as described in step 1, *Table 8-5* of the counter service manual, proceed with *Table 8-5* troubleshooting information.
   b. Perform the Operation Verification in Section IV of the service manual if any repairs or adjustments are made.

2. Check 10 MHz FREQ STD OUT from counter - route around from back panel to front panel low frequency input port (BNC connector). Place the impedance select switch in the 50-ohm position and place the range switch in the 10 Hz-500 MHz position. The counter should display 10 MHz (±1 Hz) for a 1 Hz resolution setting.

3. Check IF OUT from counter — use a counter or an Oscope which will be able to count in the IF range up to 100 MHz, and measure the IF signal from the rear panel. Place the 5342A (5343A) range switch in the 500 MHz-18 (26) GHz position, and input a 0 dBm CW signal at

   1 . 000 XXX XXX GHz (X denotes a "don't care" digit).

   Verify that the microwave counter shows the proper frequency, then perform the following key sequence on the 5342A/43A counter front panel:

   SET SET 4

   This is one of the counter's diagnostic modes which allows the user to observe the current IF frequency for the input of interest. Compare the frequency displayed by the microwave counter with that displayed by the other counter or Oscope - both displays should match.

4. Check rear panel interconnections:
   - Check interface cable for continuity (no cuts or breaks), and verify that the pin connector for each instrument has no bent or missing pins
   - Connect Processor Interface ribbon cable to both instruments
   - Connect counter's IF OUT to 5344A's IF IN using a BNC cable
   - Connect counter's FREQ STD OUT to 5344A's 10 MHZ IN using a BNC cable

5. Power up the 5344A:
   a. If the 5344A does not power up properly as described in Section III "OPERATOR'S CHECKS" refer to *Table 8-3*, 5344A Troubleshooting.
   b. Perform the Operation Verification in Section IV if any repairs or adjustments are made.

6. Performance Test 5342A/43A and 5344A - follow directions given for the performance tests as given in Section IV of the respective manuals.

Table 8-3. 5344A Troubleshooting

The following information provides an overview of the approach to troubleshooting the 5344A Source Synchronizer.

NOTE

A majority of the measurements made rely on a 5005 Signature Multimeter, primarily because of its versatility and built-in data probe. It is recommended that a 5005 Signature Multimeter be used as it will eliminate the need for extra troubleshooting equipment.

1. Remove the top cover and plates as instructed in paragraph 8-22. Note that this requires disconnecting the interface cable (see *Figure 2-3*) between the counter and the 5344A. Be sure to reconnect the interface cable once the top cover has been removed.

2. Apply power to the counter and the 5344A, and check the power supplies; each power supply should be within its given range:

5V Supply	4.99V to 5.01V
-5.2V Supply	-5.22V to -5.18V
15V Supply	14.95V to 15.05V
-15V Supply	-15.05 to -14.95V

NOTE

Refer to the power supply adjustments in Section V if the levels are out of range, or consult *Table 8-15*, A12 Power Supply Assembly Troubleshooting if any supply is dead.

3. Check board continuity and connectors — it is recommended that each assembly be removed, examined for any contamination, and reseated. If contamination is present on any edge fingers, clean both the edge fingers and the associated edge connector with a lint-free cloth and an alcohol/water solution.

4. Proceed with verifying the operation of the kernel as described in *Table 8-4*. The kernel is probably operational if:

   a. The 5344A powers up correctly

      — CW annunciator lit
      — F1 button annunciator lit
      — 0.000000 MHz displayed
      — 10 segment tuning meter has center 2 segments dimly lit

   b. No error message is displayed at power-up

   c. Diagnostics 1 and 2 can be performed (refer to *Table 8-8*, Diagnostics).

   The kernel is probably not operational if:

   a. The 5344A powers-up with random data or a blank display

   b. The unit powers-up with an error message (refer to *Table 3-6*)

   If the kernel is operational, then proceed to step 5. If not, then refer to *Table 8-4*, Kernel Troubleshooting.

5. Proceed with diagnostics to isolate the fault to a board. Refer to *Table 8-8*, Diagnostics and begin with Diagnostic 3.

Table 8-4. Kernel Troubleshooting

The kernel for the 5344A is comprised of four assemblies:

- A1 Keyboard/Display Assembly
- A3 Keyboard/Display Interrupt Assembly
- A5 Read/Write Memory/Decoder Assembly
- A11 ROM Buffer Assembly

These boards must he working before any other portion of the unit can be verified for proper operation. The following procedure outlines the the order and manner in which the kernel should be troubleshoot.

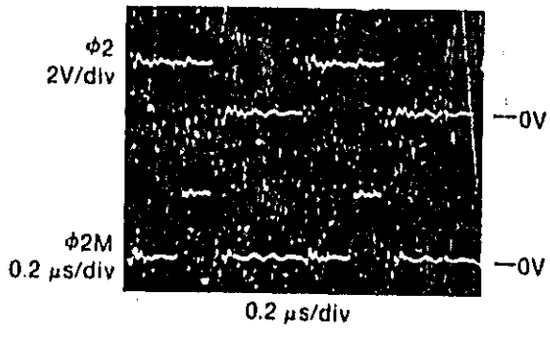
NOTES

- Voltage levels and frequencies provided are TTL compatible unless otherwise noted.
- Voltage and frequency tolerances are 10% unless otherwise noted.
- The front panel ribbon cable (from the A1 Display Board to the A3 Keyboard/Display Interrupt Assembly) may be disconnected during freerun to blank the 5344A display.
- The 5344A should be switched off before removing or replacing board assemblies.
- Values given in parentheses denote 5343A levels, voltages, frequencies, and signatures.
- Values preceded by a "~" indicate an approximate value for an unstable voltage or frequency.

Begin checking the operation of the kernel by verifying the signals (levels or frequencies) as given for the board test points. The following table gives these values and the order in which to check them.

	FREQUENCY OR VOLTAGE	IF FAULTY, SUSPECT
A11	TP1 (CS0) : 72 Hz (108 Hz)	U14
	TP2 (ϕ2M) : 1 MHz	U2
	TP3 (ϕ2) : 1 MHz	Counter processor

The signals at Test Points 2 and 3 should appear as shown here:



	TP4 (CS1) : 290 Hz	U14
	TP5 (CS2) : TTL HIGH	U14
	TP6 (CS3) : ~4.8 kHz	U14
	TP7 (LA15) : 180 Hz (~350 kHz)	U7
	TP8 (RD) : ~2 kHz — ~10 kHz	Counter processor
	TP9 (VMA) : ~113 kHz	Counter processor
	TP10 (GND) : 0.00 V	Power Supply
	TP11 (+5V) : 5.0 V	Power supply

Table 8-4. Kernel Troubleshooting (Continued)

A5	TP1 (CS0) : 4.3 kHz (5 kHz)	U2
	TP2 (CS1) : TTL HIGH (30 Hz)	U2
	TP3 (ϕ2) : 1 MHz	A11
	TP4 (CS2) : TTL HIGH	U2
	TP5 (CS3) : TTL HIGH	U2
	TP6 (EDL) : TTL HIGH	U10
	TP7 (+5V) : 5.0 V	Power Supply
	TP8 (GND) : 0.00 V	Power Supply
	TP9 (DDB) : TTL HIGH	U10
A3	TP1 (SL0) : 976 Hz	U3
	TP2 (SL1) : 488 Hz	U3
	TP3 (SL2) : 244 Hz	U3
	TP4 (SL3) : 122 Hz	U3
	TP5 (IRQ) : 35 Hz	U11
	TP6 (LFP1) : 144 Hz	A5
	TP7 (LFP2) : 185 Hz	A5
	TP8 (+5) : 5.0 V	Power Supply
	TP9 (GND) : 0.00 V	Power Supply

If any test points show incorrect readings for signals as documented here, refer to the appropriate assembly troubleshooting table that follows.

If all readings are correct, proceed to verify operation of the A11 Assembly by checking voltages, frequencies, and signatures for this board as given in *Table 8-5*, A11 Main ROM/Buffer Assembly Troubleshooting. The purpose of checking this board first is to establish the validity of the information passed from the counter to the 5344A.

If all readings for the A11 Assembly are correct, verify the following assemblies in a like manner and in this order:

- A5 Main ROM/Buffer Assembly
- A3 Keyboard/Display Interrupt Assembly
- A1 Keyboard/Display Assembly

Table 8-5. A11 Main ROM/Buffer Assembly Troubleshooting

Turn off power to the 5344A and place the A11 Assembly on two 05342-60033 extender boards.

1. If the counter powers up correctly, but the 5344A does not, then check that the LRST (Low Reset) line is functioning properly.

   5342A: Monitor 5344A A11U12(8) and observe these levels:

Only Counter Powered Up	Counter and 5344A Powered Up
2.6 V → 2.9 V (Unstable)	4.8 V ± 0.2 V

   5343A: DC levels do not provide a simple check of this line. Therefore, use an Oscope to look for the transition of 5344A A11U12(8) from TTL high when the counter only is powered up, to TTL low when the 5344A is first switched on, then to TTL high shortly thereafter.

2. Troubleshoot using Signature Analysis

   a. Place the counter in freerun by following the directions given in the service manual under "A14 Microprocessor Troubleshooting". Verify that the characteristic 0003 signature (probe light brightly lit) occurs when +5V is probed, and that the characteristic 0000 signature (probe light not lit) occurs when ground is probed.

   b. Probe the address bus entering and leaving A11 for signatures. These signatures are available at A11U5/U7.

   c. Both inputs and outputs should be checked. If the input signatures are not correct, then it is likely that the counter address information is not being transferred correctly to the 5344A. If the output signatures are not correct, then suspect a faulty buffer (U5 or U7).

U5/U7 Freerun signatures — observe that these signatures are for **address lines** and IC pin numbers.

Low Address Line (LA)	Signature	IC Pins
0	UUUF	U5(3,17)
1	FFFU	U5(5,15)
2	6487	U5(7,13)
3	P760	U5(9,11)
4	1U5H	U5(2,18)
5	0355	U5(4,16)
6	U75A	U5(6,14)
7	6F99	U5(8,12)
8	7792	U7(7,13)
9	6322	U7(5,15)
10	17C6	U7(3,17)
11	6U2C	U7(6,14)
12	4FC9	U7(9,11)
13	486C	U7(8,12)
14	9UP2	U7(2,18)
15	0001	U7(4,16)
+5V	0003*	U5,U7(20)
GND	0000*	U5,U7(1,10,19)

* indicates that the probe light is **NOT** blinking

Table 8-5. A11 Main ROM/Buffer Assembly Troubleshooting (Continued)

Probe the 4 Chip Select lines (CS0-CS3). Signatures should be as follows:

TP1 (CS0) - HA92
TP2 (CS1) - P7AA
TP3 (CS2) - 132H
TP4 (CS3) - F4AC

If any chip select signatures are incorrect, suspect U14 and proceed to verify this IC (and others) using the freerun signatures given here:

PIN	U9	U10	U11	U13	U14	U15
1	PACH	0001	0003*	PACF		0003*
2	3064 (2521)	0002		0003		0002
3		9UP2		PACU	486C	
4	U618 (6319)	9UP1			0003*	9UP2
5		PACU			0003*	0003*
6	947U (402P)	PACF		0000*	0003*	PACU
7		0000*		0000*	0003*	0000*
8	FOU8 (AU16)	0003*		0000*	0000*	PACH
9		0000*			F4AC	0003*
10	0000*	0000*	0000*		P7AA	0003*
11	CCFH (FO23)	0003*		PACH	132H	
12		PACP		PACP	HA92	0002
13	U40C (9AC1)	PACH		0003	4FC9	9UP1
14		0003*		0003*	PACH	0003*
15	FHA5 (234A)			0000*	0000*	
16					0003*	
17	P279 (1HF7)					
18						
19	PACH		PACU			
20	0003*		0003*			

NOTE

Blanks indicate unstable or meaningless signatures.

* indicates that the probe light is **NOT** blinking.

If incorrect signatures are encountered, backtrace along the signal path from output to input until a device is found where the input shows a correct signature, but the output shows an incorrect one. This particular IC is likely to be the cause of the fault.

3. ROM Data Check — ROM data is verified on power-up by a checksum test. If an incorrect checksum is obtained, Err 13 will appear in the display with the component designator of the faulty component.

Table 8-6. A5 R/W Memory/Decoder Assembly Troubleshooting

Turn off power to the 5344A and place the A5 Assembly on two 05342-60033 extender boards.

1. Troubleshoot using Signature Analysis

   Check validity of control signals generated from control registers U10 and U14.

   Place the counter in freerun by following the directions given in the service manual under "A14 Microprocessor Troubleshooting". Verify that the characteristic 0003 signature (probe light brightly lit) occurs when +5V is probed, and that the characteristic 0000 signature (probe light not lit) occurs when ground is probed. Power up the 5344A, and place the 5005 in the kHz mode.

   a. Freerun sets U10 outputs high — Verify that output pins are TTL high as indicated by a brightly lit 5005 probe light. That is, pins 4, 5, 6, 7, 9 10, 11, and 12 should be TTL high during freerun.

   b. Freerun sets U14 outputs low — Verify that output pins are at TTL low as indicated by an unlit 5005 probe light. That is, pins 4, 5, 6, 7, 9, 10, and 11 should be TTL low during freerun.

      U10 and U14 can also be checked by Diagnostic 16, provided that the keyboard is functional. Refer to "Diagnostics" for detailed information.

If outputs occur which are not expected, verify that the inputs to the control registers are correct by checking freerun signatures. Start by verifying that Low Address lines LA0-2 are correct (consult signatures given for U12 in the following table), then proceed to verify signatures for these components:

PIN	U2	U3	U5	U7	U9	U12
1		6322	9UP2	0001	4632	UUUF
2		37C6	0002	0002	0003	FFFU
3	4FC9	6U2C	0002	486C	4631	8487
4	0003*	C9U1	9UP2	4868	0003(0000*)	70C7
5	0003*	0000*	486C	0003(0000)	C4A7	F2HH
6	0003*	0003*	C9U1	0000	C4A4	0C74
7	0003*	C4A7	0000*	0000*	0000*	2HH3
8	0000*	0000*	0003*	70C4	1F68	0000*
9	A8HP	HHP2	0000	70C7	0003(0000)	C74P
10	2H91	4CFC	0000*	0003*	1F6C	HH3C
11	AUCC	7PP5	0003	0000*	1F6C	74PU
12	79CA	528P	534H	4632	C4A7	H3CP
13	6U2C	4631	4868	4631	A8FF	0003(0000)
14	0000*	A8FF	0003*	0003*	0003*	59PA
15	534H	59PA				0000*
16	0003*	0003*				0003*

NOTE: * probe light not flashing.

NOTE

If incorrect signatures are encountered, backtrace along the signal path from output to input until a device is found where the input shows a correct signature, but the output shows an incorrect one. This particular IC is likely to be the cause of the fault.

Table 8-6. A5 R/W Memory/Decorder Assembly Troubleshooting (Continued)

2. Power up the counter and the 5344A for normal operation and check for frequency or voltage at the indicated pins:

U13

PIN		PIN	
1	0.00V	16	5.0V
2	1 MHz	15	0.99V
3	5.0V	14	0.05V
4	0.16V	13	TTL HIGH
5	TTL HIGH	12	TTL LOW
6	0.02V	11	5.0V
7	0.97V	10	TTL HIGH
8	0.00V	9	1 MHz

U11

1	TTL LOW	20	5.0V
2	TTL HIGH	19	TTL LOW
3	0.00V	18	0.6V
4	3.1 kHz (1.2 kHz)	17	0.2V
5	2.9 kHz (960 Hz)	16	3.0 kHz (1.0 kHz)
6	2.6 kHz (1.0 kHz)	15	2.0 kHz (880 Hz)
7	2.6 kHz (1.1 kHz)	14	2.5 kHz (1.2 kHz)
8	0.2V	13	2.9 kHz (610 Hz)
9	5.0V	12	1 MHz
10	0.00V	11	0.6V

3. U1 — U1 is tested on power-up using a walking ones algorithm. If this check fails, then Err 14 will appear in the 5344A display.

Table 8-7. A3 Keyboard/Display Interrupt Assembly Troubleshooting

Turn off power to the 5344A and place the A3 Assembly on two 05342-60033 extender boards.

1. Power up the counter and the 5344A for normal operation, and verify operation of U3 Keyboard/Display Interrupt IC. Check the pins for listed frequency or voltage:

PIN		PIN	
21	~ 120 kHz	20	0.00 V
22	175 Hz	19	140 Hz (108 Hz)
23	3.9 kHz	18	140 Hz (72 Hz)
24	244 Hz	17	140 Hz (72 Hz)
25	TTL HIGH	16	140 Hz (72 Hz)
26	2.2 kHz	15	140 Hz (36 Hz)
27	1.7 kHz	14	140 Hz (72 Hz)
28	1.7 kHz	13	140 Hz (TTL HIGH)
29	1.7 kHz	12	140 Hz (72 Hz)
30	1.9 kHz	11	140 Hz
31	1.9 kHz	10	35 Hz ± 1 Hz
32	976 Hz	9	TTL LOW
33	488 Hz	8	TTL HIGH
34	244 Hz	7	TTL HIGH
35	122 Hz	6	TTL HIGH
36	TTL HIGH	5	TTL HIGH
37	TTL HIGH	4	TTL LOW
38	TTL HIGH	3	1 MHz
39	TTL HIGH	2	TTL HIGH
40	5.0 V	1	TTL HIGH

Table 8-7. A3 Keyboard/Display Interrupt Assembly Troubleshooting (Continued)

Power-up conditions for transistors Q1-Q4. Check the pins for the listed frequency or voltage:

Q1

PIN		PIN	
8	1.6 kHz (1.3 kHz)	7	2.4 kHz (2.0 kHz)
9	4.5 V	6	4.8 V
10	4.8 V	5	4.8 V
11	0.0 V	4	0.0 V
12	4.8 V	3	4.8 V
13	4.6 V	2	4.8 V
14	1.6 kHz (1.1 kHz)	1	2.4 kHz (1.8 kHz)

Q2

PIN		PIN	
8	2.1 kHz (2.0 kHz)	7	2.0 kHz (1.6 kHz)
9	4.5 V	6	4.6 V
10	4.8 V	5	4.8 V
11	0.0 V	4	0.0 V
12	4.8 V	3	4.8 V
13	4.5 V	2	4.6 V
14	2.1 kHz (1.8 kHz)	1	1.9 kHz (1.6 kHz)

Q3

E	5.0 V
B	4.1 V
C	4.9 V

Q4

	5.0 V
	4.1 V
	4.9 V

Powerup conditions for Interrupt FF U7. Check the pins for the listed frequency or voltage.

U7

PIN		PIN	
9	35 Hz	8	0.00 V
10	35 Hz	7	4.0 V
11	35 Hz	6	4.4 V
12	5.0 V	5	4.0 V
13	4.0 V	4	4.0 V
14	4.0 V	3	5.0 V
15	4.9 V	2	4.9 V
16	5.0 V	1	4.0 V

Table 8-7. A3 Keyboard/Display Interrupt Assembly Troubleshooting (Continued)

2. Troubleshoot using Signature Analysis

   Place the counter in freerun by following the directions given in the service manual under "A14 Microprocessor Troubleshooting". Verify that the characteristic 0003 signature (probe light brightly lit) occurs when +5V is probed, and that the characteristic 0000 signature (probe light not lit) occurs when ground is probed.

PIN	U2	U4	U5	U6	U8
1	86CP	7PP5	UUUF	0003*	P1AF
2	86CH		FFFU	0003*	0000*
3	0000		8487		
4	0003		0000		0000*
5			4CFC	0003*	
6			0003*	0003*	0003*
7	0000*		U723		
8			0000*		
9			CHFC	0003*	
10	0000	0000*	AU71	0000*	0000*
11	0003	F82H	6CHU	C86C	0003*
12	0003*	F82H (0000)	1AU4	0003*	
13	0000*	F82H	86CP		
14	0003*	34CC (UF96)	P1AF		
15		F82H (0000)	C868		0000*
16		F82H (0000)	0003*	0003*	
17		0000			0000*
18		0000 (F82H)			
19		7PP5		H04P (blank)	P1AF
20		0003*		0003*	0003*

NOTE: * indicates that the probe light is NOT blinking. Blanks indicate meaningless or unstable signatures.

NOTE

If incorrect signatures are encountered, backtrace along the signal path from output to input until a device is found where the input shows a correct signature, but the output shows an incorrect one. This particular IC is likely to be the cause of the fault.

3. Check for correct operation of Timer IC U14.

   Monitor U14(3) and check for a timing signal of 35 (±1) Hz. If this signal is incorrect, verify timer circuitry.

4. Verify correct operation of Interrupt Gating circuitry.

   Interrupt gating is performed by ICs U9-U11. To verify operation, check for these conditions at power up of the counter and the 5344A:

   U9, U10 — use simple NAND gate logic to verify operation of these ICs.

   U11 — check for an inverted signal of 35 Hz from pin 11 to pin 8. The remaining input pins are TTL high, so the only pins of interest are input pin 11 and output pin 8.

Table 8-7. A3 Keyboard/Display Interrupt Assembly Troubleshooting (Continued)

5. Verify Clock Generator U12

   Monitor U12(8) and check for a signal of approximately 1 MHz. Also, the signal appears similar to $\phi 2$ when observed with an Oscope. If this signal is not present, verify that the inputs are correct. Signals $\phi 2$, $\phi 2M$, and LRD may be compared to the test pins on board A11.

6. Verify Rotary Pulse Generator (RPG) FF U1

   Check outputs of this FF while rotating the RPG as indicated:

   Pin 5 — monitor this pin while rotating the RPG. The output should stay TTL low independent of direction.
   Pin 9 — monitor at power up: TTL high
   — monitor while rotating the RPG clockwise: goes TTL low and stays low
   — monitor while rotating the RPG counterclockwise: goes TTL high and stays high

Table 8-8. A1 Keyboard/Display Assembly Troubleshooting

1. If possible, use Diagnostics 1 and 2 to check the keyboard and LEDs. Refer to *Table 8-9*, Diagnostics for further information. If these can be performed, then there is a high probability that the keyboard and display LEDs are operating correctly. If this is not the case, then proceed by disassembling the front panel as instructed in paragraph 8-26.
2. Power up the counter and the 5344A for normal operation, and verify operation of the U9 Scan Line Decoder. Check the pins for the listed frequency or voltage:

U9

PIN		PIN	
1	244 Hz	9	488 Hz
2	0.03 V	10	244 Hz
3	488 Hz	11	488 Hz
4	244 Hz	12	244 Hz
5	488 Hz	13	976 Hz
6	244 Hz	14	0.03 V
7	732 Hz	15	244 Hz
8	0.03 V	16	5.0 V

If signals are not as expected, then the IC or High Scan Line (HSL) information from A3 may be faulty.

3. Verify operation of Display Drivers U1-U5,U7,U8,U10

Check for these power up frequencies:

LSL3 at U1(2): 122 Hz
HSL3 at U2(2): 122 Hz

then check the following outputs of the display drivers:

IC	Pin 3	Pin 5
U1	1.7 kHz	976 Hz
U2	1.7 kHz	1.6 kHz
U3	1.5 kHz	1.6 kHz
U4	1.4 kHz	1.5 kHz
U5	1.4 kHz	1.3 kHz
U7	1.4 kHz	1.1 kHz
U8	1.1 kHz	976 Hz
U10	1.1 kHz	1.1 kHz

Table 8-8. A1 Keyboard/Display Assembly Troubleshooting (Continued)

4. Verify operation of U6 Bar Graph Driver

   Check for the following power-up levels at the indicated pins.

PIN		PIN	
1	1.3 V	10	3.58 V
2	0.02V	11	3.58 V
3	4.9 V	12	3.58 V
4	0.02 V	13	3.58 V
5	1.97 V	14	3.15 V
6	3.80 V	15	1.72 V
7	3.80 V	16	1.19 V
8	2.06 V	17	1.19 V
9	.9 V	18	1.23 V

5. Verify operation of Rotary Pulse Generator (RPG)

   Initial Check:
   Power up the counter and the 5344A. Using a 5005 data probe in the kHz mode, monitor the RED/BLK and BR/BLK nodes on the A1 assembly, (location of the nodes are shown in the photo of the board below). Rotate the RPG clockwise and counterclockwise and observe that the probe light blinks to indicate a change in state.

   Further Check:
   Power-up the counter and the 5344A for each of these checks.

   RED/BLK Node: Probe this node (see photo) and slowly turn the RPG clockwise. Note that the 10 kHz position digit changes only while the data probe light is lit. The probe light should be changing state from lit to unlit as the RPG is rotated.

   Now turn the RPC counterclockwise. Note that the 10 kHz position digit changes on the unlit-to-lit transition of the probe light.

   BR/BLK Node: Probe this node (see photo) and slowly turn the RPG clockwise. Note that the 10 kHz position digit changes on the unlit-to-lit transition of the probe light.

   Now turn the RPG counterclockwise. Note that the 10 kHz position digit changes only while the data probe light is lit.

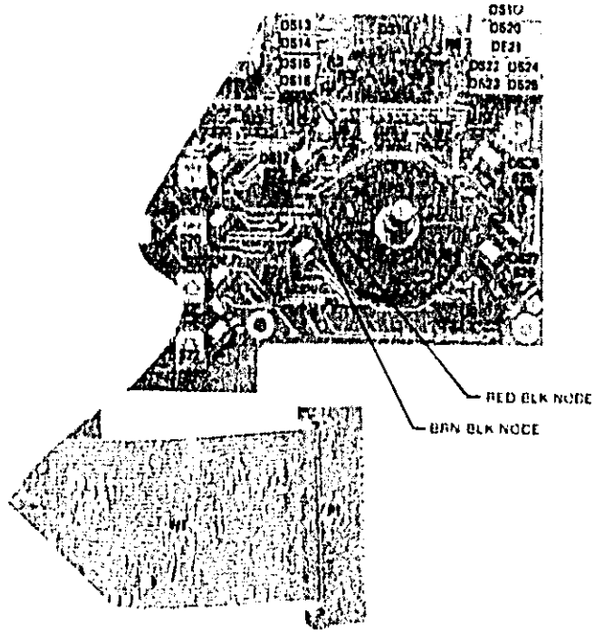


Table 8-9. Diagnostics

If you have reached this portion of the troubleshooting, it is assumed that the kernel is functional, and that it has been verified for correct operation.

The next step in the troubleshooting flow is to execute diagnostics to isolate the fault to an assembly or component.

Begin with the Self Test Description, then proceed to the Diagnostics Description which details the diagnostics and provides an order in which to perform them. For any failed diagnostic, refer to step 5 which gives the suspected assembly or component which may be at fault for that diagnostic.

The diagnostic tests check the instrument by functional block in the order given below:

FUNCTIONAL BLOCK	ASSEMBLY/ASSEMBLIES
Main Loop	A6
Phase Lock Loop	A7, A9, and A10
10 V Ramp	A8
HP-IB/Ramp	A4

1. Self Test Description

   On power up, the 5344S performs its self test routine. If all tests pass, the 5344S performs its initialization and then passes control to the 5342A/5343A which performs its own self test and proceeds to freerun (5342A/5343A counting, 5344S idle).

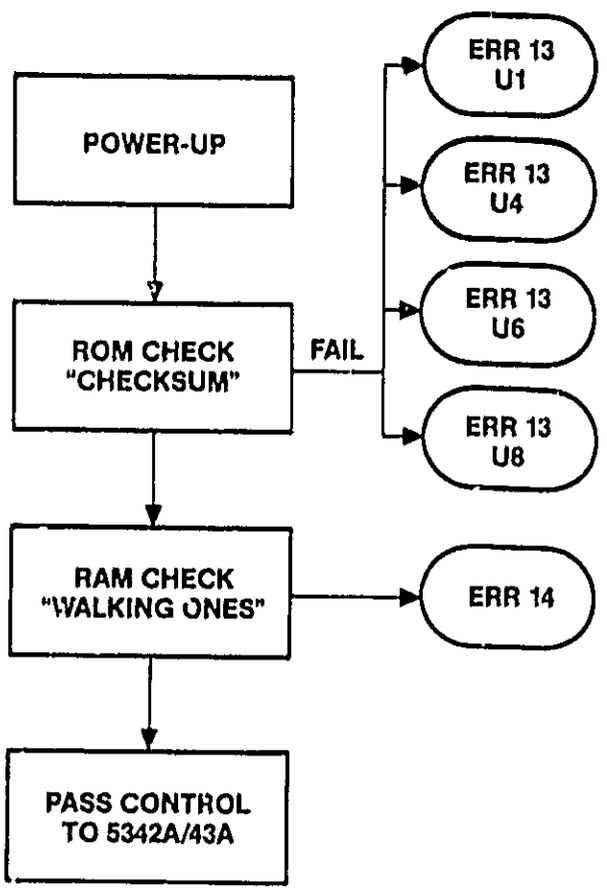


Table 8-9. Diagnostics (Continued)

The following tests are performed on power up:

ROM CHECK. The 5344S has four 4K EPROMS or two 8K PROMs. These are tested during the power up self test by performing a checksum calculation and comparing the result with the checksum stored in the PROM. (Checksums are calculated for each 4K block of code. Therefore, when 8K PROMs are being used, each one has two checksums). If the computed checksum (2 bytes) does not match the stored checksum, ERR 13 is displayed along with an indication of the error:

DISPLAY	4K PROMs	8K PROMs
U1	U1	U1 (low half)
U4	U4	U4 (low half)
U6	U6	U1 (high half)
U8	U8	U4 (high half)

RAM CHECK. All bytes in RAM are initialized and a series of write-read-compare sequences is done using the "walking ones" algorithm*. Each bit pattern is stored at the currently addressed location. That location is then read back and compared to the pattern. Any mismatches are considered errors. Each byte is checked for initialization. If it is not initialized, it is considered to be affected by some other change and is treated as an error. All RAM CHECK errors display "Err 14".

* The "walking ones" algorithm is as follows: the initial bit pattern is 0000 0001, with each following pattern shifting the one "on" bit left one position. The resulting series is 0000 0001, 0000 0010, 0000 0100, etc. In this way, each bit is forced to go low→high and then high→low again.

2. Diagnostics Description

The diagnostics consist of a series of tests designed to troubleshoot problems with the Keyboard/Display circuits, the Main Loop board, Fractional N chip, VCO and Ramp generation circuits. The diagnostics are entered by pressing the F2 key on the front panel of the 5344A, while in the Lock/Roll mode. At this point the 5344A display will fill with a row of "d's". Then enter a one or two digit test number (X) and press RESET. The 5344S is then prepared to execute test X.

It is necessary that the 5344S NOT be locked in Lock/Roll, and NOT be in single sweep mode. If, after F2 is pressed, a key other than a number is pressed, the 5344S will ignore that key. The exception is another function key, which will cause the 5344S to go to that function.

Once in the diagnostic mode, moving on to a different test can be accomplished in either of two ways, as follows:

a. The UP-arrow and DOWN-arrow keys can be used to scroll through the tests sequentially. For example, while in Diagnostic 3, pressing UP-arrow moves control on to Diagnostic 4, while DOWN-arrow key moves control to Diagnostic 2.

If Diagnostic 1 is the current test, the DOWN-arrow key is processed according to the Diagnostic 1 procedure listed below. If the current test is the last one, the UP-arrow has no effect.

If Diagnostic 15 is the current test, the UP-arrow will be ignored. If Diagnostic 16 were to be accidentally entered in this way, there would be no way to guarantee recovery. Therefore, the only way to enter Diagnostic 16 is through number entry. Similarly, Diagnostic 17 cannot be entered using the arrow keys.

b. Pressing another one- or two-digit test number and RESET will change operation to that test. If a three-digit (or some other invalid) sequence is entered, the sequence will be ignored and control returned to the previous diagnostic. If the first key sequence after entering the diagnostic mode is invalid, the 5344S will default to Diagnostic 1.

NOTE

To exit the diagnostic mode, press the RESET key twice. The 5344S then reinitializes and returns to a "warmstart" routine.

Table 8-9. Diagnostic (continued)

3. Diagnostic Procedures

DIAGNOSTIC 1

To enter Diagnostic 1 (with the 5344S system interconnections as shown in *Figure 4-1*), apply power, press the MODE key repeatedly until LK/R appears on the 5344A display, then press the F2 key. Press the numeric 1 key, then press RESET. Press each of the keys listed below for the display indicated in the leftmost digits (the diagnostic number d1 will appear in the rightmost digits):

Key ..... Display	Key ..... Display	Key ..... Display	Key ..... Display
MODE ..... dd	7 07	8 08	9 09
F1 ..... F1	4 04	5 05	6 06
F2 ..... F2	1 01	2 02	3 03
SWP TIME ..... St	0 00	. ...	ACQUIRE .... AC
MKR FREQ .... EE			
STEP SIZE ..... SS			
GHz/s ..... gh	FINE/	MANUAL	
MHz/ms ..... HH	COURSE ..... FC	LOCK LL	
Up arrow*			
Down arrow .. dn	RESET ..... rt	AUTO ..... AL	

**UP arrow will advance control to Diagnostic 2. This is the only way to exit from Diagnostic 1.*

DIAGNOSTIC 2

Enter Diagnostic 2 from Diagnostic 1 by pressing the Up arrow key. This test illuminates all front panel lights.

NOTE

Diagnostics 3 through 10 test various combinations of states on A6 Main Loop board. Tests that require an input signal to the counter or monitoring with an oscilloscope are so indicated. Additional information is given for Diagnostics 3 through 8 to indicate the condition of certain control signals. This informaton can be used to verify that the control signals are as expected. For example, Diagnostic 4 indicates that both the Wide Band and the Narrow Band amplifiers, A6U10A and U10C, outputs are off (disconnected from TP5), the gain of Variable Gain Amplifier U11 is 5 (although difficult to monitor), and the TICKLE signal input to transistor Q3 is toggling (see *Figure 8-29*). The expected FM OUT signal waveform is shown in the illustration.

DIAGNOSTIC 3

NOTE

For Diagnostics 3 through 6, connect an oscilloscope such as an HP 1725A to FM OUT of the 5344A.

This test verifies operation of the output amplifier and tickle voltage.
Conditions:

- NB off
- WB off
- TICKLE off
- HOLD off
- Full Gain

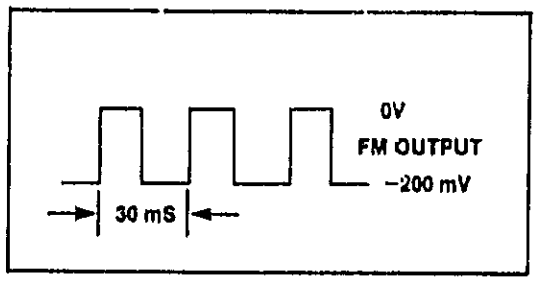
Expected results: FM OUTPUT = 0.00(±0.02) volts

Table 8-9. Diagnostics (Continued)

DIAGNOSTIC 4

This test verifies operation of the output amplifier and tickle voltage.
Conditions:
- NB off
- WB off
- HOLD off
- Gain = 5
- Oscillate TICKLE on/off (30 ms period)

Expected results: See waveform below



DIAGNOSTIC 5

This test verifies operation of the HOLD circuit. The output may drift as much as 4 mV/second.
Conditions:
- NB off
- WB off
- TICKLE on/off (30 ms period)

Expected results: FM OUTPUT = –200 mV.

DIAGNOSTIC 6

This test verifies operation of the variable gain amplifier under microprocessor control.
Conditions:
- NB off
- WB off
- TICKLE on
- HOLD off
- Step Gain from 0 to 255, repeat

Expected results: See waveform below

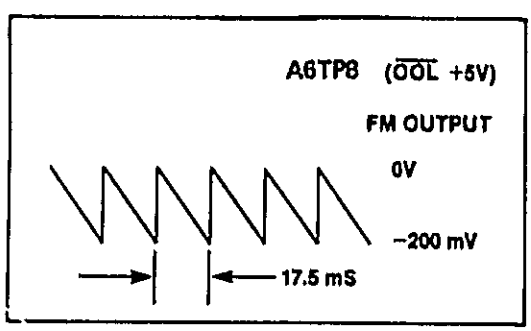


Table 8-9. Diagnostics (Continued)

NOTE

For diagnostics 7 and 8 the FM OUTPUT must not be connected to the source used to provide the counter input signal. Connect the 5344S in the test setup shown below.

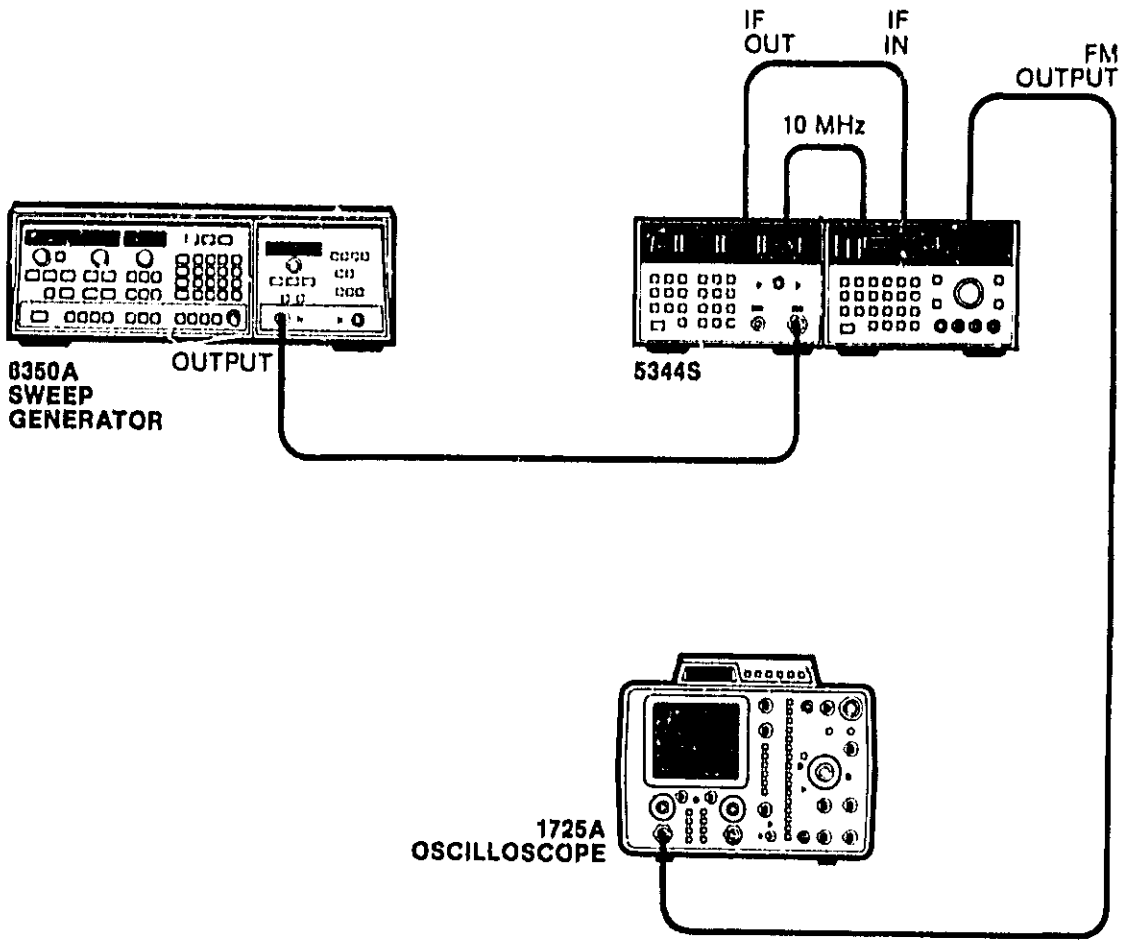


Table 8-9. Diagnostics (Continued)

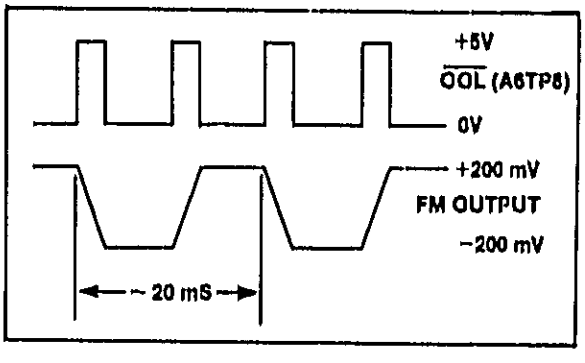
DIAGNOSTIC 7

This test verifies operation of the phase detector and loop amplifier. If the counter input signal is at the minimum specified level, the operation of the IF input amplifiers is checked. The test is performed for Wide Band mode of operation only.

Conditions:

NB off
WB on
TICKLE off
HOLD off
Gain = 1/50
Oscillate polarity on/off (20 ms period)

Expected result: See waveform below



DIAGNOSTIC 8

Repeats diagnostic 7 in the Narrow Band mode of operation. Same test setup.

Conditions:

NB on
WB off
TICKLE off
HOLD off
Gain = 1/50
Oscillate polarity on/off (440 ms period)

Expected results: See waveform below

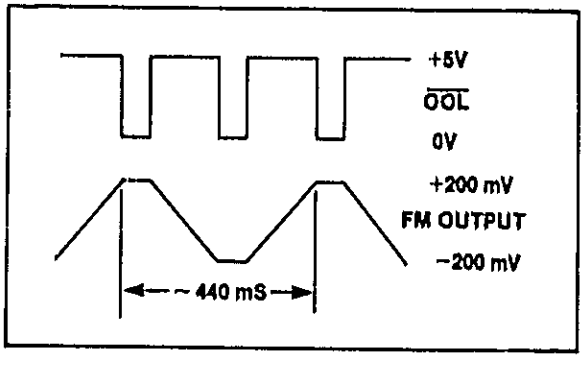
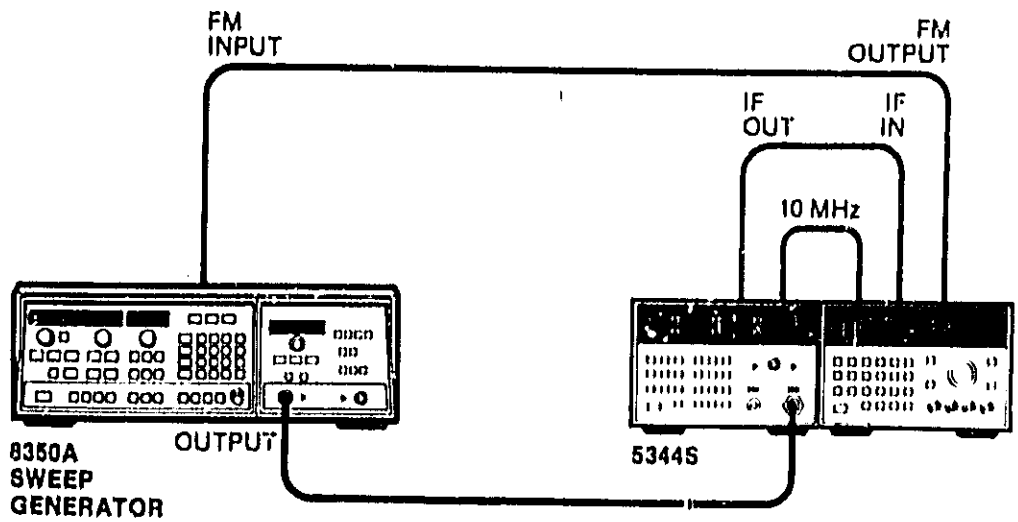


Table 8-9. Diagnostics (Continued)

NOTE

For Diagnostics 9 and 10, connect the 5344s in the test setup shown below.



DIAGNOSTIC 9

Measures the appropriate IFs to calculate the sensitivity in MHz/volt which is displayed (XX.X) on the 5344S.

DIAGNOSTIC 10

Overrides processor control of the loop, forcing it closed. Masks the Out-of-Lock interrupt and locks to the CW frequency entered. The IF of the lock frequency is displayed on the 5342A (5343A). After getting to Diagnostic 10, the CW frequency may be entered after pressing F1 key.

NOTE

Diagnostics 11 through 13 are concerned with the Fractional N chip and the VCO circuits. Use an oscilloscope, such as the HP 1725A to monitor the test points or signals indicated in Diagnostics 11 through 17.

DIAGNOSTIC 11

Locks the Fractional N Synthesizer to a frequency of 25 MHz (lower limit).

Expected results: Tuning Voltage at A9TP2 = 10.8 volts

DIAGNOSTIC 12

Locks the Fractional N Synthesizer to a frequency of 50 MHz (upper limit).

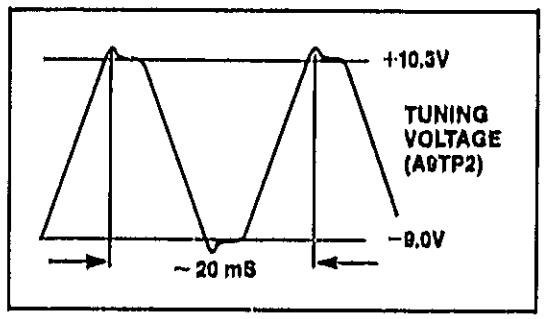
Expected results: Tuning Voltage = <1 volt.

Table 8-9. Diagnostics (Continued)

DIAGNOSTIC 13

Performs a locked sweep (no markers) with a Delta F of 25 MHz. (Start frequency = 25 MHz, Stop frequency = 50 MHz).

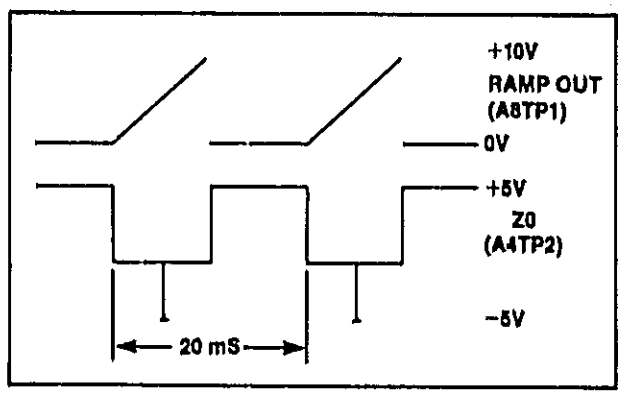
Expected result: See waveform below



DIAGNOSTIC 14

Checks the Ramp and Z-axis circuits by performing the same test as Diagnostic 13 with the addition of one marker at a frequency of 37.5 MHz.

Expected results: See waveform below



DIAGNOSTIC 15

Allows adjustment of the A8 RAMP OUT 10-volt ramp.

Expected result: A8TP1 = 10 volts

Table 8-9. Diagnostics (Continued)

DIAGNOSTIC 16

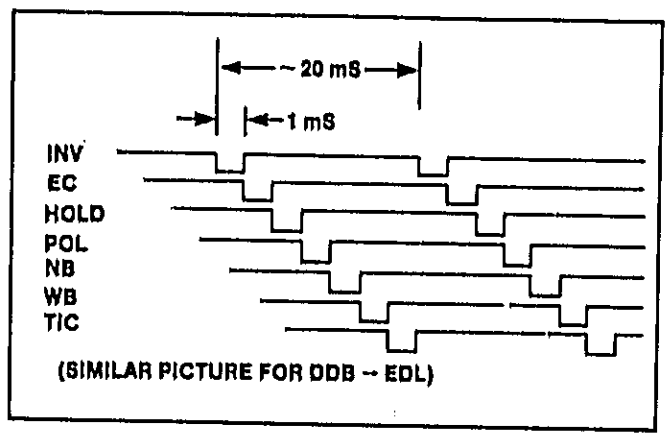
NOTE

To perform Diagnostic 16, unsolder one end of jumpers W1 and W2 on A5 board.

When the test is completed, resolder the jumpers and power up the 53445.

This diagnostic verifies the digital control lines from the Control Decoders on the A5 board (see schematic diagram, *Figure 8-28*). The control lines are toggled in specified order (outputs of A5U14, and A5U10).

Expected results: See waveforms below for the A5U14 outputs. The A5U10 output waveforms are similar (DDB to EDL signals).



DIAGNOSTIC 17

This test sets a memory flag to disable AUTO LOCK HP-IB timeout error. No visible effect except the display indicates the diagnostic is being performed.

5. Diagnostics Versus Suspected Faulty Assembly/Component

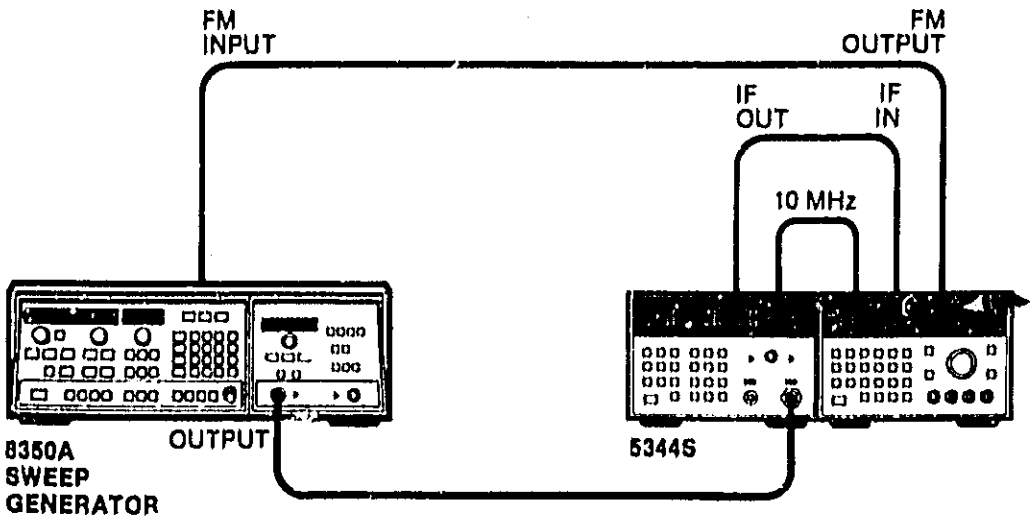
Diagnostic	Suspected Assembly	Component
1	A1, A3	
2	A1, A3	
3	A6	U11, U12, Q6, Q7
4	A6	U11, U12, Q6, Q7
5	A6	U9
6	A6	U11
7	A6	U7, K1, K2
8	A6	U7, K1, K2
9	A6	
10	A6	
11	A7, A9, A10	
12	A7, A9, A10	
13	A7, A9, A10	
14	A4, A8	
15	A8	
16	A5	U10, U14
17	Used for software purposes only	

NOTE

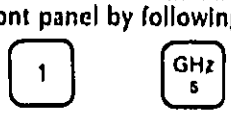
Table 8-10 on the following page provides additional information to isolate the fault within the Phase Lock Loop Circuitry.

Table 8-10. Phase Lock Loop Overall Troubleshooting

1. Power down the 5344A and remove the A9 Analog Assembly. This disconnects the VCO control voltage from the A7 VCO Assembly.
2. Place the A7 Assembly on extender board 05342-60030, and power up the counter and the 5344A.
3. Measure the frequency of the signal at A7U1 pin 14. The frequency should be 40 (±5) MHz. Also, this frequency should be present at the collector of transistor A7Q4, and at the emitters of Q5 and Q6. If the frequency is correct, proceed to step 4. If the frequency is not correct, measure dc voltages as given in *Table 8-13*, A7 VCO Assembly Troubleshooting, to isolate the defective component.
4. Power down the 5344A and reinstall the A9 Analog Assembly.
5. Make the necessary connections to the counter, 5344A, and the frequency source to make a CW manual lock. Consult the figure given here for these connections. Power up the counter, 5344A, and the source.



6. Set the source frequency to 1.000 XXX XXX GHz as indicated on the counter display. Key in 1.000 000 000 GHz on the 5344A front panel by following this key sequence:



7. Enter Diagnostic 10 (See *Table 8-9*). A properly operating instrument will show the stable IF frequency in the counter display, 1.000 000 000 GHz in the 5344A display, and the LOCKED annunciator of the 5344A lit. In addition, the LED on the A7 VCO Assembly, DS1, will be off.

   Measure the voltage levels at A7U2 Pins 1 and 7. This phase lock loop circuitry is probably operating correctly if the level at both pins is approximately -13 Volts, and the LED is off as stated in the above paragraph.

   If this is not the case, then one pin will be approximately +13 Volts, and the other approximately -13 Volts. Connect an oscilloscope probe to A9TP1 and proceed to step 8.

8. If A7U2 pin 1 is positive, and:
   - the signal at A9 TP1 is positive, then suspect the Integrator, Bias, or Sample and Hold circuitry on the A9 Assembly.
   - the signal at A9 TP1 is negative, then suspect the divide-by-N.F circuitry on the A10 Assembly, or the Phase Comparator circuitry on the A9 Assembly.

   If A7U2 pin 7 is positive, and:
   - the signal at A9 TP1 is positive, then suspect the divide-by-N.F circuitry on the A10 Assembly, or the Phase Comparator circuitry on the A9 Assembly.
   - the signal at A9 TP1 is negative, then suspect the Integrator, Bias, or Sample and Hold circuitry on the A9 Assembly.

Table 8-11. A4 HP-IB Interface/Ramp and Z Axis Assembly Troubleshooting

The A4 Assembly consists of two separate blocks of circuitry. The first of these is the HP-IB Interface circuitry. The other is the Ramp and Z Axis circuitry. The troubleshooting information is divided into these two areas. Refer to the schematic diagram, *Figure 8-27*.

HP-IB Interface

1. To verify correct operation of the HP-IB portion as well as the 5344A in general, run the HP-IB Operation Verification tape. Information relating to this can be found in Section IV, Performance Tests.
2. If the unit does not behave as expected during the course of the tape, or a problem is suspected with the HP-IB circuitry, then the recommended procedure is to swap out the HP-IB chip, A4U3. Since this is in a socket, it should be fairly easy to check for correct operation of this part by swapping (provided that another is readily available).

   If the above step does not help to isolate the fault, then it is recommended that the following ICs be changed out in this order: Receiver U6, Receiver U7, then Bus Driver U4.

Ramp and Z Axis

Place the A4 Assembly on two 05342-60033 extender boards.

Z Axis Circuitry —

Observe the following waveforms for U2D during Diagnostic 14.

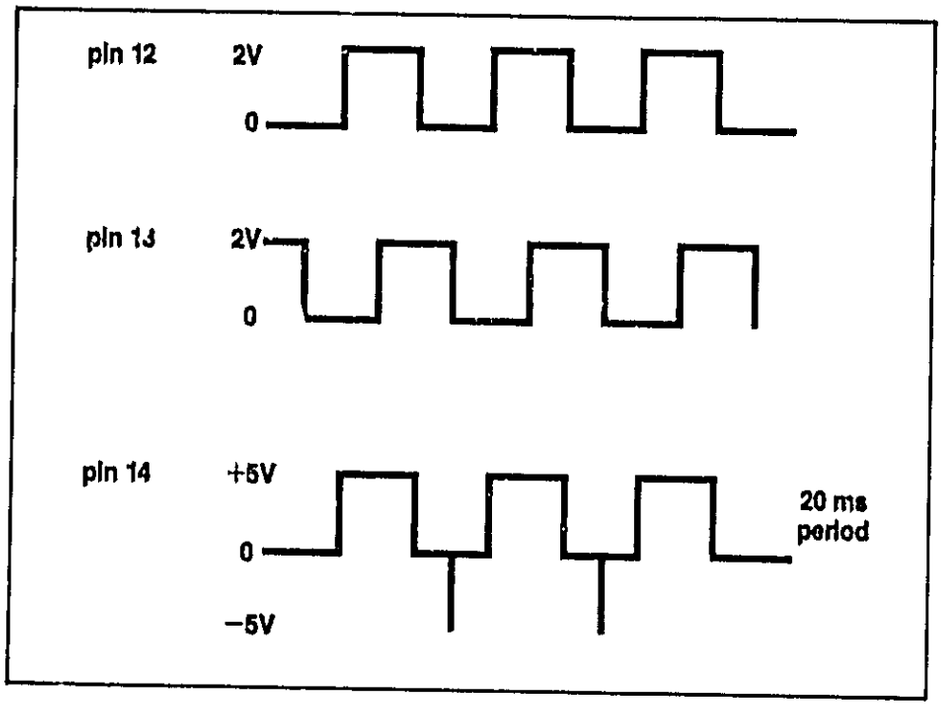


Table 8-11. A4 HP-IB Interface/Ramp and Z Axis Assembly Troubleshooting (Continued)

Also note that the signal at TP2 (ZO) resembles the signal present at U2 pin 14.

Z Axis and 10V Ramp Select Circuitry —

Note that the circuitry used to implement the selection for each of these is identical. This fact can be helpful in that suspect portions of one circuit can be compared against the same portion of the other to verify operation. DC levels at power-up should prove to be helpful.

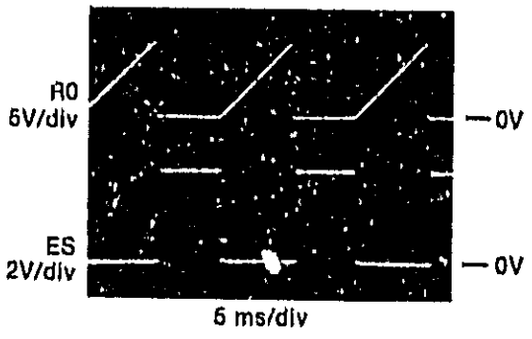
Enter Diagnostic 14 (see *Table 8-9*) and observe that the waveform present at TP2 (ZO) resembles that at U2 pin 14 as mentioned above, and that this same waveform is present at all nodes of FET Q5.

Also in Diagnostic 14, note that the waveform present at TP3 (RO) also appears at all nodes of FET Q16. The RO waveform for Diagnostic 14 appears in the next step under EOS Circuitry.

EOS Detec Circuitry —

Use a BNC cable to connect the 5344A front panel SWEEP OUT connector to the SWEEP IN connector.

Enter Diagnostic 14 and observe that the waveform present at the RO test point is now present at U2 pin 3. The following photo gives the waveforms at the RO and ES test points during this diagnostic:



Trace the ramp waveform at U2 pin 3 to U2 pin 1, to pin 7 of U1 and U2 as a square waveform, and finally to the ES test point.

Waveforms similar to that at U2 pin 7 also occur at U2 pin 8 and U1 pin 1.

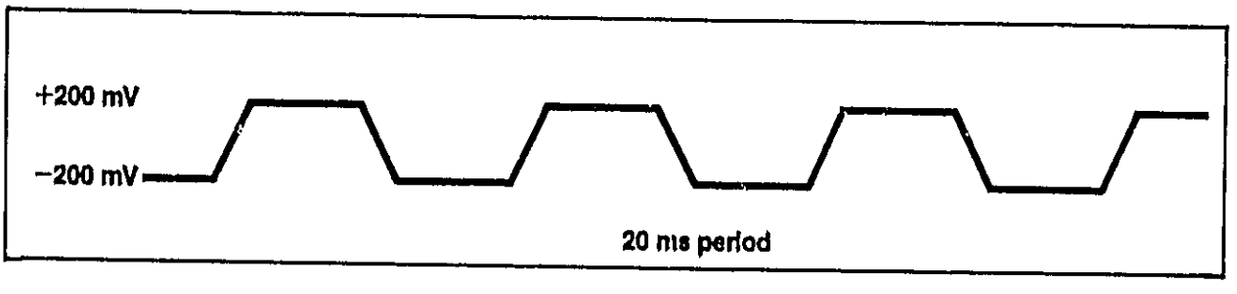
Table 8-12. A6 Main Loop Assembly Troubleshooting

1. Check the following test points to verify proper operation of the A6 Assembly. Power up the counter and the 5344A for normal operation and proceed:

		SUSPECT
TP 1 (V)	12 MHz ECL (~50 MHz ECL)	U5
TP 2 (POL):	ECL LOW	U6
TP 3 (R) :	ECL HIGH (~20 MHz ECL)	U5
TP 4 (GND) :	0.00 V	Power Supply
TP 5 (S/H) :	0.00 V	U10, K1, K2
TP 6 (D/A) :	0.00 V	U9
TP 7 (FM OUT) :	0.00 V	U11, U12
TP 8 ($\overline{OOL}$) :	TTL HIGH	
TP 9 (TEST IN) :	FLOATING	U11, U12
TP 10 (TEST OUT) :	0.00 V	

Enter Diagnostic 7 (see *Table 8-9*) and verify the following levels and frequencies without an input signal applied:

		SUSPECT
TP 1 (V) :	8 MHz ECL (37 MHz ECL)	
TP 2 (POL) :	54 Hz ECL	
TP 3 (R) :	8 MHz ECL (37 MHz ECL)	Consult table above for suspect assembly/ component.
TP 4 (GND) :	0.00 V	
TP 5 (S/H) :	54 Hz	
TP 6 (D/A) :	54 Hz	
TP 7 (FM OUT) :		



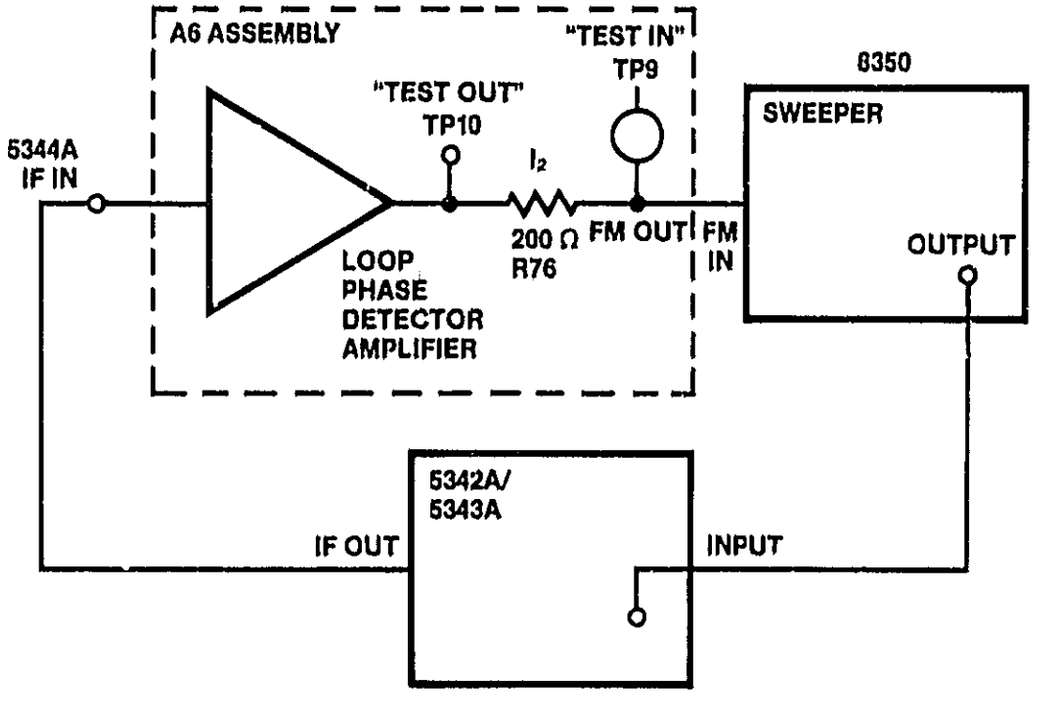
TP 8 ($\overline{OOL}$) :	106 Hz (TTL High)
TP 9 (TEST IN) :	FLOATING (54 Hz)
TP 10 (TEST OUT):	Same signal as shown for FM OUT under Diagnostic 7

If the measured signals do not agree with the documented ones, it is likely that the A6 Assembly is not operating correctly. Place the A6 Assembly on extender board part number 05342-60043 and proceed.

Table 8-12. A6 Main Loop Assembly Troubleshooting (Continued)

An alternate check of the A6 board is provided here. This is a loop response test which allows verification of the A6 Assembly operation.

If the response obtained is the same as the waveform given, then there is a high probability that all components in the loop are operating correctly. The setup for this test is given here:



The principle of this test is to inject a signal into the FM port of the sweeper, attempting to pull the frequency. If the frequency of the injected signal is low, the loop will operate to cancel its effect by generating a current opposite and equal to that injected.

The loop response with frequency is viewed by displaying the signal "Test Out" on a spectrum analyzer with the injected signal provided by the tracking generator of the analyzer.

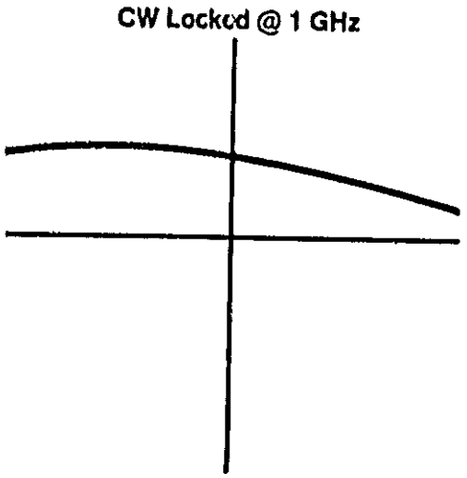
Connect an HP 8556A to the 5344A as follows (with other connections as given in the previous figure):

- 8556 TRACKING GEN OUT to 5344A A6 test point "TEST IN"
- 8556 INPUT to 5344A test point "TEST OUT"
- 8556 input level -50 dBm

scan width	20 kHz 0-10f
bandwidth	3 kHz
scan time	5 msec
log ref level	0 dBm 10 dB log

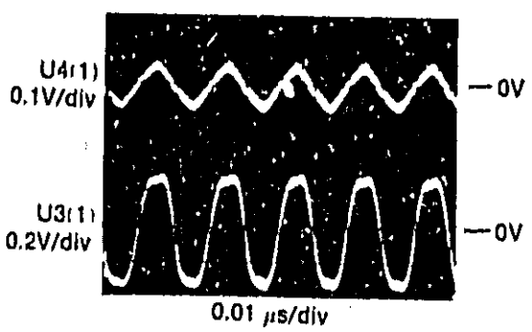
Table 8-12. A6 Main Loop Assembly Troubleshooting (Continued)

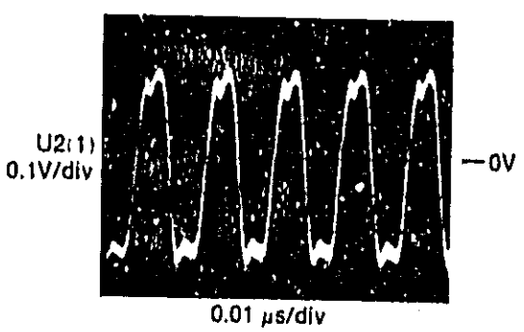
Adjust the Tracking Generator Level to get the display as shown. The vertical position is not important - only the shape of the curve.



2. Verify operation of Amplifiers/Limiters U2-U4.

   These components can be checked by consulting the Oscope photos given below. These photos were taken with Fin equal to 1.000 XXX XXX GHz.





3. Verify operation of ECL FF U1.

   Look for division by two of the input signal. The input occurs at pin 11 and the output occurs at pin 10. Compare with these scope photos. The input signal applied to the counter is 1.000 XXX XXX GHz.

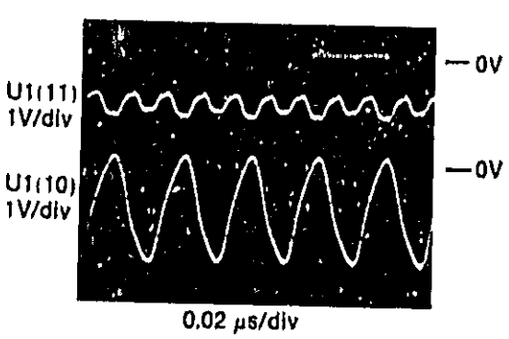
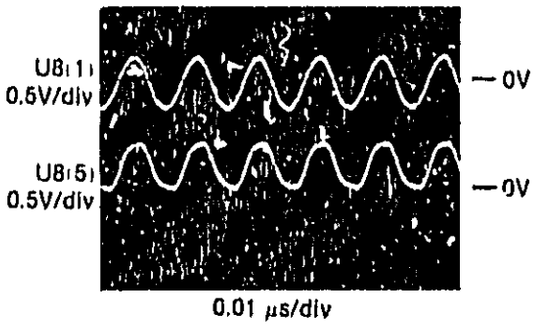


Table 8-12. A6 Main Loop Assembly Troubleshooting (Continued)

4. Verify operation of Amp Limiter U8.

   Compare input/output with these scope photos. No input signal is needed.



5. Verify operation of ECL NOR Gate U5.

   Check for correct operation by examining inputs and outputs during Diagnostic 7.

   Enter Diagnostic 7 and verify the following:

	Inputs	Outputs
Pin 4 Pin 5 Pin 6 Pin 7	8 ±1 MHz (20 MHz) 54 ±2 Hz ECL HIGH (51 MHz) 54 ±2 Hz	Pin 2 7 MHz (37 MHz)
Pin 10 Pin 11 Pin 12 Pin 13	8 ±1 MHz (20 MHz) 54 ±2 Hz ECL HIGH (51 MHz) 54 ±2 Hz	14 8 MHz (37 MHz)

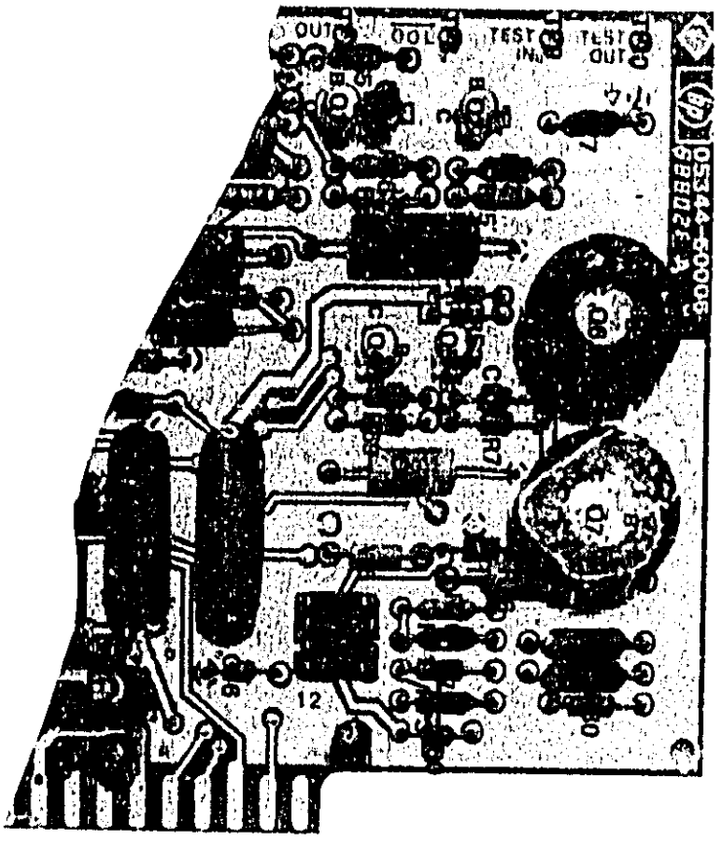
6. Verify operation of transistors Q1-Q7.

   Check for proper levels of the given transistors at power up. Consult the table given below.

   Power up the counter and the 5344A for normal operation and verify the following levels:

Q	E	B	C
1	0.00 V	-1.1 V	4.9 V
2	5.0 V	4.9 V	0.0 V
3	0.00V	0.2 V	4.9 V
4	0.00 V	0.13 V	4.9 V
5	0.00 V	0.13 V	4.9 V
6	0.5 V	1.1 V	15.0 V
7	-0.5 V	-1.1 V	-15.0 V

Table 8-12. A6 Main Loop Assembly Troubleshooting (Continued)



7. Verify operation of Sample and Hold IC U9.

   Check for correct operation of this component by comparing scope photos provided for inputs and outputs during Diagnostic 7.

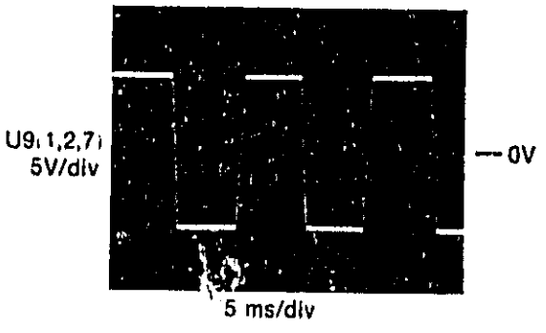
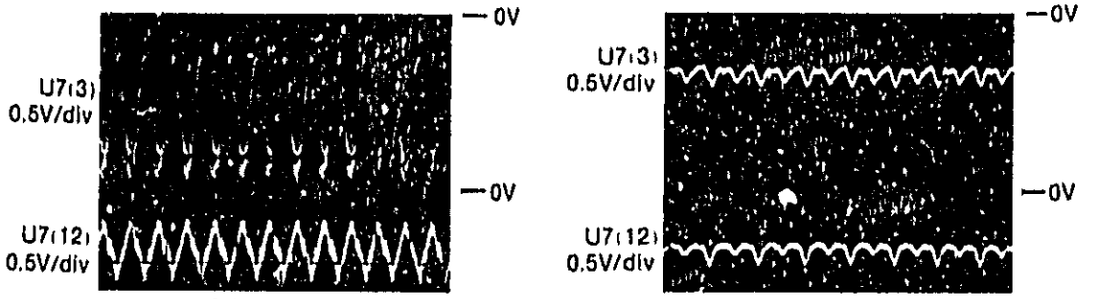


Table 8-12. A6 Main Loop Assembly Troubleshooting (Continued)

8. Verify operation of Phase Lock Loop IC U7.

   Check for correct operation of this component by comparing scope photos provided for inputs/outputs.



9. Verify operation of Op Amp U10.

   Check for correct behavior of this IC by comparing outputs with inputs as given below for power up conditions and during Diagnostic 7.

   Power up the counter and the 5344A for normal operation and observe the following voltage levels at the indicated pins. Quite simply, the output state can be determined from the input levels and the polarity of each input.

   Power-up conditions (note that voltage levels are approximate – values should be within 10%).

Inputs		Outputs	
Pin 2	-1.3 V	Pin 1	14.5 V
Pin 3	-0.8 V		
Pin 5	-10.3 V	Pin 7	-13.7 V
Pin 6	0.0 V		
Pin 9	-1.2 V	Pin 8	14.5 V
Pin 10	-0.8 V		
Pin 12	0.0 V	Pin 14	-13.7
Pin 13	10.3 V		

Enter Diagnostic 7 (see *Table 8-9*) and verify the following levels/frequencies:

Inputs		Outputs	
Pin 2	-0.9 V	Pin 1	54 Hz
Pin 3	-0.9 V		
Pin 5	-10.3 V	Pin 7	54 Hz
Pin 6	54 Hz		
Pin 9	-0.85 V	Pin 8	14.5 V
Pin 10	-0.84 V		
Pin 12	54 Hz	Pin 14	54 Hz
Pin 13	10.3 V		

Table 8-12. A6 Main Loop Assembly Troubleshooting (Continued)

10. Verify operation of Relays K1 and K2.

    Power up the counter and the 5344A for normal operation. Both relays should be open. This condition can be verified by observing levels at pins 1 and 4 of each relay and noting that they are different.

    Enter Diagnostic 7 and verify that relay K1 is open and K2 is closed. Conditions can be checked once again by comparing levels at pins 1 and 4 for K1, and by observing a 54 Hz signal present at pins 1 and 4 of K2.

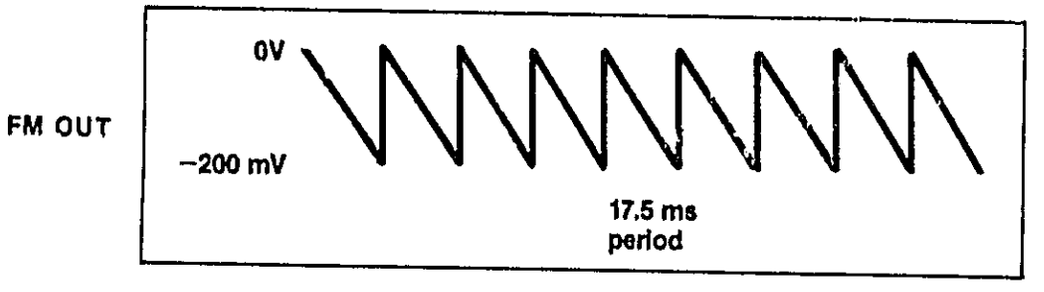
    Enter Diagnostic 8 and verify that relay K1 is closed and K2 is open. Conditions can be checked by comparing signals at pins 1 and 4 using an Oscope.

11. Verify operation of output stage ICs U11 and U12.

    ICs U11 and U12 operate together as part of the output stage. These components interact, so it is somewhat difficult to establish which of these is faulty if the output stage is suspected as inoperative. The following documentation provides some characterization of this stage.

    U11 — this component can be checked using Diagnostic 6. Verify the given levels/frequencies for the indicated pins. Frequencies should be within 1 kHz.

Pin 4	51.5 kHz	(36.8 kHz)
Pin 5	22.1 kHz	
Pin 6	58.8 kHz	(22 kHz)
Pin 7	55.6 kHz	(37 kHz)
Pin 8	88.5 kHz	(59 kHz)
Pin 9	88.3 kHz	(59 kHz)
Pin 10	73.6 kHz	(29 kHz)
Pin 11	88.2 kHz	(59 kHz)
Pin 12	14.7 kHz	
Pin 13	14.7 kHz	
Pin 15	0.18 ±0.05V	



U12 — Input: the input to this IC is at virtual ground so is not easily monitored.

U12 — Output: Pin 6 closely matches the FM OUT signal. Correct operation can be verified using Diagnostics 3 through 8 to compare the expected FM OUT signal with this output pin.

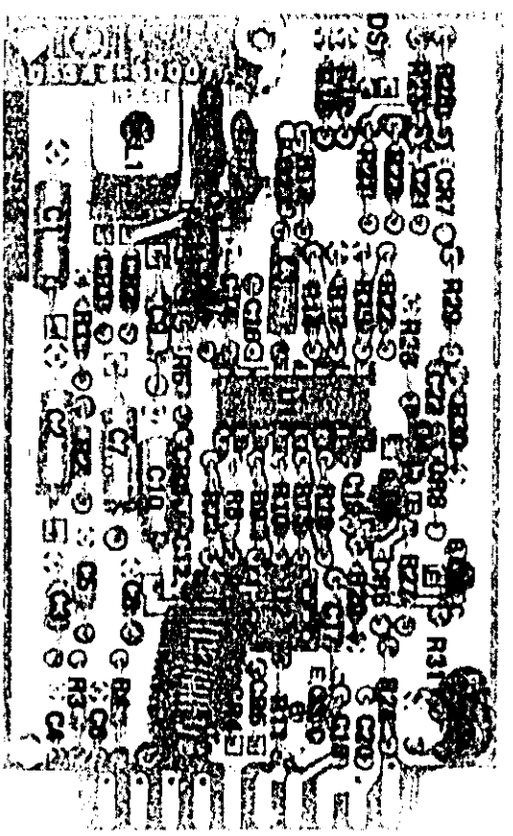
Table 8-13. A7 VCO Assembly Troubleshooting

Place the A7 Assembly on extender board 05342-60030, remove the A9 Assembly, and proceed.

1. Verify operation of transistors Q1-Q6.

   The following table provides voltage levels for transistors Q1-6. Power-up the counter and 5344A, then verify these levels:

Q	E	B	C
1	1.0V	-1.6V	12.0V
2	1.3V	1.6V	3.8V
3	0.00V	-0.1V	3.6V
4	3.0V	3.7V	12.8V
5	12.9V	12.8V	0.00V
6	2.9V	13.5V	14.5V



COMPONENT SIDE 1 — 10
SOLDER SIDE 1 — 10

P1

Table 8-13. A7 VCO Assembly Troubleshooting (Continued)

2. Verify operation of IC U1.

   The following table provides voltage levels for IC U1. Power-up the counter and 5344A, and with the A9 Assembly removed, verify these levels:

PIN		PIN	
1	5.0V	16	5.0V
2	3.7V	15	4.5V
3	3.7V	14	3.7V
4	0.00V	13	0.00V
5	3.7V	12	0.00V
6	3.7V	11	3.7V
7	0.00V	10	0.00V
8	0.00V	9	4.0V

3. Verify operation of IC U2 (Comparator).

   The following table provides voltage levels for IC U2. Power up the counter and 5344A with the A9 Assembly removed, then verify these levels:

PIN		PIN	
5	-4.7V	4	-15.0V
6	5.0V	3	5.0V
7	-13.0V	2	11.7V
8	14.5V	1	-13.0V

Table 8-14. A8 10 Volt Ramp/Timebase Assembly Troubleshooting

1. Verify A8 board operation by checking the test points listed below.

   Power up the counter and the 5344A for normal operation, and verify these levels/frequencies at the A8 test pins:

TP		IF FAULTY, SUSPECT
1	(RAMP OUT): 0.00 V	U3, U4
2	(100 KHZ): 100 kHz (±50 Hz) *	U5, Q1
3	(10 MHZ): 10 MHz	Counter 10 MHz Out
4	(LMRK): TTL LOW	U5
5	(MDC): TTL LOW	A5
6	(HBLK): TTL HIGH	U16
7	(MUX): TTL HIGH	U10
8	(PDC): TTL LOW	A5
9	(CTR CLR): TTL LOW	A5

   Enter Diagnostic 14 (refer to *Table 8-9*, Diagnostics) and verify these levels/frequencies at the A8 test pins:

TP		
1	(RAMP OUT): 52 Hz	NOTE: If faulty, then suspect component or assembly as given above.
2	(100 KHZ): 100 kHz (±50 Hz) *	
3	(10 MHZ): 10 MHz	
4	(LMRK): 52 Hz	
5	(MDC): TTL LOW	
6	(HBLK): 52 Hz	
7	(MUX): 51 kHz	
8	(PDC): TTL LOW	
9	(CTR CLR): 52 Hz	

   NOTE: * denotes that this signal is NOT at TTL compatible levels. Use the 5005 noise margin adjustment key to change to user selectable levels. Using the Vp+ and Vp- functions will aid to determine signal thresholds. If levels are adjusted properly, the probe light of the 5005 (in the kHz mode) will blink when the node is probed. Also, the signal can be viewed and measured on an Oscope.

   If signals check out as expected, it is fairly likely that this assembly is operating correctly.

   If any signal is not as expected, place the A8 assembly on extender board 05342-60033, and proceed troubleshooting.

2. Verify operation of Data Register U9.

   Power up the counter and the 5344A for normal operation. Verify the following for U9:

   - observe signal transitions at input pins (3, 4, 7, 8, 13, 14, 17, and 18). These transitions may be observed with an Oscope, or by noting the flashing light of a 5005 data probe (set to the kHz mode).
   - input pin 11 should be at TTL low.
   - all output pins should be at TTL high.

   Enter Diagnostic 14 and verify the following:

   - observe signal transitions at input pins (3, 4, 7, 8, 13, 14, 17, and 18). These transitions may be observed with an Oscope, or by noting the flashing light of a 5005 data probe (set to the kHz mode).
   - input pin 11 should be at TTL low.
   - output pins 2, 5, 12, and 19 should be at TTL high.
   - output pins 6, 9, 15, and 16 should be TTL low.

Table 8-14. A8 10 Volt Ramp/Timebase Assembly Troubleshooting (Continued)

3. Verify operation of Decade Divider U2.

   Power up the counter and the 5344A for normal operation. Verify operation of U2 by checking for frequency at the listed pins:

Pin	Frequency
12	10 MHz
13 and 4	1 MHz
9 and 15	2 MHz
7 and 1	200 kHz
3	100 kHz

4. Verify operation of Binary Counters U7 and U12.

   These counters are best checked using a combination of Diagnostic 14 and a CF/ΔF Manual Lock.

   The following table gives frequencies for pins of interest using Diagnostic 14 (note that these frequencies are approximate):

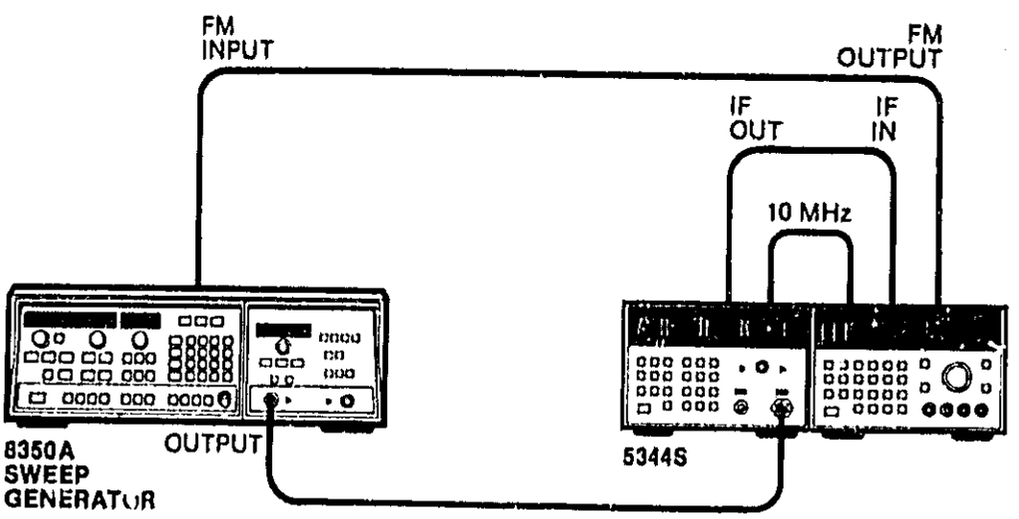
U7

Pin	Frequency
13	51 kHz
11	26 kHz
10	13 kHz
9	6.5 kHz
8	3.2 kHz
1	3.2 kHz
3	1.6 kHz
4	800 Hz
5	400 Hz
6	200 Hz

U12

Pin	Frequency
13	200 Hz
11	100 Hz
10	50 Hz

To fully check operation of counter U12, a CF/ΔF manual lock must be performed. Refer to *Figure 3-9* for detailed information. Use the following test setup.



Use a 0 dBm signal at 1 GHz for CF, 40 MHz for ΔF, a 100 ms Sweep Time, and manually lock the 5344S. Verify the remainder of the pins on U12 by starting at pin 10 and checking for division down through pin 3, as follow:

Pin	Frequency
10	74 Hz
9	37 Hz
8	19 Hz
1	19 Hz
3	10 Hz

Table 8-14. A8 10 Volt Ramp/Timebase Assembly Troubleshooting (Continued)

5. Verify operation of FF U11.

Power up the counter and the 5344A for normal operation. Check inputs and outputs for U11 as given below:

Inputs	Outputs
Pins 4, 5, 12, and 13 should have signal transitions present. Use an Oscope or 5005 data probe to verify. Pin 9 should be at TTL low.	Pin 2 LOW 7 LOW 10 LOW 15 LOW

To further check this component, perform a manual lock CF/ΔF sweep (if possible) with a 100 ms sweep time. Use a 1 GHz 0 dBm signal for CF, and 40 MHz for ΔF. Check inputs and outputs for U11 as given below:

Inputs	Outputs
Pins 4, 5, 12, and 13 should have signal transitions present. Use an Oscope or 5005 data probe to verify. Pin 9 should be at TTL low.	Pin 2 HIGH 7 HIGH 10 LOW 15 LOW

6. Verify operation of Binary Counters U1 and U8

To check these ICs for correct operation, enter Diagnostic 14 and check for division by two. The following table provides approximate frequencies for the pins of interest:

	Pin	Frequency
U1	13	52 kHz
	11	26 kHz
	10	13 kHz
	9	6.5 kHz
	8	3.2 kHz
	1	3.2 kHz
	3	1.6 kHz
	4	830 Hz
	5	415 Hz
	6	208 Hz
U8	1	208 Hz
	3	104 Hz
	4	52 Hz
	13	52 kHz
	10	104 Hz
	9	52 Hz

7. Verify operation of FFs U5 and U16

To check these ICs for correct operation, enter Diagnostic 14 and check for approximate frequencies as given below.

	Inputs	Outputs
U5	Pin 2 52 Hz 3 500 Hz	Pin 6 52 Hz
	11 10 MHz 12 100 kHz	9 100 kHz
U16	Pin 2 52 Hz 3 620 Hz	5 52 Hz
	11 100 kHz 12 52 Hz	8 52 Hz

Table 8-14. A8 10 Volt Ramp/Timebase Assembly Troubleshooting (Continued)

8. Verify operation of Multiplexer U10

Multiplexer U10 can be checked using Diagnostic 13 and a manual lock (if possible).

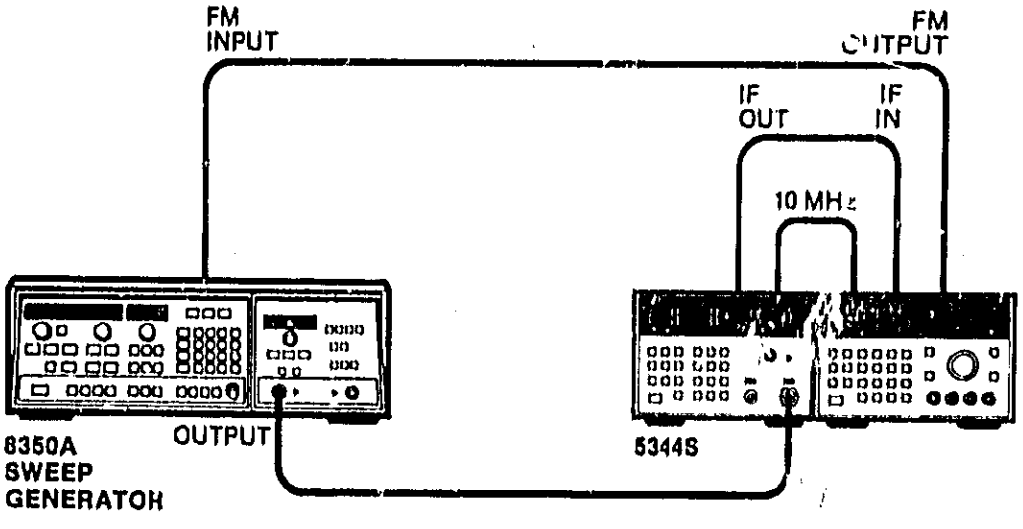
Diagnostic 13

Enter Diagnostic 13. Verify that all binary weighted inputs (pins 11, 13, 14, and 15) are at TTL low levels. This weighting selects the 0 data line, so the output signal at pin 10 should match that at input pin 8 (54 kHz).

Manual Lock

Place the counter in a manual CF/ΔF lock with a 0 dBm signal at 1 GHz for CF, 40 MHz for ΔF, and a Sweep Time of 100 ms. Connect the 5344S in the test setup shown below.

Verify that pins 11 and 13 are at TTL low levels, while pins 14 and 15 are at TTL high levels. This weighting selects data line 3, so that the output signal at pin 10 should match that at input 5 (9.3 kHz).



9. Verify operation of Binary Counters U6 and U14

Diagnostics 13 can be used to check these ICs. Verify that inputs and outputs are as given in the table below:

Diagnostic 13

U6 Inputs	U14 Inputs
Pin 1 54 Hz 2 10 MHz 3 TTL LOW 4 TTL LOW 5 TTL HIGH 6 TTL HIGH 7 54 Hz 9 54 kHz	Pin 1 54 Hz 2 10 MHz 3 TTL HIGH 4 TTL LOW 5 TTL LOW 6 TTL HIGH 7 376 kHz 9 54 kHz
Output Pin 15 376 kHz	**Output** Pin 15 54 kHz

Table 8-14. A8 10 Volt Ramp/Timebase Assembly Troubleshooting (Continued)

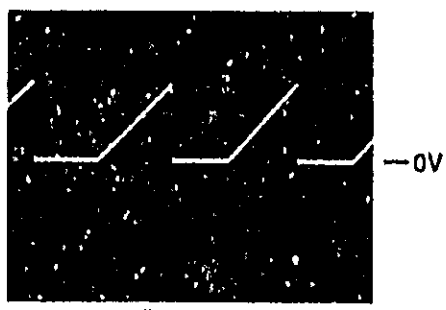
10. Verify operation of DAC and Op Amp Circuitry

The recommended procedure to check out these components consists of checking for a correct output signal for given known inputs.

Check DAC U4 inputs in Diagnostic 13 and verify that the Op Amp output is as shown in the Oscope photo.

Diagnostic 13

Pin	Frequency
4	54 Hz
5	108 Hz
6	216 Hz
7	432 Hz
8	864 Hz
9	1.6 kHz
10	3.32 kHz
11	6.7 kHz
12	13.4 kHz
13	26.8 kHz



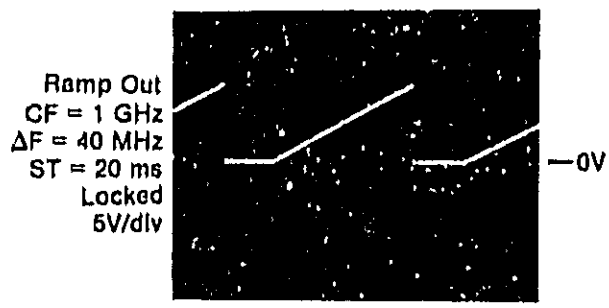
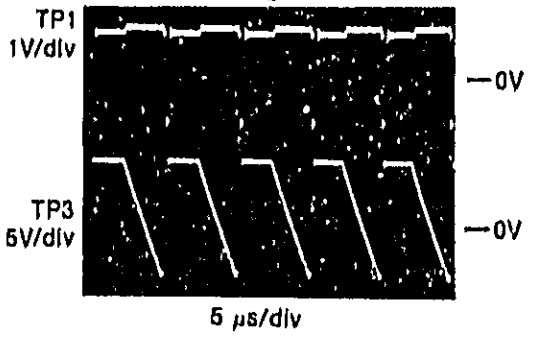


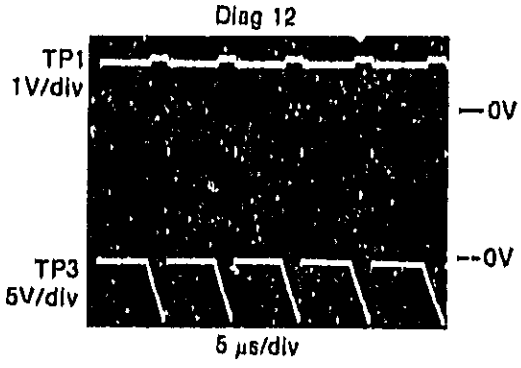
Table 8-15. A9 Analog Assembly Troubleshooting

1. Use the following scope photos taken at Test Points 1, 2, and 3 during the indicated diagnostic to verify operation of this assembly.

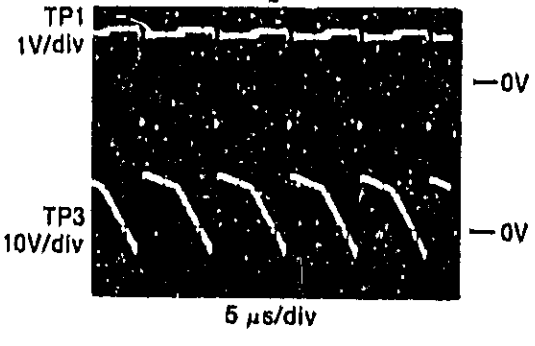
Diag 11



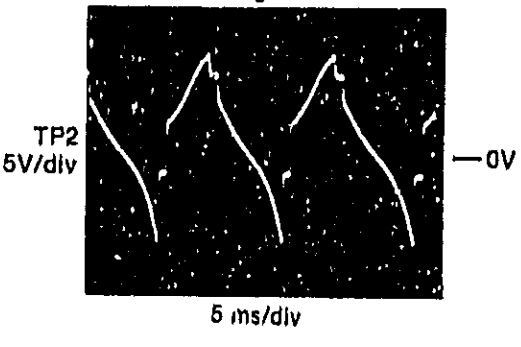
Diag 12



Diag 13



Diag 13



Diagnostic	Test Point 1	Test Point 2	Test Point 3
11	Photo	10.8 V	Photo
12	Photo	<1 V	Photo
13	Photo	Photo	Photo

2. If waveforms and levels do not appear as expected, then place the A9 Assembly on extender board 05344-600014 and proceed.

Troubleshoot to the problem area as indicated by the results of the Test Point waveforms. There are three key blocks on this board and the troubleshooting is broken up into these main areas:

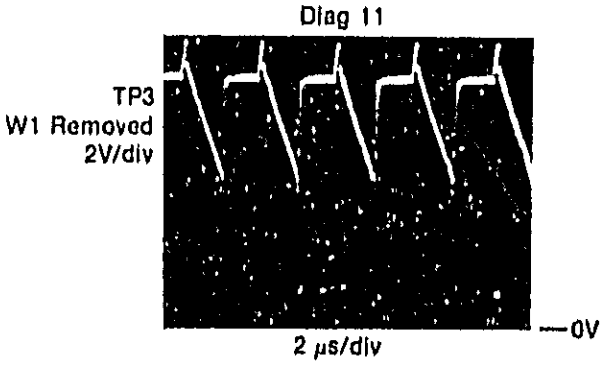
a. Phase Comparator Circuitry (TP1)
b. Sample and Hold Circuitry (TP2)
c. Integrator Circuitry (TP3).

Table 8-15. A9 Analog Assembly Troubleshooting (Continued)

If Test Point 1 looks incorrect, it is a simple matter to troubleshoot the phase comparator circuitry. However, if TP 1 looks good, but both TP 2 and 3 look bad (as may be the case because of feedback), the task becomes somewhat more difficult. To isolate the problem area, open jumper W1 and verify the following during Diagnostic 11:

Test Point 2: -13.6 V ±1 V

Test Point 3:



The problem should now be isolated to a particular circuit block. Proceed troubleshooting at that circuit block.

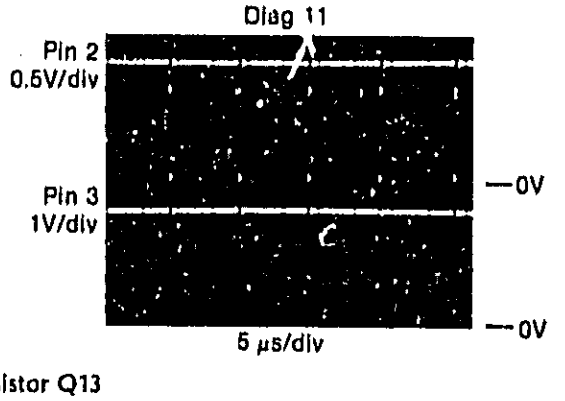
3. Phase Comparator

If TP 1 waveforms do not appear as shown, then verify the operation of individual components as indicated.

a. Phase Comparator U3

Enter Diagnostic 11 and verify that input pins 5, 6, 11, and 13 have a 100 kHz signal present.

Output pin 15 should be at TTL HIGH, and pin 2 should have the following waveform (pin 3 should be its complement):



b. Transistor Q13

The following waveform shows the collector of Q13 during Diagnostic 11

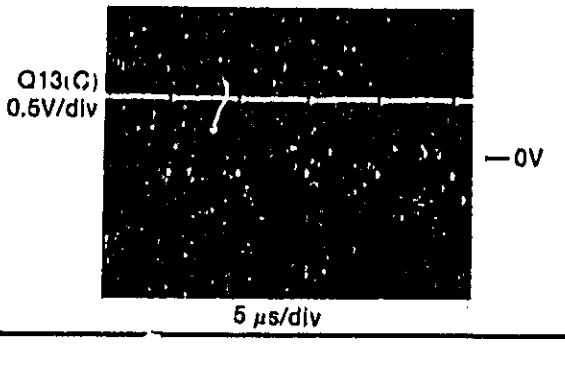


Table 8-15. A9 Analog Assembly Troubleshooting (Continued)

Another waveform which may be of help is that of TP 1 during this same diagnostic. This waveform will help to isolate transistors Q13-16 if any are faulty.

4. Sample and Hold Circuitry

If TP2 looks incorrect, but TP3 has checked out OK, then verify operation of the block as indicated.

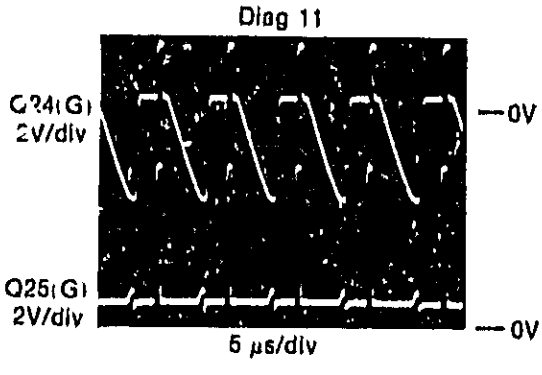
a. Open the Integrator feedback input by unsoldering one end of A9R58. Open the Integrator output by unsoldering one end of jumper W1 (this may have been done to isolate the trouble area).

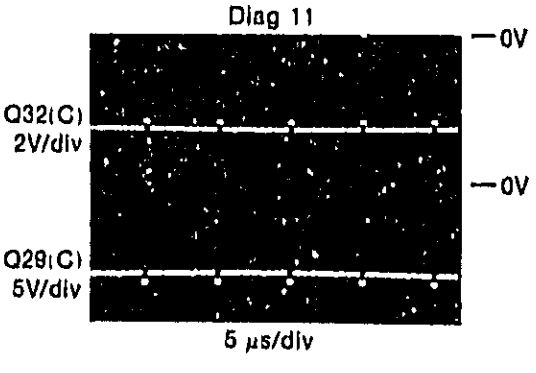
b. Apply +5 Volts to the Sample and Hold circuit at A9Q24 source. The voltage at TP2 should be +6 (± 0.5) volts. If not, then suspect U6 or U7 as faulty. Proceed to step c.

c. If this voltage is not correct, then apply +5 volts at A9U7 pin 3. The output voltage at A9U7 pin 6 should be +5 volts, and that at A9U6 pin 6 should be +5.5 volts. Replace the suspected faulty component if these levels are not present.

d. Resolder the loose end of A9R58 and W1 to close the Integrator feedback input and the output loop.

e. Finally, check for the presence of the Sample and Hold Control signal from the base of A9Q29 to the gates of A9Q24 and Q25. The photos shown g[illegible] waveforms for the indicated nodes during Diagnostic 11.





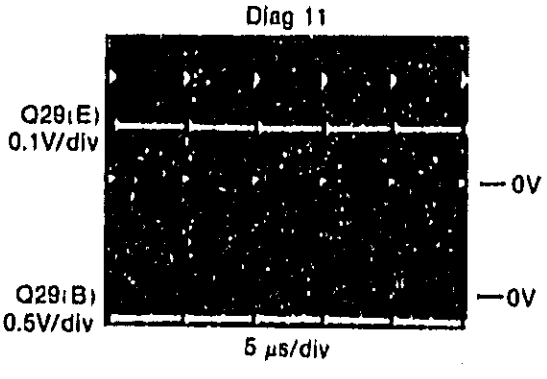


Table 8-15. A9 Analog Assembly Troubleshooting (Continued)

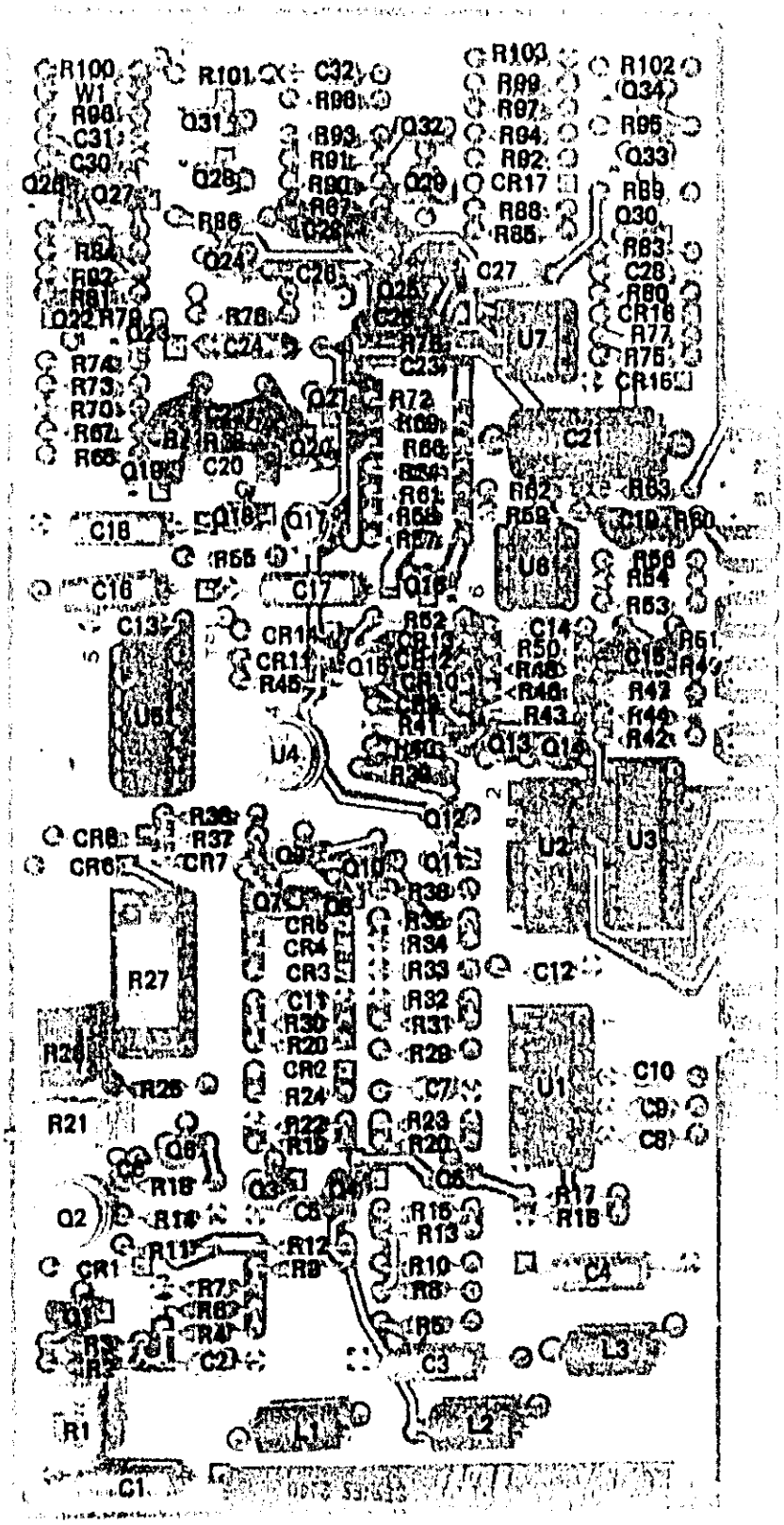


Table 8-15. A9 Analog Assembly Troubleshooting (Continued)

5. Integrator Circuitry

If TP3 looks incorrect, but TP1 checks out OK, then check out the operation of this block a indicated.

a. Open the Integrator input by unsoldering one end of A9CR9, CR10, and R58. Open the Integrator output by unsoldering one end of W1 (this may have been done to isolate the trouble area).

b. Connect a jumper in the W2 position. The plate-through holes for this connection are located adjacent to resistor R78. This places a 1 kOhm resistor across integrating capacitor C24, and the Integrator should now function as an op amp. The voltage at A9TP3 should be 0 Volts (± 0.1 Volts).

If this voltage is correct, continue on to step c. If this voltage is not correct, troubleshoot the Integrator by comparing voltage levels as given in the following table:

Integrator DC Voltage Levels

Transistor	E	B	C
Q18	13.3	12.7	-0.1
19	-13.5	-12.8	-0.1
20	-0.6	0.2	13.3
21	-0.6	0.2	12.7
22	0.6	-0.1	-15
23	-0.9	-0.1	15
26	0.0	0.6	15
27	0.0	-0.9	-15
Q17:	G1 -0.1 G2 0.0	D1 15 D2 15	S1 0.2 S2 0.2

c. Resolder the loose end of A9CR9, CR10, R58, and remove jumper W2 to close the Integrator feedback input and the output loop.

d. Check operation of DACs U1 and U2

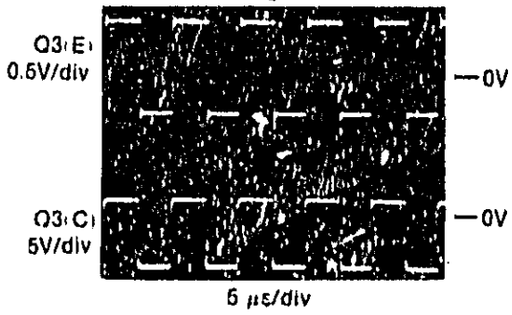
Enter Diagnostic 11 and verify that a 100 (± 1) kHz signal is present at the inputs and outputs of U1 and U2 (Bias and API lines). The Latch Clock should be a 1.4 ± 0.1 MHz signal.

e. The Summing Amplifier and Current Sources can be verified by comparison of levels and waveforms given. Enter Diagnostic 11 and check for the following:

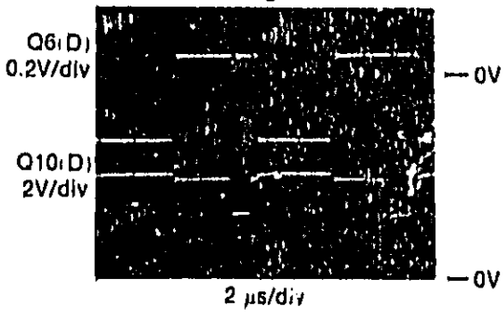
Table 8-15. A9 Analog Assembly Troubleshooting (Continued)

Transistors:

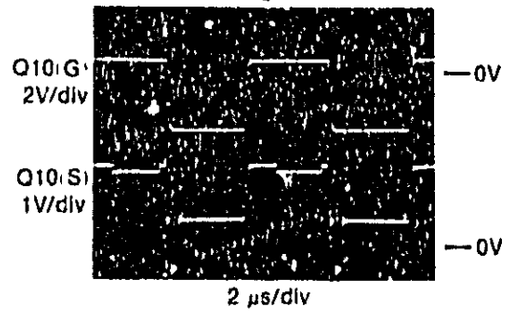
Diag 11



Diag 11



Diag 11

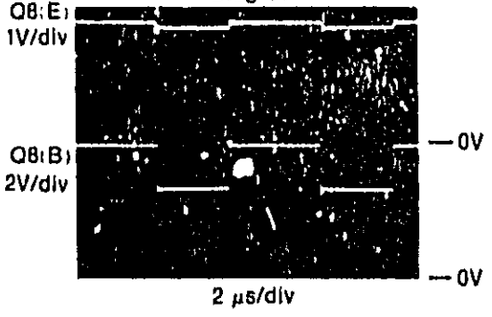


Q6	G	7.4 (± 0.2) V	Q9	G	-6.2 (± 0.2) V	Q12	G	11 (± 1)V
	S	5.0 (± 0.2) V		S	-5.8 (± 0.2) V		D	8.7 (± 0.2) V
							S	5.0 (± 0.2) V

API Lines

API lines 1, 2, and 3 behave identically during this diagnostic, so the given waveform can be used as a model for the other two lines.

Diag 11



Transistor Array U5

Verify the following dc voltage levels at the indicated pins.

Pin 1	-5.8	14	0.0
2	-8.1	13	-15
3	-8.8	12	-15
4	-8.1	11	+8.2
5	-5.8	10	+8.8
6	-8.1	9	-8.1
7	-8.8	8	+5.6

Table 8-16. A10 Digital Assembly Troubleshooting

1. Begin checking the operation of this board by verifying the signals as given for the test points in the following table. Power up the counter and the 5344A for normal operation and check for these signals:

TP	Frequency or Voltage	If Faulty, Suspect
1 (VCO/2)	20.5 MHz	U6
2 (CHIP)	5.6 MHz	U7
3 (SLF)	TTL HIGH	U8, Q2
4 (PRELOAD)	85.6 kHz or 57 kHz	U20
5 (START CYCLE)	85.6 kHz or 57 kHz	U9
6 (PULSE REMOVE)	57 kHz	U8
7	85.6 kHz or 57 kHz	U12
8 (VCO/10)	5.6 MHz	U20

Enter Diagnostic 14 and verify these levels and frequencies:

TP	Frequency or Voltage	If Faulty, Suspect
1 (VCO/2)	18.4 MHz	U6
2 (CHIP)	3.7 MHz	U7
3 (SLF)	440 Hz ± 100 Hz	U8, Q2
4 (PRELOAD)	100 kHz	U20
5 (START CYCLE)	100 kHz	U9
6 (PULSE REMOVE)	32.3 kHz	U8
7	100 kHz	U12
8 (VCO/10)	3.6 MHz	U20

2. If signals observed are not correct, then turn off power to the 5344A, remove the A9 Assembly, and place the A10 Assembly on two 05342-60034 extender boards. Removing the A9 Assembly disconnects the VCO control voltage from the A7 board.
3. Power up the 5344A and measure the frequency of the VCO signal at jumper A10W1. This signal should be 40 (± 5) MHz.
4. Connect Test Point A10TP6 and U13 Pin 1 to ground. These connections disable the divide-by-N Shift Register and the Pulse Remove circuits.
5. Measure the frequency at each of the following nodes, keeping in mind the relationship of the measured signal to the VCO. Suspect ICs may be verified for their operation (transitions at input/output pins) during Diagnostic 14 as given in step 7.

   A10TP1 should be VCO/2. If not, suspect A10U1 and U6.

   A10TP8 should be VCO/10. If not, suspect A10U19 and U20.

   A10U11 Pin 4 should be VCO/100. If not, check A10U16.

   A10 TP7 should be VCO/1000. If not, check A10U11, U12, U15, and U16.

   A10 TP4 should be VCO/1000. If not, check A10U15 and U21.

   A10 TP2 should be VCO/10. If not, check A10U7.

   A10 TP5 should be VCO/1000. If not, check A10U9.

   A10 Q1 Collector should be VCO/1000 (a very narrow pulse). If not, check A10U3, U4, Q1, and C3.

   A10U8 Pins 2, 3, 4, 5, 6, 10, and 11 should be VCO/1000. If not, suspect U8.

6. Power down the 5344A, disconnect the ground connection from A10TP6 and U13 Pin 1, and replace the A9 Assembly. Next, power up the unit, and enter Diagnostic 11 to check for the presence of pulses at the input, output, and clock pins of A10U13 and U17. If pulses are present at the input and clock pins, and Pin 1 is at TTL HIGH, but no pulses appear at the output pins, then the particular IC is probably defective. If pulses are present at the outputs, then ICs in the divide-by-5 counter circuit may be defective. In this case, check A10U18, U21, and U22.

Table 8-16. A10 Digital Assembly Troubleshooting (Continued)

7. The following table provides frequencies at nodes of interest during Diagnostic 14. Enter Diagnostic 14 and verify the given frequencies at the indicated pins:

IC	Pin	Frequency
U1	3	71 kHz
	11	71 kHz
U2	1	71 kHz
	11	71 kHz
	13	3.7 MHz
U3	9	100 kHz
	12	100 kHz
U4	2	67 kHz
	3	100 kHz
	5	12.9 kHz
	9	100 kHz
	12	100 kHz
U6	2	71 kHz
	12	71 kHz
U7	3	3.7 MHz
	12	7.3 MHz
U8	2	100 kHz
	3	100 kHz
	4	100 kHz
	5	100 kHz
	6	100 kHz
	7	3.7 MHz
	10	100 kHz
	11	100 kHz
	12	32.3 kHz
	13	111 kHz
	14	145 kHz
	15	116 kHz
	16	130 kHz
	17	262 kHz
	18	440 Hz ± 100 Hz
	20	25.2 kHz (16.6 kHz)
	21	24.9 kHz (15.4 kHz)
	22	24.4 kHz (14.5 kHz)
	23	25.4 kHz (16.7 kHz)
	24	620 Hz
	25	104 Hz
	26	4.1 kHz
	28	100 kHz
U9	2	7.3 MHz
	13	3.7 MHz
U10	2	620 Hz
	3	18.4 MHz
	5	620 Hz
U11	8	25 MHz
U12	1	66 kHz
	9	31 kHz
	10	75.4 kHz
	14	405 kHz
	15	67 kHz

Table 8-16. A10 Digital Assembly Troubleshooting (Continued)

IC	Pin	Frequency
U13	2	67 kHz
	3	130 kHz
	4	116 kHz
	5	65.8 kHz
	6	145 kHz
	7	75 kHz
	9	262 kHz
	10	75 kHz
	11	75 kHz
	12	65.8 kHz
	13	65.8 kHz
	14	67 MHz
	15	67 MHz
U16	1	65.8 kHz
	9	31 kHz
	10	75.4 kHz
	15	67 kHz
U17	3	111 kHz
	5	67 kHz
	6	31 kHz
	7	31 kHz
	10	65.8 kHz
	13	31 kHz
	15	75.4 kHz
U19	4	33.6 kHz
	9	3.7 MHz
	10	33.6 kHz
	11	7.4 MHz
	14	66.4 kHz
	15	66.4 kHz
U20	3	3.7 MHz
	4	32.7 kHz
	11	3.7 MHz
	12	100 kHz
	14	100 kHz
	15	67 kHz

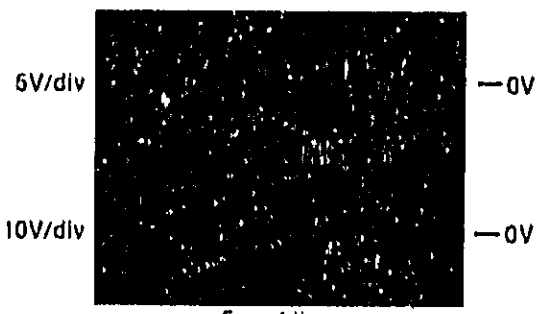
Table 8-17. A12 Power Supply Assembly Troubleshooting

Remove the bottom cover as instructed in paragraph 8-24. Remove all connections from the counter to the 5344A so that it is completely isolated. Apply power to the 5344A.

The following are input waveforms to diode bridges CR1, CR5 and CR6, and to diode pair CR1. These waveforms were taken on the solder side of the motherboard at the nodes indicated by the transformer wire color.

+5 Volt Supply

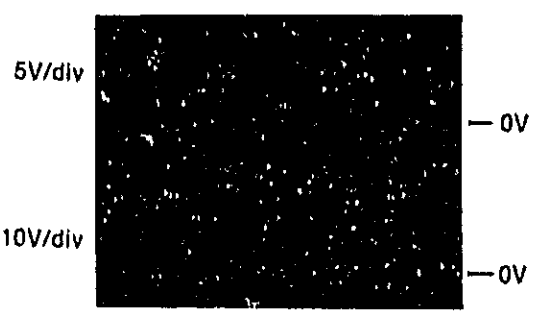
Waveforms taken at the YEL terminals:



The approximate dc level into Fuse F1 is +15V with a small amount of ripple on this waveform.

+15 Volt Supply

Waveform taken at the RED terminals:



The approximate dc level into Regulator U4 is +20 Volts.

-15 Volt Supply

Waveforms at the GRN terminals resemble those at the RED terminals (photo given above). The difference is that the amplitude of the waveform is 0 to -20 Volts peak-to-peak.

The approximate dc level into Regulator U3 is -20 Volts.

-5.2 Volt Supply

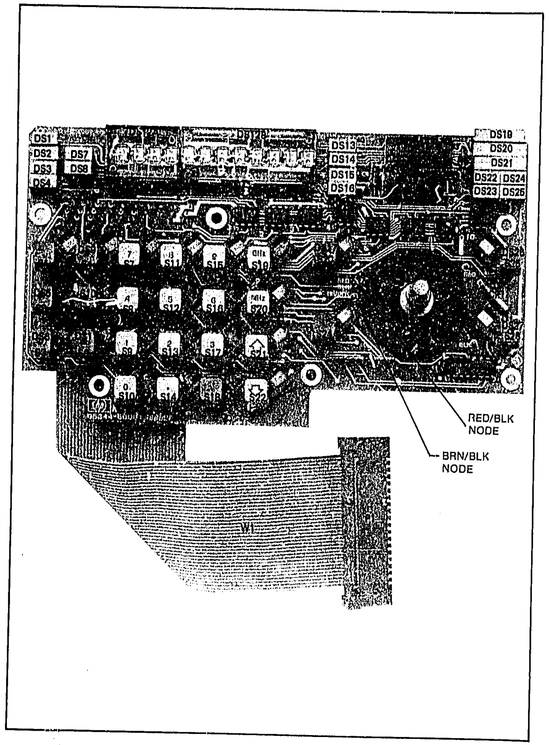
Waveforms at the BLU terminals resemble those at the RED terminals (photo given above). The difference is that the amplitude of the waveform is 0 to -10 Volts peak-to-peak.

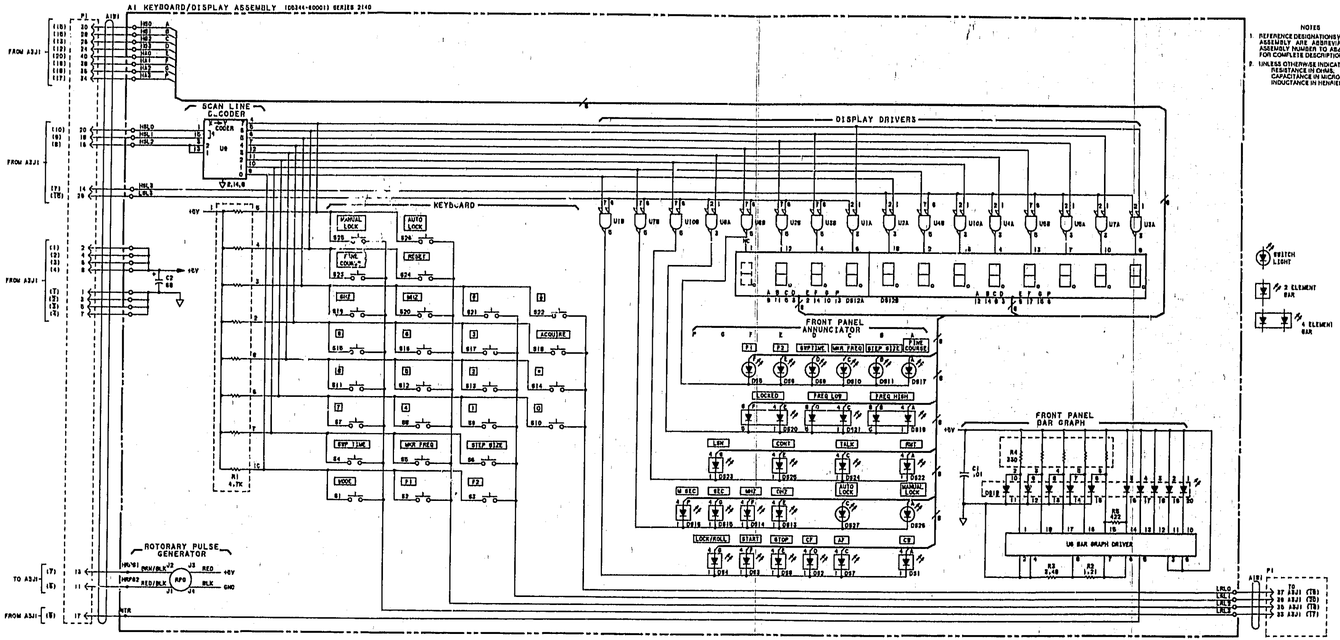
The approximate dc level into Regulator U2 is -10 Volts.

The following table provides power up conditions of Regulator U1. Check for the given level at the indicated pins.

U1

Pin	Voltage
1	3.8 V
2	13 V
3	13.7 V
4	0.00 V
5	1.7 V
6	1.7 V
7	4.4 V
8	5.0 V





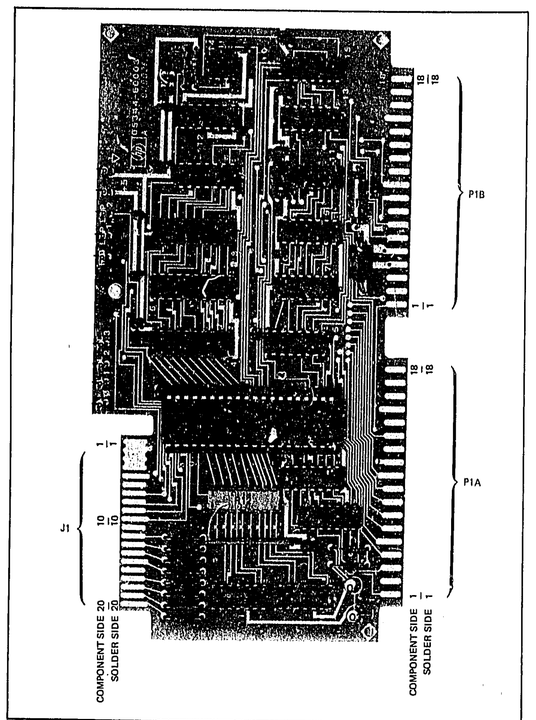
A1 Reference Designations

C1, C2
DS1-27
J1-4
R1-5
U1-26
W1
XDS12

A1 TABLE OF ACTIVE ELEMENTS

Reference Designations	HP Part Number	Mfr. Part Number
DS1-4, DS7, DS8, DS12, DS15, DS16, DS22-26	1990-0696	1LM1-2000
DS5, DS6, DS9, DS11 DS17	1990-0670	1900-0670
DS13	05344-20202	05344-202U2
DS14, DS18-21	1990-0569	1LM1-2350
U1-6, U7, U8, U10	1820-1016	SN74LS05P
U9	1826-0655	LM3914N
U11	1820-1427	SN74LS156N

Figure 8-25. A1 Keyboard/Display Assembly



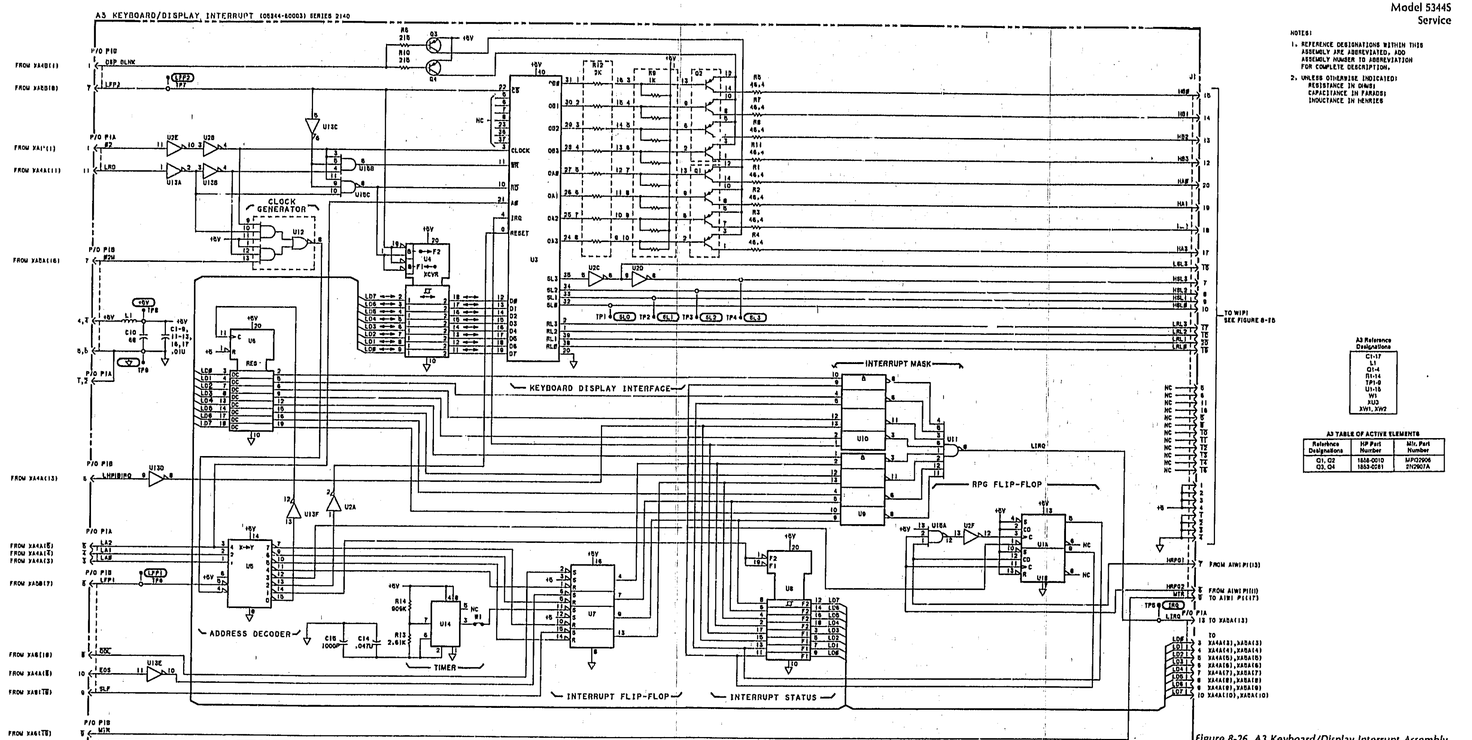
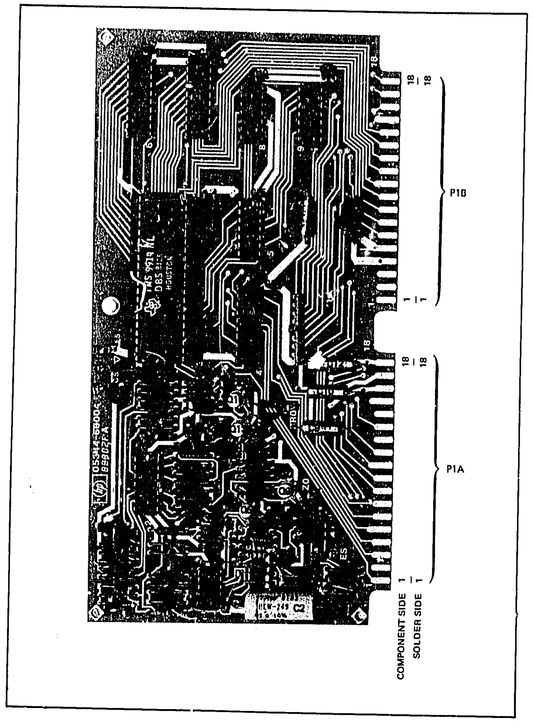
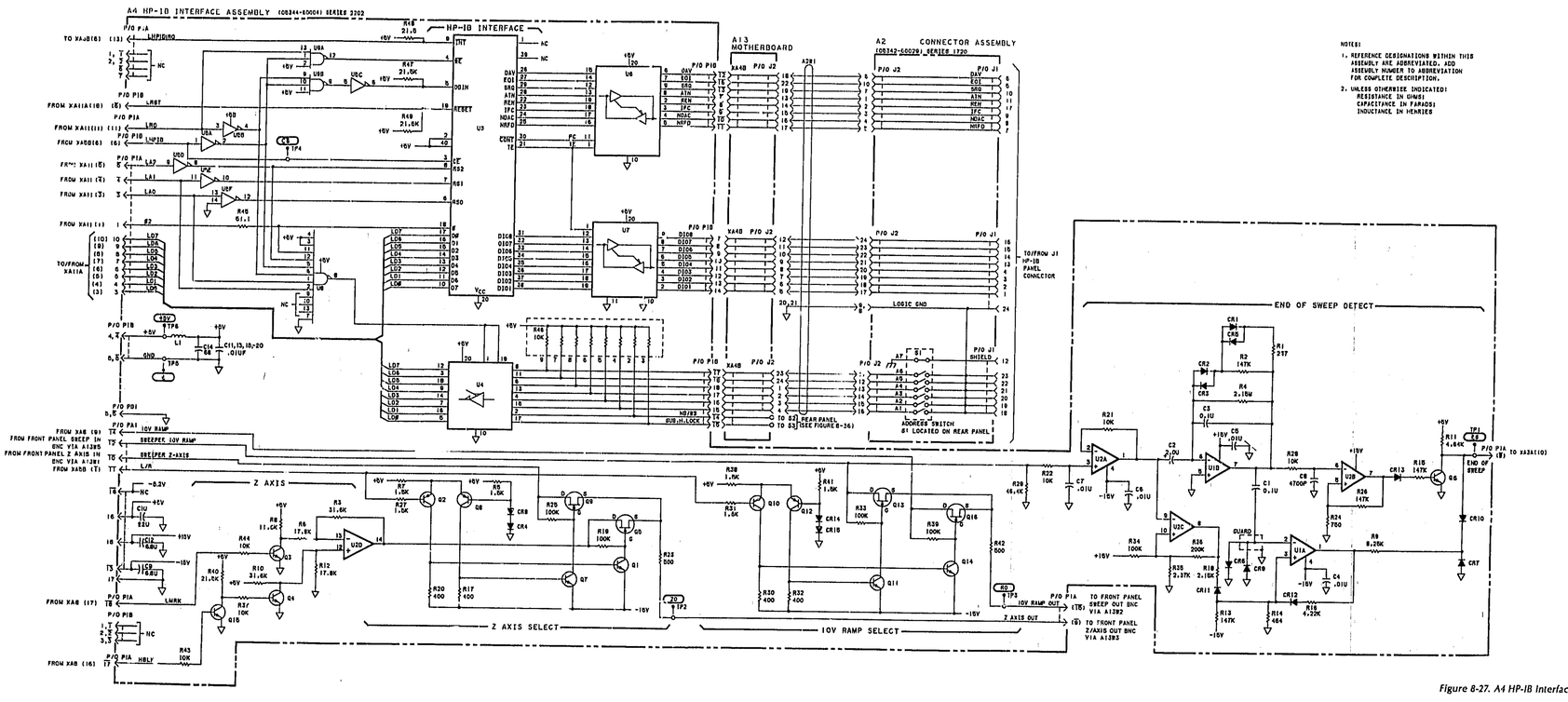


Figure 8-26. A3 Keyboard/Display Interrupt Assembly





NOTES:

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS
   CAPACITANCE IN FARADS
   INDUCTANCE IN HENRIES

A2 Reference Designations

J1-J2
MP1-3
S1
W1

A2 TABLE OF ACTIVE ELEMENTS

Reference Designations	HP Part Number	Mfr. Part Number
None		

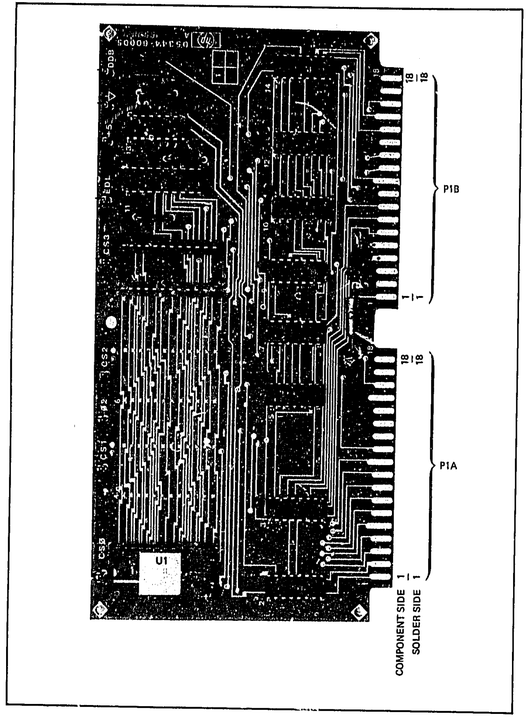
A4 TABLE OF ACTIVE ELEMENTS

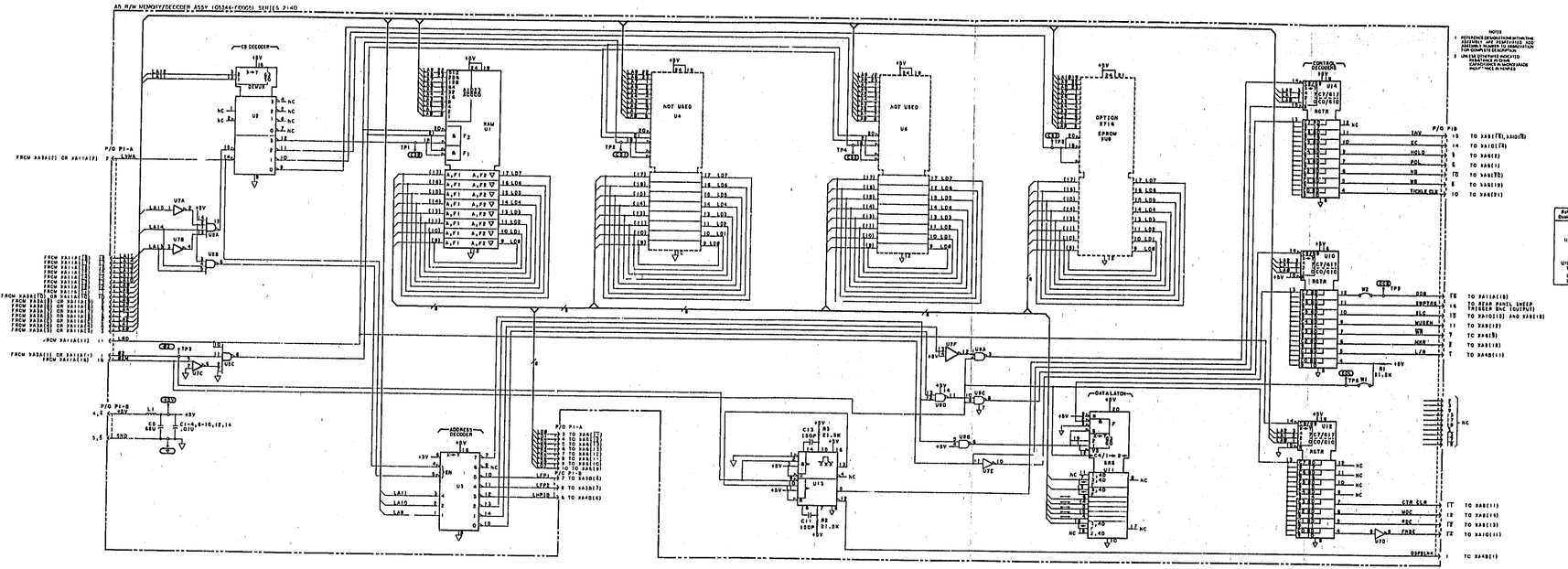
Reference Designations	HP Part Number	Mfr. Part Number
CR1-3, CR5	1901-0018	IC1-0018
CR4, CR7, CR8, CR10, CR12-15	1901-0050	1 J1-0030
CR6, CR9	1901-0044	1901-0044
CR11, CR12	1901-0618	1901-0618
Q1, Q3, Q4, Q6, Q7, Q11, Q14, Q15	1854-0215	2N3904
Q2, Q8, Q10, Q12	1853-0036	1853-0026
Q5, Q9, Q13, Q16	1853-0420	2N4391
U1	1826-0521	TL072CP
U2	1826-0315	LM348N
U3	1826-2448	1826-2448
U4	1820-2624	SN74LS244N
U5	1820-1199	SN74LS04N
U6	1820-2483	SN75161N
U7	1820-2485	SN75160N
U8	1820-1207	SN74LS30N
U9	1820-1202	SN74LS15N

A4 Reference Designations

C1-20
CR1-15
L1
Q1-16
R1-48
TP1-6
U1-9

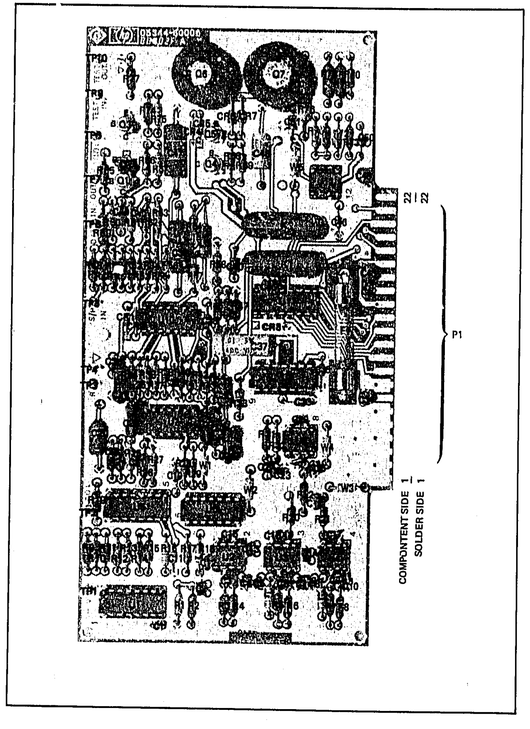
Figure 8-27. A4 HP-IB Interface/A2 HP-IB Connector Assembly

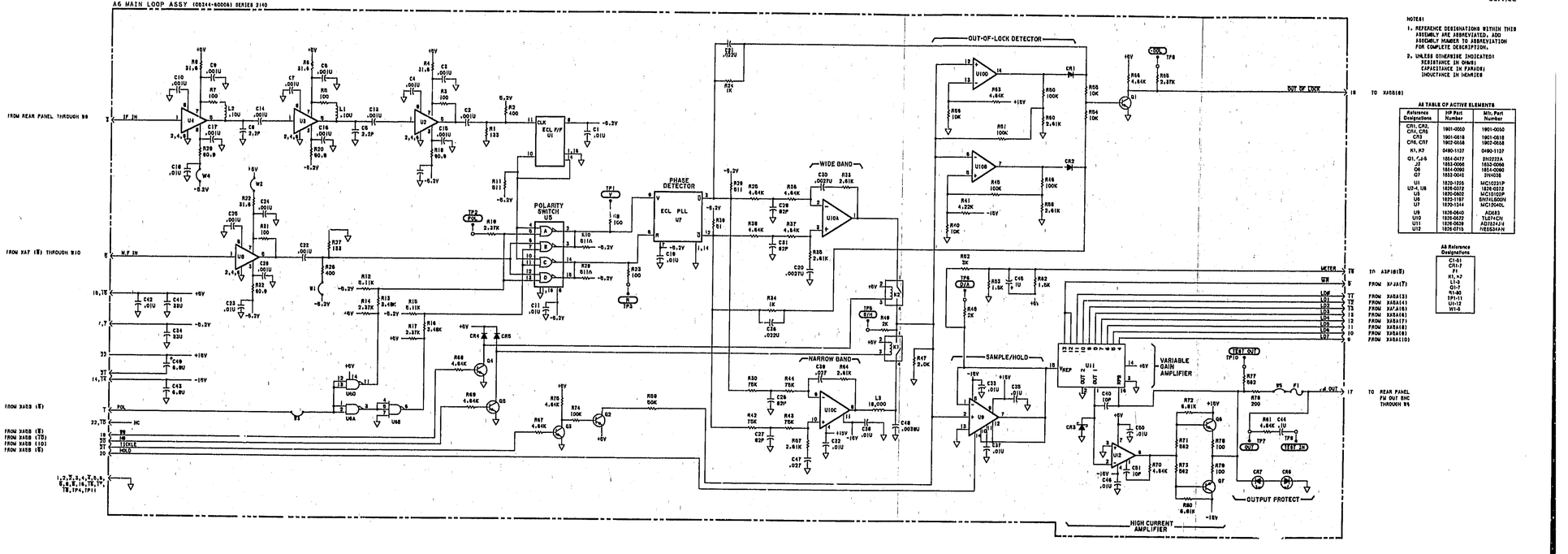




Reference Designators	HP Part Number	MFR. Part Number
U1	1818-1313	MX4116A2P-4
U2	1820-1216	SN74LS153N
U3, U6	1820-1215	SN74LS139N
U4	Not Used	
U5	1820-1902	SN74LS10N
U7	1820-1198	SN74LS04N
U8, U9	1820-1197	SN74LS00N
U10	1820-1278	SN74LS125N
U11	1820-1867	SN74LS299N
U12	1820-1273	SN74LS137N

Figure 8-28. A5 R/W Memory/Decoder Assembly





NOTES:
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN FARADS; INDUCTANCE IN HENRIES

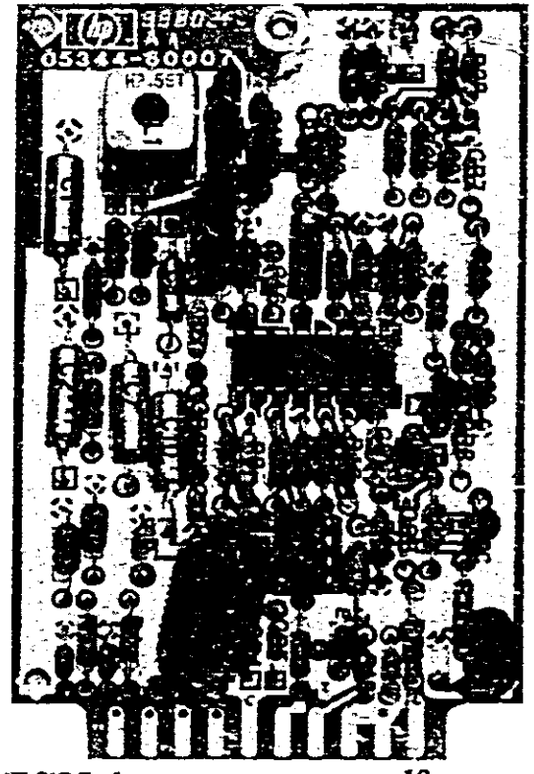
A6 TABLE OF ACTIVE ELEMENTS

Reference Designations	HP Part Number	Mfr. Part Number
CR1, CR2, CR4, CR5	1901-0050	1901-0050
CR3	1901-0518	1901-0518
CR6, CR7	1902-0068	1902-0068
K1, K2	0490-1137	0490-1137
Q1, Q4-6	1854-0477	2N2222A
J2	1853-0066	1853-0066
Q3	1854-0060	1854-0060
Q7	1853-0045	2N4036
U1	1820-1225	MC10231P
U2-4, U8	1826-0272	1826-0272
U5	1820-0803	MC10102P
U6	1820-1197	SN74LS00N
U7	1820-1344	MC12040L
U9	1826-0640	AD843
U10	1826-0632	TL074CN
U11	1826-0638	AD7624J-N
U12	1826-0715	NE5542-N

A6 Reference Designations

C1-61
CR1-7
F1
K1, K2
L1-3
Q1-7
R1-70
TP1-11
U1-12
W1-8

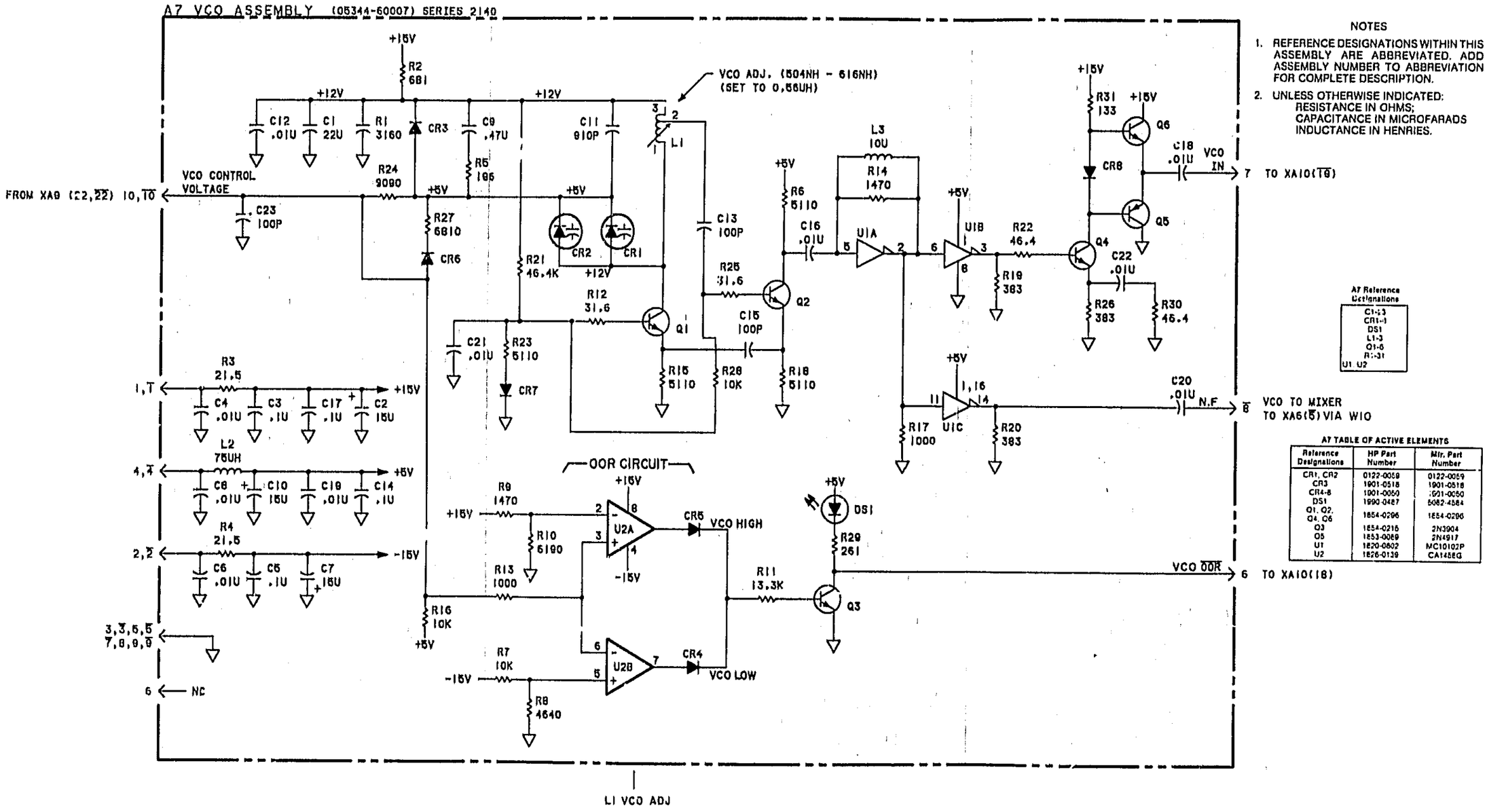
Figure 8-29. A6 Main Loop Assembly



COMPONENT SIDE 1 10

SOLDER SIDE 1 10

P1



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN MICROFARADS
   INDUCTANCE IN HENRIES.

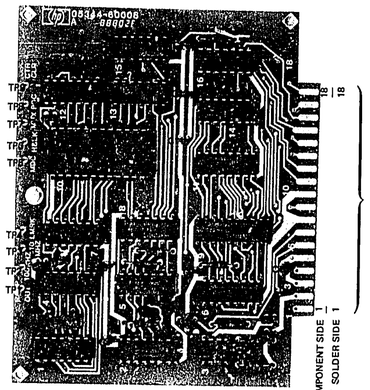
A7 Reference Designations

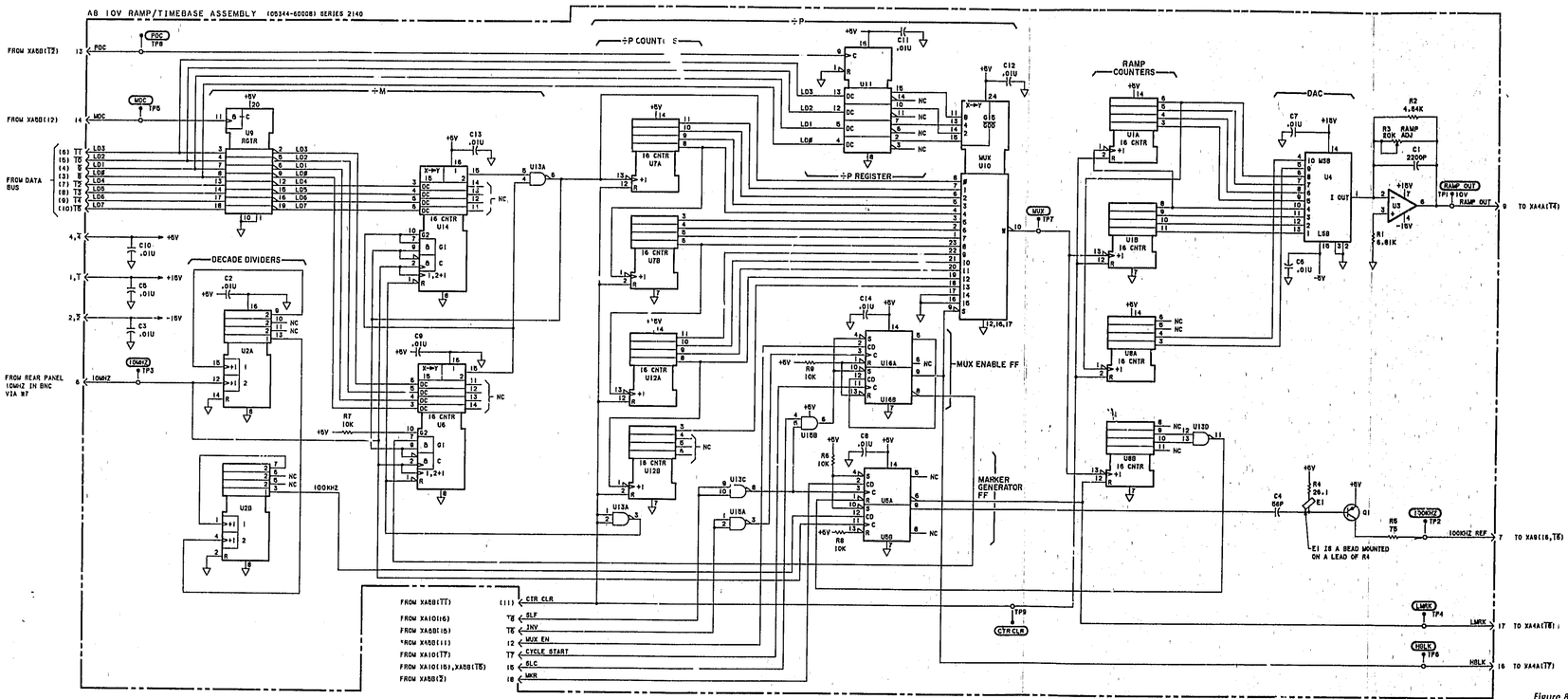
C1-43
CR1-8
DS1
L1-3
Q1-6
R1-31
U1, U2

A7 TABLE OF ACTIVE ELEMENTS

Reference Designations	HP Part Number	Mfr. Part Number
CR1, CR2	0122-0059	0122-0059
CR3	1901-0518	1901-0518
CR4-8	1901-0050	1901-0050
DS1	1990-0487	5082-4584
Q1, Q2, Q4, Q6	1854-0296	1854-0296
Q3	1854-0215	2N3904
Q5	1853-0089	2N4917
U1	1820-0602	MC10102P
U2	1826-0139	CA1458G

Figure 8-30. A7 VCO Assembly





NOTES:

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS
   CAPACITANCE IN FARADS
   INDUCTANCE IN HENRIES

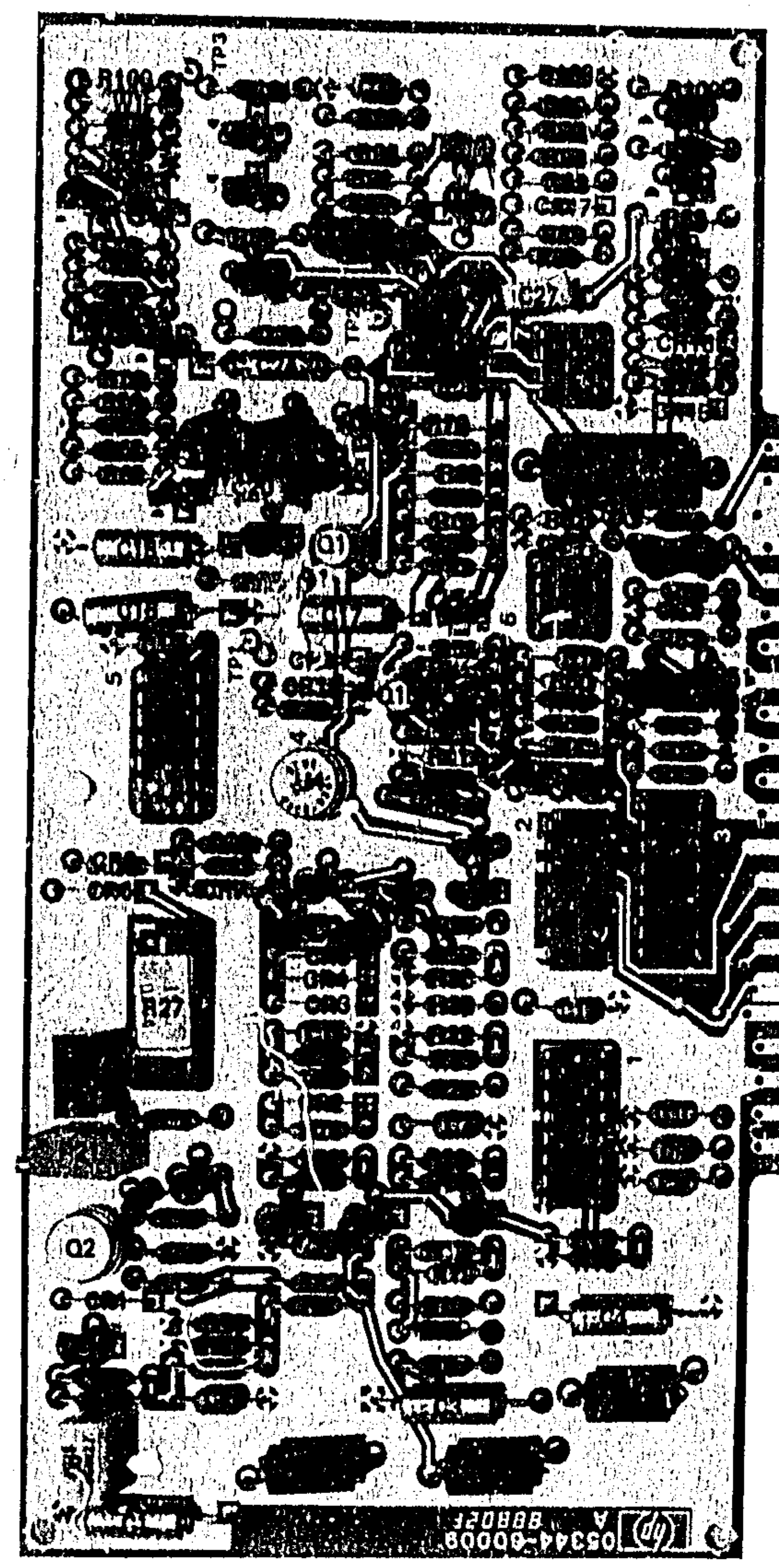
A8 Reference Designations

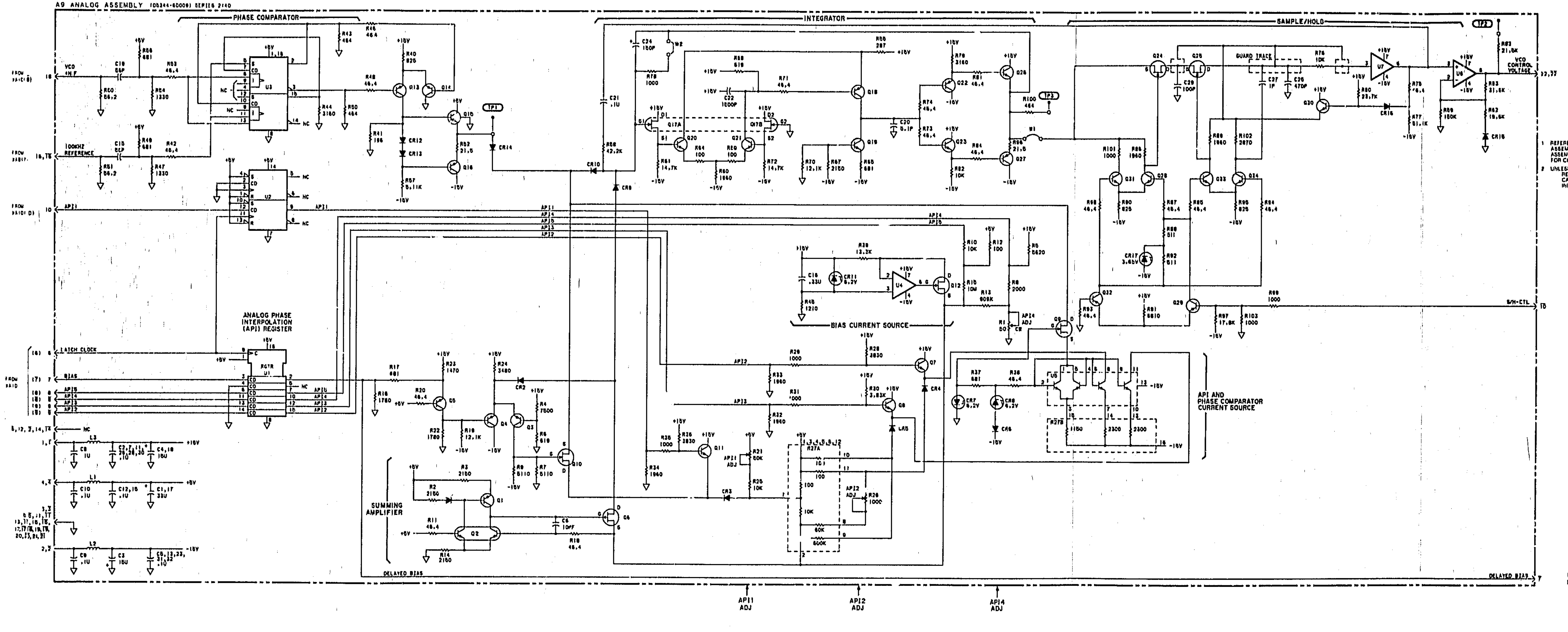
C1-14
L1
Q1
R1-8
TP1-8
U1-16
XU1U

A8 TABLE OF ACTIVE ELEMENTS

Reference Designations	HP Part Number	Mfr. Part Number
Q1	1853-0048	MPS918
U1, U7, U8, U12	1820-2066	SN74LS393N
U2	1820-1991	SN74LS390N
U3	1820-0493	LM307N
U4	1826-0264	AD7520LN
U5	1820-0683	SN74S74N
U6	1820-1430	SN74LS161AN
U9	1820-1858	SN74LS377N
U10	1820-0640	SN74150N
U11	1820-2244	SN74LS378N
U13, U15	1820-1197	SN74LS00N
U14	1820-1430	SN74LS161AN
U16	1820-1112	SN74LS74AN

Figure 8-31. A8 10V Ramp/Timebase Assembly





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION
2. UNLESS OTHERWISE INDICATED
   RESISTANCE IN OHMS
   CAPACITANCE IN MICROFARADS
   INDUCTANCE IN HENRIES

A9 Reference Designations
C1-37
CR1-17
L1-3
Q1-34
R1-103
TP1-3
U1-7
W1

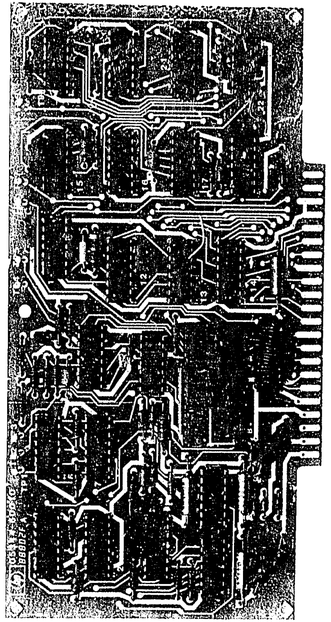
A9 TABLE OF ACTIVE ELEMENTS

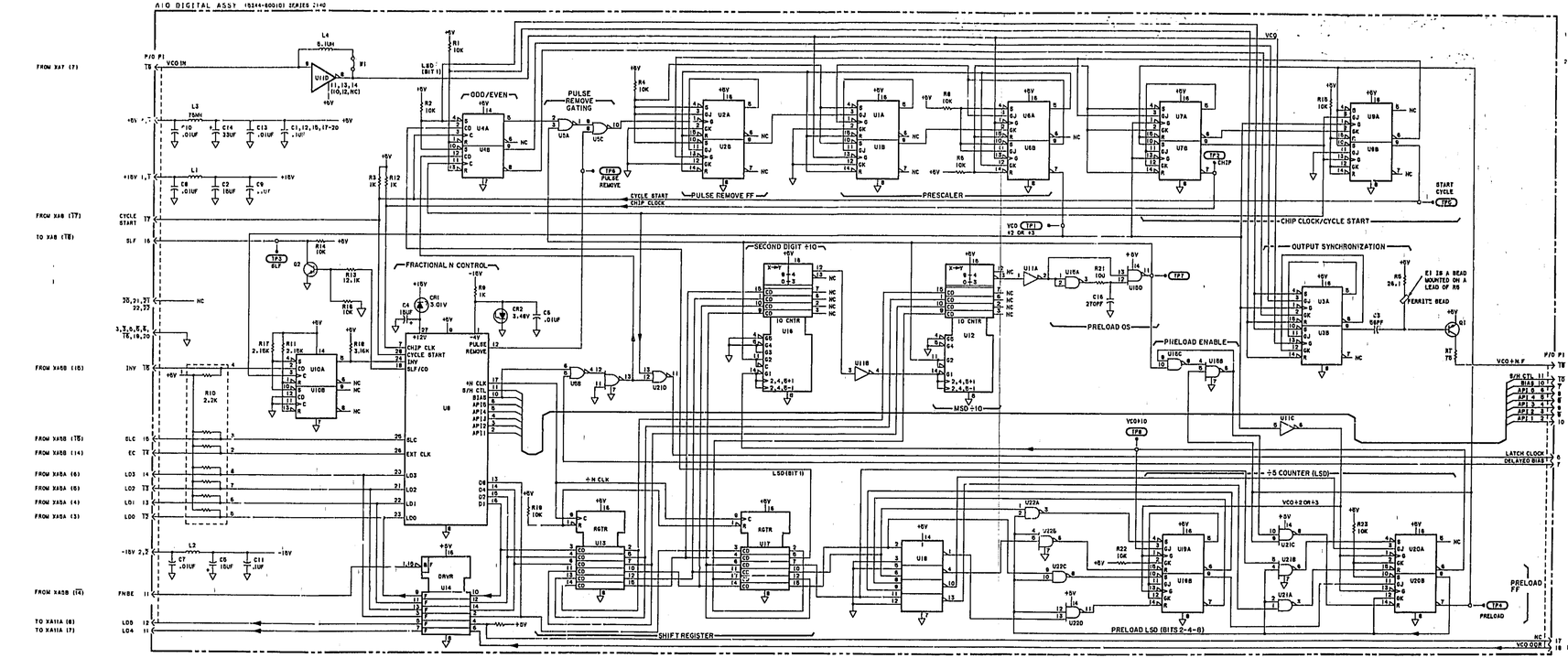
Reference Designations	HP Part Number	Mfr. Part Number
CR1, CR3-6, CR6, CR12-13, CR15-16	1901-0050	1901-0050
CR2, CR9, CR10, CR14	1901-0535	1901-0535
CR7, CR8 CR11 CR17	1902-0777 1902-0680 1902-3084	1N825 1N827 1902-3084
Q1, Q3, Q4, Q5, Q15, Q22, Q27, Q29, Q32	1853-0086	2N4917
Q2 Q6, Q12 Q7, Q8, Q11, Q30 Q9, Q10, Q24, Q25	1854-0221 1855-0082 1854-0215 1855-0081	1854-0221 1855-0082 2N3904 1855-0081
Q13, Q14, Q16 Q15 Q17	1853-0448 1854-0345 1855-0049	MPSH81 2N5179 1855-0049
Q19, Q20, Q21, Q23, Q26, Q28, Q31, Q33, Q34	1854-0798	1854-0798
U1 U2 U3 U4 U5 U6 U7	1820-1198 1820-1112 1820-0817 1826-0043 1821-0001 1820-0493 1826-0208	SN74LS174N SN74LS74AN MC10131P CA3011 CA3046 LM307N LM310N

A9 TABLE OF ACTIVE ELEMENTS

Reference Designations	HP Part Number	Mfr. Part Number
CR1, CR3-5, CR6, CR12, CR13, CR15, CR16	1901-0050	1901-0050
CR2, CR9, CR10, CR14	1901-0535	1901-0535
CR7, CR8, CR11 CR17	1902-0777 1902-0680 1902-3084	1N825 1N827 1902-3084
Q1, Q3, Q4, Q5, Q15, Q22, Q27, Q29, Q32	1853-0086	2N4917
Q2	1854-0221	1854-0221
Q6, Q12	1855-0082	1855-0082
Q7, Q8, Q11, Q30	1854-0215	2N3904
Q9, Q10, Q24, Q25	1855-0081	1855-0081
Q13, Q14, Q16	1853-0448	MPSH81
Q15	1854-0345	2N5179
Q17	1855-0049	1855-0049
Q19, Q20, Q21, Q23, Q26, Q28, Q31, Q33, Q34	1854-0798	1854-0798
U1 U2 U3 U4 U5 U6 U7	1820-1198 1820-1112 1820-0817 1826-0043 1821-0001 1820-0493 1826-0208	SN74LS174N SN74LS74AN MC10131P CA3011 CA3046 LM307N LM310N

Figure 8-32. A9 Analog Assembly





NOTES

1 REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED A10 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION

2 UNLESS OTHERWISE INDICATED RESISTANCE IN OHMS CAPACITANCE IN MICROFARADS INDUCTANCE IN HENRIES

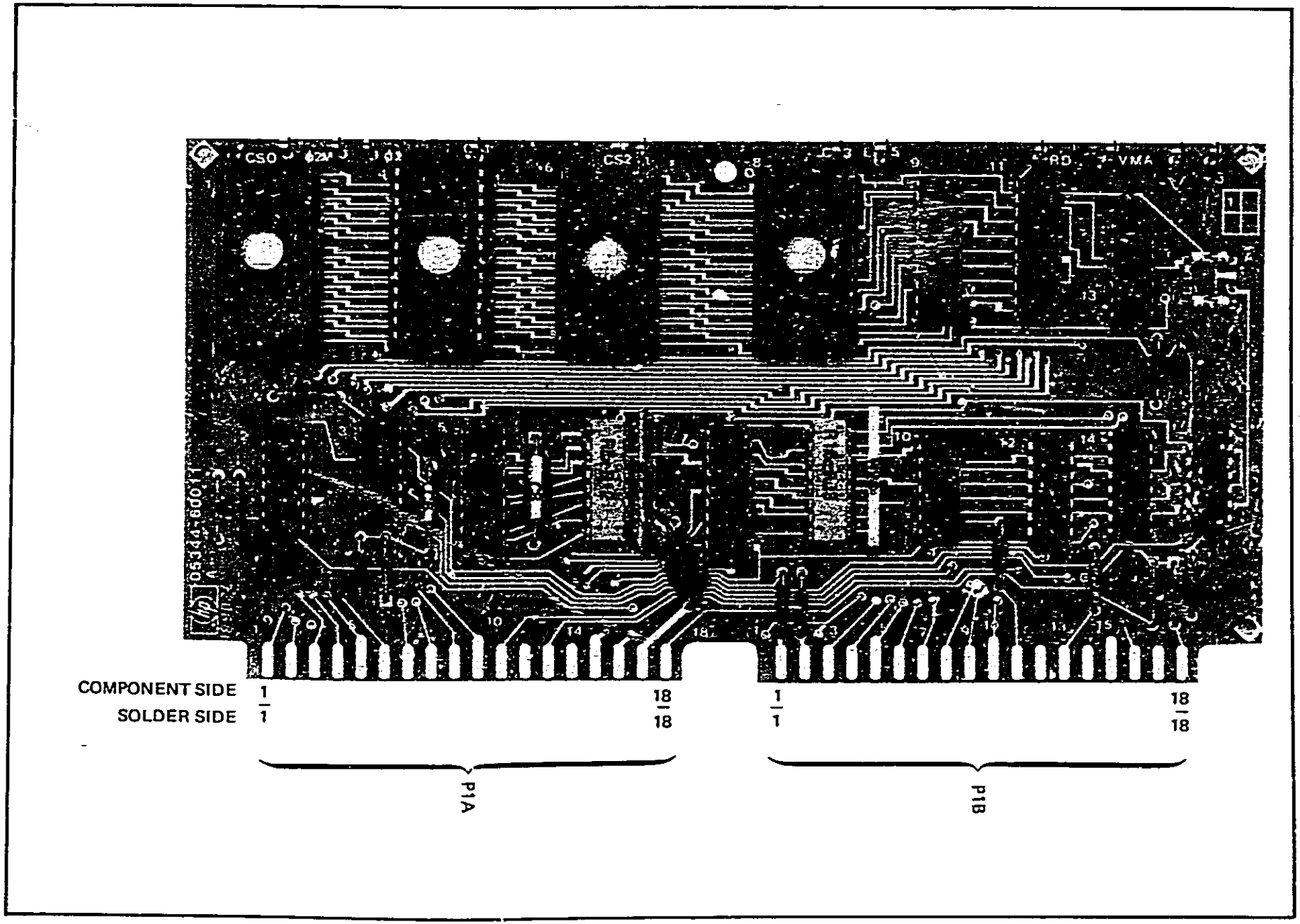
A10 Reference Designations

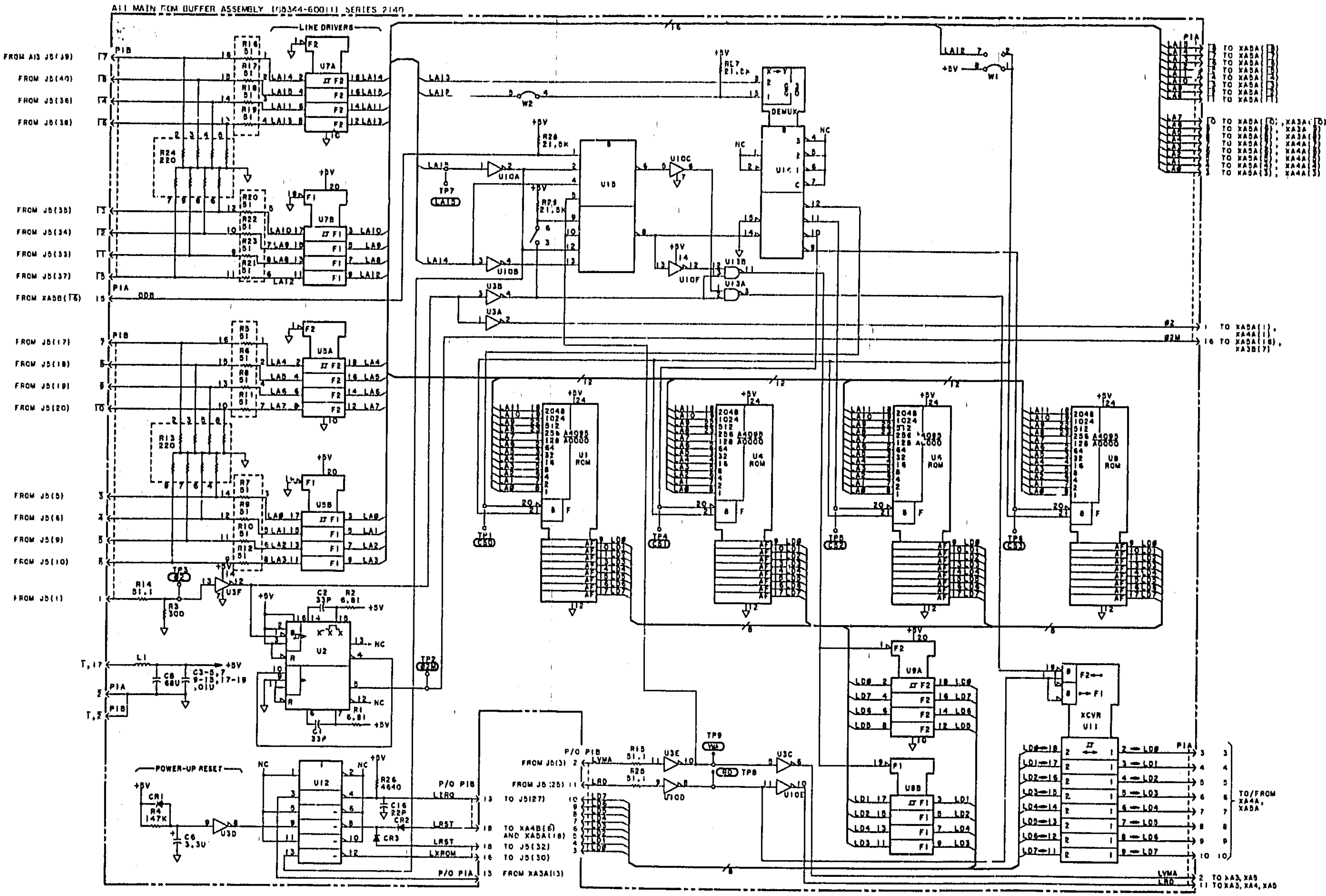
C1-20
CR1-2
E1
L1-4
Q1-2
R1-23
TP1-6
U1-22
W1
XU8

A10 TABLE OF ACTIVE ELEMENTS

Reference Designations	HP Part Number	Mfr. Part Number
CR1	1902-3030	1902-3030
CR2	1902-3044	1902-3048
Q1	1853-0448	MPS-H81
Q2	1854-0071	1854-0071
U1-3, U6, U7, U8, U19, U20	1820-0629	SN74S112N
U4-10	1820-0602	SN74S74N
U5	1820-1144	SN74LS02N
U18	1820-2004	820-2004
U11	1820-0603	SN74S00N
U12, U16	1820-1278	SN74LS190N
U13 U17	1820-1198	SN74LS174N
U14	1820-1541	SN74LS366N
U15, U21, U18	1820-1681 1820-1222	SN74S00N SN74S00N

Figure 8-33. A10 Digital Assembly


CS0
CS2
RD
VMA
05344-60011
COMPONENT SIDE
SOLDER SIDE
1
1
18
18
1
1
18
18
P1A
P1B



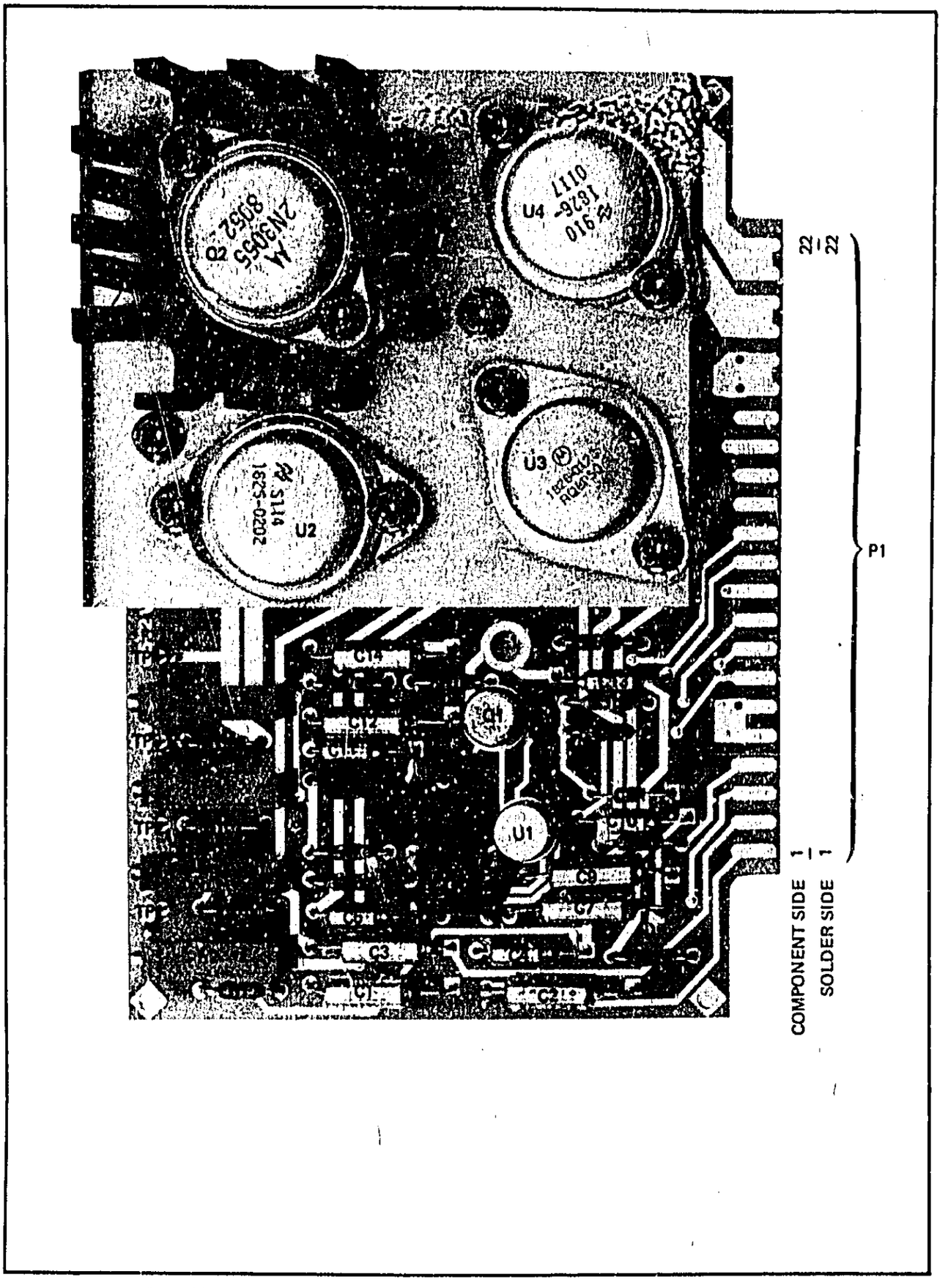
A11 Reference Designations

C1-18
CR1-3
L1
R1-28
TP1-11
U1-15
W1, W2
XU1, XU4, XU6, XU8

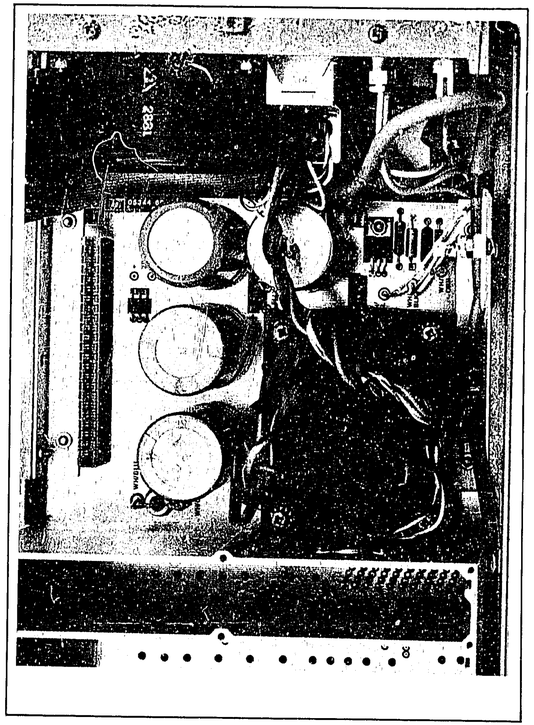
A11 TABLE OF ACTIVE ELEMENTS

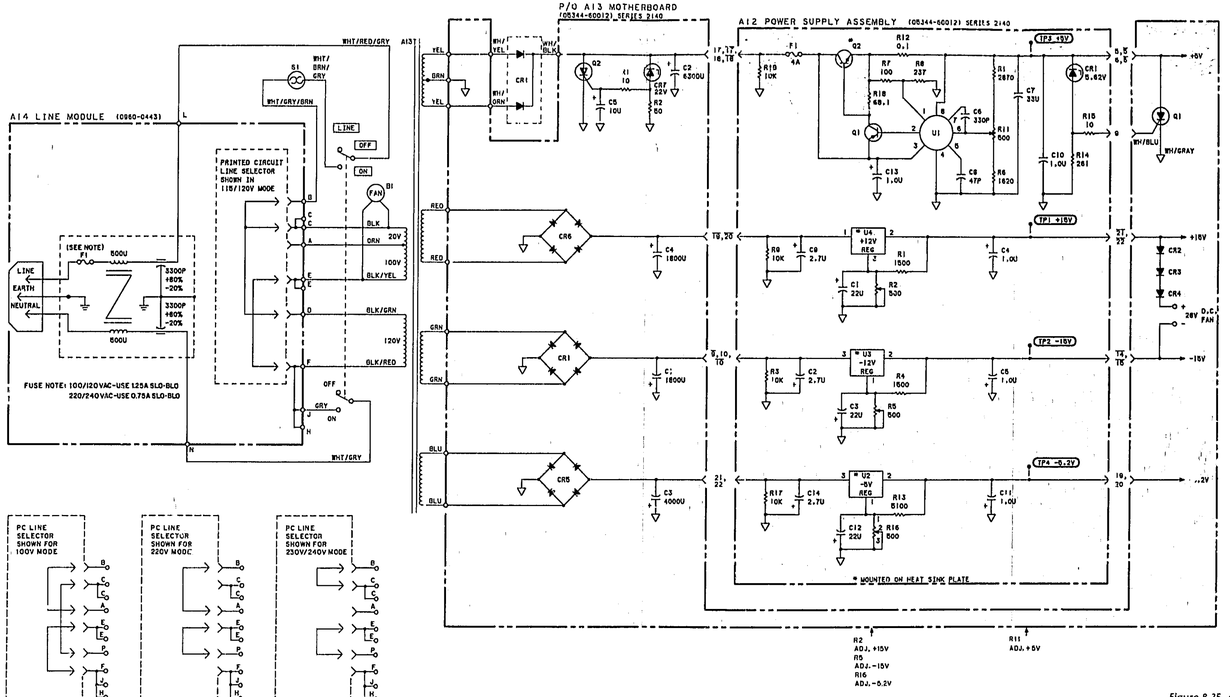
Reference Designations	HP Part Number	Mfr. Part Number
CR1-3	1901-0047	1901-0047
U1	05344-80006	05344-80006
U2	1820-1437	SN74LS221N
U3, U10	1820-1416	SN74LS14N
U4	05344-80002	05344-80002
U5, U7, U9	1820-2024	SN74LS244N
U6	05344-80003	05344-80003
U8	05344-80004	05344-80004
U11	1820-2076	SN74LS245N
U12	1820-1200	SN74LS05N
U13	1820-1197	SN74LS00N
U14	1820-1245	SN74LS155N
U15	1820-1204	SN74LS20N

Figure 8-34. A11 Main ROM/Buffer Assembly



Part of Figure 8-35. A12/A13/A14 Power Supply/Motherboard/Line Component Locator





NOTES:

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. FOR ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN FARADS; INDUCTANCE IN HENRIES

A12 Reference Designations

C1-14
CR1
F1
Q1-2
R1-18
U1-4

A12 TABLE OF ACTIVE ELEMENTS

Reference Designations	HP Part Number	Mfr. Part Number
CR1	1902-3104	1902-3104
F1	2110-0478	CAW-4
Q1	1853-0037	1823-0037
Q2	1854-0063	2N3055
U1	1826-0247	LM305H
U2	1826-0202	LM320K-05
U3	1826-0123	MC7912CK
U4	1826-0117	7812KC

A13 Reference Designations

C1-5
CR1-7
J1-4
Q1, Q2
R1, R2
T1
W1-10
XA3A, XA3B, XA4A, XA4B, XA5A, XA5B, XA6, XA7, XA8A, XA8B, XA9, XA10, XA11A, XA11B, XA12

A13 TABLE OF ACTIVE ELEMENTS

Reference Designation	HP Part Number	Mfr. Part Number
CR1, CR5, CR6	1906-0006	MDA202
CR2, CR3, CR4	1901-0731	1901-0731
CR7	1902-1268	1N5358B
Q1	1884-0024	1884-0024
Q2	1884-0066	2N6402
T1	9100-4124	9100-4224

Figure 8-35. A12 Power Supply/A13 Motherboard/ A14 Module Assembly

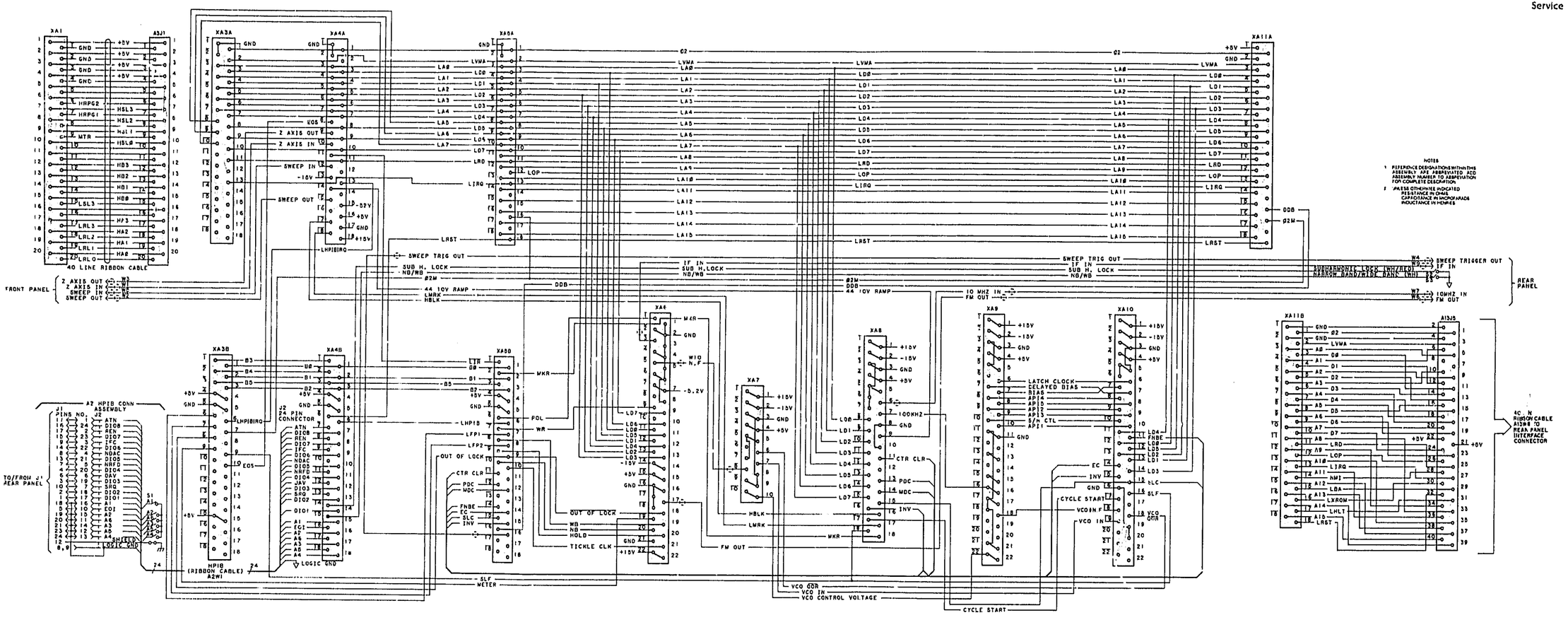


Figure 8-36. A13 Motherboard Wiring Diagram

MANUAL UPDATING CHANGES **CHANGE DATE:** July 30, 1985

*** * * * MANUAL UPDATING COVERAGE * * * ***

This supplement adapts your manual to instruments with serial numbers prefixed through 2510.

*** * * * MANUAL IDENTIFICATION * * * ***

Instrument: HP 5344S Microwave Source Synthesizer Operating & Service Manual

Manual Part No: 05344-90009
Manual Microfiche: 05344-90010
Manual Print Date: Sept 1983

ABOUT THIS SUPPLEMENT

The information in this supplement is provided to correct manual errors and to adapt the manual to instruments containing changes after the manual print date.

Change and correction information in this supplement is itemized by page numbers corresponding to the original manual pages. The pages in this supplement are organized in numerical order by manual page number.

Manual updating supplements are revised as often as necessary to keep manuals as accurate as possible. Hewlett-Packard recommends that you periodically request the latest edition of this supplement. Free copies are available from all HP offices. When requesting copies quote the model number, print date, and part number listed at the top of this page.

HOW TO USE THIS SUPPLEMENT

Insert this title page in front of the title page in your manual.

Perform all changes specified for "All Serials", and all changes through the Series Prefix of your instrument or board.

Insert any complete replacement pages provided into your manual in the proper location.

If your manual has been updated according to the last edition of this supplement, you need only perform those changes pertaining to the new series prefix. See List of Effective Pages on the reverse side of this page. New information affecting "All Serials" will be indicated by a "Ø" in front of the page number.

HEWLETT PACKARD

SALES & SUPPORT OFFICES
Arranged alphabetically by country

LIST OF EFFECTIVE PAGES

SERIAL PREFIX OR SERIAL NUMBER	PAGES
All Serials	6-3, 6-7, 6-27
2314A	6-7, 6-8
2415A	6-9, 6-10, 8-103
2438A	6-27
2510A	1-5, 2-4, 6-3, 6-27 This changes 5344S cabinet parts and hardware from "inch" to "metric".

(5344S)2314=14862,15882/2415=16260/2438=16334,16881/2510A=16666,16734

MANUAL CHANGES MODEL (05344-90009)

SERIAL PREFIX OR SERIES NUMBER	CHANGES

Page 1-5. General Information:

2510A

Table 1-2. Equipment Supplied:
>Change Front Handles part number from 5060-9899 to 5061-9499.
>Change Front Link Locks part number from 0050-0515 to 0050-2166.
>Change screws for Link Locks from 2510-0192 to 0515-1055 SCREW-MACH M4 X 0.7, 6MM LG.

Page 2-4. Installation:

2510A

Paragraph 2-19. Mating Counter to 5344A:
>Change 'Four 6-32 x 3/8" screws' to 'Four M4 x 0.7, 6mm Lg screws' in step a(3).
>Change 'Four 6-32 x 7/16" screws' to 'Four M3.5 x 0.6, 10mm lg screws' in step a(4).
>Change '(for 6/32 x 7/16" screws)' to '(for M3.5 x 0.6, 10mm lg screws)' in step a(5).
>Change '6-32 x 3/8"' to 'M4 x 0.7, 6mm lg' in steps c and d.
>Change '6-32 x 7/16"' to 'M3.5 x 0.6, 10mm lg' in step h.

Page 6-3, Figure 6-1. 5344A Mechanical Parts, Exploded View:

\# All Serials

>Change "(Option 1412)", Front Handle Kit, to "(Part of Option 142)".

2510A

>Change Lock Links (4) from 0050-0515 to 0050-2166.
>Change Front Frame from 5020-8815 to 5021-5815.
>Change Rear Frame from 5020-8816 to 5021-5816.
>Change Corner Strut from 5020-8837 to 5021-5837.
>Change Corner Strut screws from 2510-0192 to 0515-1331 SCREW-MACH M4 X 0.7, 25MM LG.
>Change Front Handle Kit (Opt 142) from 5061-0089 to 5061-9689.

Page 6-7, Table 6-2. A2 Connector Assembly Replaceable Parts:

All Serials

>Change A2J1 from 1251-3283 to 1252-0324 CONNECTOR, 24-PIN.

2314

>Delete A2J2 SOCKET-IC.
>Change S1 from 3101-1973 to 3101-2215 SW-DIP 7 SPST RDR.

MANUAL CHANGES MODEL (05344-90009)

SERIAL PREFIX OR SERIES NUMBER	CHANGES

Page 6-8, Table 6-2. A3 Keyboard/Display Interrupt Assy Replaceable Parts:

2314 >Change U11 from 1820-1207 to 1820-3460 IC-GATE TTL LS NAND 8-INP.

Pages 6-9/6-10, Table 6-2. A4 HP-IB Interface Assembly Replaceable Parts:

2415 >Change A4 (05344-60004) SERIES to 2415.
>Change A4U7 from 1820-2485 to 1820-3431 IC-TRANSCEIVER TTL LS INSTR-BUS IEEE-448.

Page 6-27, Table 6-2. Replaceable Chassis Parts:

2438 >Change RPG1 from 5060-0329 to 0960-0684 ROTARY PULSE GENERATOR, INPUT POWER: 5VDC.

Page 6-27, Table 6-2. Miscellaneous Parts:

All Serials >Change "(OPTION 1412)", Kit-Front Handle, to "(Part of Option 142)".

2510A >Change Link Lock-Front from 0050-0515 to 0050-2166.
>Change Frame-Front from 5020-8815 to 5020-5815.
>Change Frame-Rear from 5020-8816 to 5021-5816.
>Change Strut-Corner from 5020-8837 to 5021-5837.
>Change Strap-Handle Cap, Front from 5040-7219 to 5041-6819.
>Change Strap-Handle Cap, Rear from 5040-7220 to 5040-7221.
>Change Strap-System II from 5060-9899 to 5061-9499.
>Change Cover-Bottom from 5061-1940 to 05342-60141.
>Add 0515-0893 SCREW-MACH M3.5 X 0.6, 10MM LG (for Cable Shield).
>Add 0515-0896 SCREW-MACH M4 X 0.7, 10MM LG (for Front Handles).
>Add 0515-1055 SCREW-MACH M4 X 0.7, 6MM LG (for Link Lock).
>Add 0515-1132 SCREW-MACH M5 X 0.8, 10MM LG (for Strap Handle).
>Add 0515-1331 SCREW-MACH M5 X 0.8, 25MM LG (for Corner Struts).

Page 6-27, Table 6-2. Option Kits:

All Serials >Change 5061-0089, Kit-Front Handle (Option 1412) to "(Part of Option 142)".

2510A >Change Kit-Rack Flange (Opt 908) from 5061-0077 to 5061-9677.
>Change Kit-Front Handle (Opt 142) from 5061-0089 to 5061-9689.
>Change Rack-Flange (Opt 913) from 5061-2071 to 5061-9771.

Page 8-103, Figure 8-27. A4 Interface/A2 HP-IB Connector Assembly:

2415 >Change A4 (05344-60004) SERIES to 2415.