MODEL 4271 A 1 MHz DIGITAL LCR METER

SERIAL PREFIXED: 1310J-

See Section VII for Other Serial Prefixes.

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Part No. 04271-99000

Printed: AUG. 1973



SECTION I GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This section contains general information about the Model 4271A 1 MHz DIGITAL LCR METER. A general description plus information on specifications, accessories, and instrument identification is given.

1-3. SPECIFICATIONS.

1-4. Table 1-1 is a complete list of the Model 4271A critical specifications that are controlled by tolerances. Table 1-2 contains general information that describes the operating characteristics of the 4271A.

1-5. DESCRIPTION.

1-6. Automatic high speed, precision L, C and Loss Measurements are features of this new Model 4271A 1 MHz Digital LCR Meter. Using a four-terminal pair measurement technique to minimize stray capacitance and residual inductance, with low level test signals convenient for semi-conductors, capacitance measurements from 00.000pF to 19.000nF and inductance measurements from 0000.0nH to 1900.0 $\mu\rm H$ are easily made. Basic capacitance measurement accuracy is 0.1%. Readout is 4-digit LED display

with 90% overrange. Capacitance loss components are measured as paralleled conductance (100.00 μδ to 100.00m % in 4 ranges) or dissipation factor (to 1.0000). Inductance loss components are measured as series resistance (10.000 Ω to 10.000 $k\Omega$) or dissipation factor (to 1,0000). Selectable functions with loss components simultaneously displayed are C-D, C-G, L-R or L-D. Loss readout is 4-digit LED display. Capacitance measurement test voltages are 20 mV rms -LOW, 500 mV rms-HIGH and inductance test currents are 5 DC bias variable from 00.0 V to 39.9 V mA to $2\mu A$. in 0.1 V steps is optional. Full interface compatibility with HP calculators and digital recorders completes the versatile Model 4271A. Typical applications are C and L measurements of discrete components in the laboratory or on the production line, semi-conductor measurements and L or C examinations of delay lines and pulse transformers.

1-7. INSTRUMENT IDENTIFICATION.

1-8. Hewlett-Packard uses a two-section nine-character (0000J00000) or eight-character (000-00000 or 000J00000) serial number. The first three of four digits (serial prefix) identify a series of instruments;

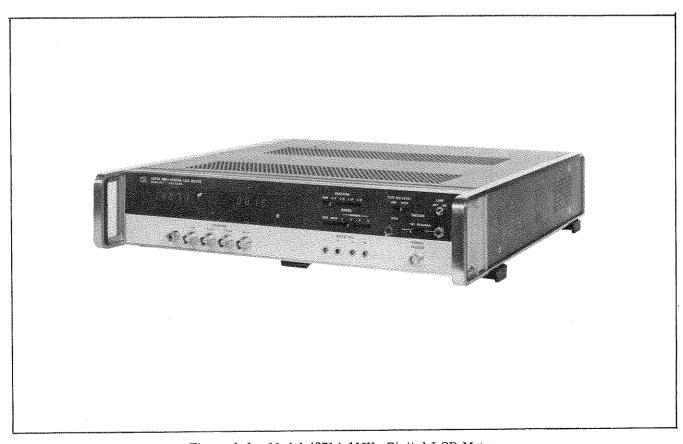


Figure 1-1. Model 4271A 1MHz Digital LCR Meter.

CAPACITANCE MEASUREMENT

<u>Parameters Measured</u>: Capacitance and conductance (C-G) or capacitance and dissipation factor (C-D).

Measurement Circuit: Capacitance-equivalent parallel conductance by four-terminal pair method.

Available Full Scale Ranges:

	RANGE	Capacitance	Conductance	DISSIPATION FACTOR*
Full Scale Display	1 2 3	10.000pF 100.00pF 1000.0pF	100.00μຽ 1000.0μຽ 10.000mຽ	1.0000
Over- range	1-4	10,000nF 90%	100.00m ³	60%

* When reading of C is more than 1500 counts.

Test Signal:

Test Level:

RANGE	TEST SIG LEVEL-HIGH	TEST SIG LEVEL-LOW
1	$500~\mathrm{mVrms}\pm10\%$	$20~\mathrm{mVrms}\pm10\%$
2	$500~\mathrm{mVrms}\pm10\%$	20 mVrms ± 10%
3	$500~\mathrm{mVrms}\pm10\%$	$20~\mathrm{mVrms}\pm10\%$
4	$20~\mathrm{mVrms} \pm 20\%$	$20~\mathrm{mVrms} \pm 20\%$

Frequency: 1MHz ±0.01%

Offset Adjustment: OFFSET ADJ compensates for stray capacitance or residual conductance of test fixture. The variable ranges are 1pF and 1μδ.

Accuracy: Conditions-Conductance reading is less than 100 counts.

Accuracy listed in Table applies over a temperature range of $23^{\circ}C$ $\pm 5^{\circ}C$. (At $0^{\circ}C$ to $50^{\circ}C$, accuracy is doubled).

Warm-Up Time: ≥60 min.

Accuracy Check: HP Model 16021A Test Fixture should be used to prevent errors caused by improper connection to standard device.

Accuracy of Capacitance Measurements:

RANGE	TEST SIG LEVEL-HIGH	TEST SIG LEVEL-LOW
	\pm (% of reading + counts)	±(% of reading + counts)
1	0.1 + 7	0.2 + 8
2	0.1 + 3	0.2 + 4
3	0.1 + 3	0.2 + 3
4*	0.4 + 3	0.4 + 3

Accuracy of Conductance Measurements:

RANGE	TEST SIG LEVEL-HIGH	TEST'SIG LEVEL-LOW
	\pm (% of reading + counts)	±(% of reading + counts)
1	$0.2 + (7 + \frac{Nc}{1000})$	$0.3 + (7 + \frac{2}{1000} \text{ Ne})$
2	$0.2 + (3 + \frac{Nc}{1000})$	$0.3 + (3 + \frac{2}{1000} \text{ Nc})$
3, 4*	1.2 + $(2 + \frac{2}{1000} \cdot Nc)$	1. 2 + $(2 + \frac{2}{1000} \cdot \text{Nc})$

Where N_C is capacitance readout in counts.

Accuracy of Dissipation Factor Measurements:

RANGE	TEST SIG LEVEL-HIGH	TEST SIG LEVEL-LOW
	\pm (% of reading + counts)	\pm (% of reading + counts)
1.	1.0 + $(10 + \frac{20,000}{Nc})$	1. 0 + $(15 + \frac{30,000}{Nc})$
2, 3	$1.0 + (10 + \frac{10,000}{Nc})$	1.0 + $(15 + \frac{20,000}{Nc})$
4*	1. $0 + (15 + \frac{30,000}{Nc})$	1. 0 + (15 + $\frac{30,000}{\text{Nc}}$)

* On Range 4, Test Sig Level is Low only. where N_{C} is capacitance readout in counts.

INDUCTANCE MEASUREMENT

Parameters Measured: Inductance, equivalent series resistance or dissipation factor.

Measurement Circuit: Inductance, equivalent series resistance using four-terminal pair method.

Available Full Scale Ranges:

	RANGE	Inductance	Resistance	DISSIPATION FACTOR*
	1	1000.0nH	10.000Ω	
Full Scale	2	10.000 μH	100.00Ω	1,0000
Display	3	100.00 μH	1000.0Ω	1,0000
	4	1000.0μH	10,000kΩ	
Over Range	1-4	90%	90%	60%

* When reading of L is more than 1500 counts.

Test Signal:

Test Level:

RANGE	TEST SIG LEVEL-HIGH	TEST SIG LEVEL-LOW
1	$2~\mathrm{mA~rms}\pm20\%$	$2 \text{ mA rms} \pm 20\%$
2	$5~\mathrm{mA~rms}\pm10\%$	200 μ A rms \pm 10%
3	500 $\mu A \; \mathrm{rms} \pm 10\%$	$20~\mu A~{ m rms} \pm 10\%$
4	50 μ A rms \pm 10%	$2~\mu A~{ m rms} \pm 10\%$

Frequency: 1MHz ±0.01%.

Offset Adjustment: OFFSET ADJ compensates for residual inductance or residual resistance of test fixture. The variable range are 100nH and $100m\Omega$.

 $\frac{\text{Accuracy:}}{1000 \text{ counts.}} \text{ When resistance reading is less than}$

Accuracy listed in Table applies over a temperature range of 23°C $\pm 5^{\circ}$ C. (At 0°C to 50°C, accuracy is doubled).

Warm-Up Time: ≥ 60min.

Accuracy Check: HP Model 16021A Test Fixture should be used to prevent errors caused by improper connection to standard device.

Accuracy of Inductance Measurement:

RANGE	TEST SIG LEVEL-HIGH	TEST SIG LEVEL-LOW
	\pm (% of reading + counts)	±(% of reading + counts)
1*	1.0 + 15	1.0 + 15
2	0.6 + 4	0.6 + 6
3, 4	0.2 + 4	0.3 + 6

Accuracy of Resistance Measurement:

RANGE	TEST SIG LEVEL-HIGH	TEST SIG LEVEL-LOW
- Idanida	TENT NO DEVEN-111011	TENT MA BEVEL DON
	\pm (% of reading + counts)	$\pm (\% \text{ of reading } + \text{ counts})$
1*	$1.2 + (8 + \frac{2}{1000} \cdot NL)$	1.2 + $(8 + \frac{2}{1000} \cdot NL)$
2	$1.2 + (2 \div \frac{2}{1000} \cdot N_L)$	1.2 + $(2 + \frac{2}{1000} \cdot NL)$
3,4	$0.2 + (2 + \frac{2}{1000} \cdot NL)$	$0.3 + (2 + \frac{2}{1000} \cdot NL)$

Where N L is inductance readout in counts.

Accuracy of Dissipation Factor Measurement:

RANGE	TEST SIG LEVEL-HIGH	TEST SIG LEVEL-LOW
	\pm (% of reading + counts)	\pm (% of reading + counts)
1*	$1.0 + (20 + \frac{30,000}{N_L})$	$1.0 + (20 + \frac{30,000}{NL})$
2, 3	$1.0 + (15 + \frac{10,000}{NL})$	$1.0 + (20 + \frac{20,000}{NL})$
4	$1.0 + (15 + \frac{20,000}{NL})$	$1.0 + (20 + \frac{30,000}{N_L})$

* At Range 1, TEST SIG LEVEL is LOW only. Where N_L is inductance readout in counts.

CONDUCTANCE, RESISTANCE MEASUREMENTS:

Accuracy of Conductance:

	RANGE	TEST SIG LEVEL-HIGH	TEST SIG LEVEL-LOW
		\pm (% of reading + counts)	\pm (% of reading + counts)
-	1.	0.2 + 8	0.3 + 9
	2	0.2 + 4	0.3 + 5
	3, 4*	1,2 + 4	1.2 + 4

* On Range 4, TEST SIG LEVEL is LOW only.

Accuracy of Resistance:

RANGE	TEST SIG LEVEL-HIGH	TEST SIG LEVEL-LOW
	\pm (% of reading + counts)	\pm (% of reading + counts)
1*	1.2 + 10	1.2 + 10
2	1.2 + 4	1.2 + 4
3, 4	0.2 + 4	0.3 + 4

* Measuring Signal Level and accuracy are the same when TEST SIGNAL LEVEL is set to HIGH or to LOW.

Note 1

Measurement accuracy of capacitance or inductance accompanied by other very small parameters (conductance or resistance) is described in Capacitance Measurement or Inductance Measurements, measuring accuracy specifications for conductance or resistance is given for capacitance or inductance readings of less than 1000 counts.

Note 2

The specifications of parameters measured, measuring circuit, measuring range, offset adjust and measuring signal are the same for both Capacitance Measurements and Inductance Measurements.

Accuracy listed in Table applies over a temperature range of 23° C $\pm 5^{\circ}$ C. (At 0° C to 50° C, accuracy is doubled).

Warm-Up Time: ≥ 60min.

Accuracy Check: HP Model 16021A Test Fixture should be used to prevent errors caused by improper connection to standard device.

DC BIAS

<u>Internal Source</u>: DC bias is available as a built-in source (Option 001) which has following specifications:

Range: 00.0V to 39.9V, variable in steps of 0.1V.

Accuracy: ±0.2% of setting ±5mV. (When ambient temperature is at 23°C ±5°C and warm up time is more than 60min).

Output Resistance: $1.5 \text{k}\Omega \pm 10\%$. Bias voltage is applied to H_{CUR} terminal.

Short Circuit Current: Less than 6mA.

Control: Controlled by HP Model 16023A DC Bias Controller (available extra) or HP Model 9810/ 9820A Calculator when Option 005 is installed.

Control Input Connector: HP P/N 1251-0143, 14-pin receptacle, (Amphenol 57-40140).

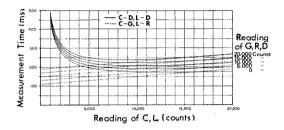
Mating Connector: HP Part No. 1251-0142. (Amphenol 57-30140).

External Source: Provision for external dc bias voltage of $\pm 200 \text{V}$ maximum with maximum bias current of 20 mA to BNC connector (EXT INPUT) on rear panel. Input Resistance (series): $10.5 \text{k}\Omega \pm 10\%$.

Monitor Output: Bias voltage monitoring BNC connector (MONITOR) on rear panel. Output resistance: $480\Omega \pm 10\%$ to Hcur terminal.

The general information listed below is presented as a typical performance guide rather than specification data which it is not.

Measuring Time: The following diagram shows time as a function of measured parameter and value when Range is fixed. When Auto Range is selected a range selection time of 100 msec/range step is added to times shown below.



Reading Rate: Reading rate is defined as the time required for one measurement cycle plus time interval between completion of a measurement cycle and the start of next cycle. The Trigger Rate control varies time internal between finish time of a measurement cycle and start of next cycle (5 msec minimum/3 sec maximum).

REMOTE/MANUAL TRIGGER: After completion of a measurement cycle, a new cycle may be started by pushing MANUAL TRIGGER button or by remote trigger input to REMOTE TRIGGER connector.

REMOTE TRIGGER Input: A measurement cycle may be initiated at Remote Trigger Connector by changing logic level state from "0" (zero volts or connection to ground through less than 200Ω) to "1" (TTL high level or open), pulse width; $\geq 1 \, \mu \text{sec}$.

MANUAL TRIGGER button: Releasing TRIGGER button (when depressed) initiates new measurement cycle.

DATA OUTPUT & CONTROL INPUT

BCD Output: Three options for varying kinds of data and output format are available.

Option 002: BCD Output of capacitance or inductance.

Option 003: BCD Output of conductance, resistance or dissipation factor.

Option 004: Serial BCD Output of capacitance/inductance and conductance/resistance/dissipation factor.

Output Signal: 1-2-4-8 code, bit and digit-parallel.

Data-4-1/2 digits, Polarity-1/2 digits, announciation Signal-1 digit, Decimal Point-1 digit and Unit-1 digit.

Level:

STATE	LEVEL	OUTPUT CHARACTERISTICS
LOW	0 to 0.4V	Maximum Sink Current-16mA
HIGH	4. 2V to 5V	Output Impedance – 300Ω

* OPT 004 Uses Ground True.

Print Command: Positive pulse, +5V, approx. $35 \mu sec$ wide. Output Impedance 300 Ω .

Hold Off: Level +2.5V to 15V with an input impedance of $10k\Omega$.

Output Connector: HP Part No. 1251-0087. 50-pin receptacle, (Amphenol 57-40500-375, HP Part No. 1251-0086) Mating Connector (Amphenol 57-30500).

ASCII code input/output for calculatorsOption 005: Enables interface with HP Model 9810A

Calculator using HP Model 11202A TTL I/O Interface Card and HP 11264A Peripheral Control Block or with HP Model 9820A Calculator using HP Model 11202A TTL I/O Interface Card and HP 11220A or HP 11224A Peripheral Control Block.

Accessory furnished: HP 16022A Test Fixture for general purpose component measurements.

Operating Temperature and Humidity: 0°C to 50°C relative humidity to 95% at 40°C.

Power Requirements: $100/120/220/240V \pm 10\% 48-66$ Hz. Power dissipation; ≤ 80 VA with any option.

Dimensions: 426 x 99 x 467 mm (W x H x D).

Weight: Approximately 10kg.

the last five digits identify a particular instrument in that series. A letter placed between the two sections identifies the country where the instrument was manufactured. The serial number appears on a plate located on the rear panel. All correspondence with Hewlett-Packard Sales/Service Offices with regard to an instrument should refer to the complete serial number.

1-9. MANUAL CHANGES.

- 1-10. This manual provides operating and service information for the HP Model 4271A 1 MHz Digital LCR Meter. The information in this manual applies directly to an instrument with the serial prefix or number indicated on the title page of this manual.
- 1-11. If the serial prefix of an instrument is higher than that on the title page, a "Manual Changes" sheet supplied will describe changes which will adapt this manual to provide correct coverage. Technical corrections (if any) to this manual, due to known error in print, are called Errata and are shown on the change sheet.
- 1-12. If the serial prefix or number of an instrument is lower than that on the title page, see Section VII Manual Changes and Options. For information on Manual coverage of any HP instrument, contact the nearest Hewlett-Packard Sales/Service Office (addresses are listed at the rear of this manual).

1-13. OPTION.

1-14. The 4271A currently includes five options given in Table 1-3 which follows.

Table 1-3. Options.

Options	Description
001	DC BIAS SUPPLY
002	C/L BCD OUTPUT
003	G/R/D BCD OUTPUT
004	PARAMETER SERIAL BCD OUTPUT
005	CALCULATOR INTERFACE

1-15. For more option information, refer to Section III and VII.

1-16. ACCESSORIES.

1-17. HP Model 16022A, which is Test Fixture for general purpose component measurements, is furnished. Accessories available for Model 4271A are listed below. See Figure 1-2 for accessory illustrations.

NOTE

The Model 16022A General Purpose Test Fixture is a furnished accessory only when a 4271A is ordered directly from an HP sales office outside Japan. This accessory is not included in sales price of Models 4271A sold in Japan including those sold to OEM manufacturers. Customers receiving instruments from OEM manufacturers in Japan should order this item separately.

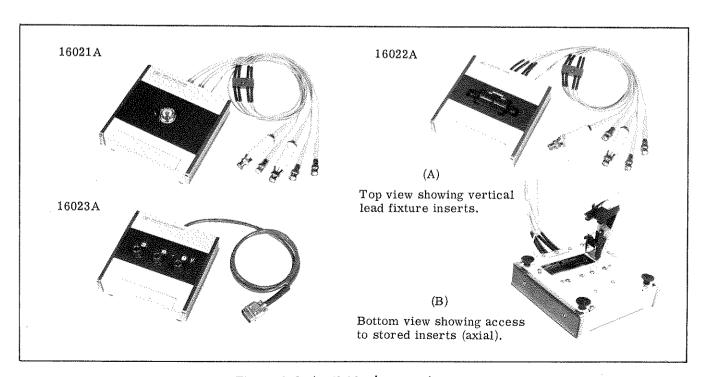


Figure-1-2 Available Accessories.

Table 1-4. Available Accessories.

Accessory	Description
Model 16021A	Calibration Connector - for calibration of 4271 A (Includes GR-900® connector).
Model 16023A	Bias Voltage Controller.
Model 16032A	Test Lead - with BNC con- nector.
Model 16033A	Test Lead - with small coaxial connector (HP P/N 1250-0324).

See Paragraphs 3-46 to 3-55 for use of these accessories.

SECTION II INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information and instructions necessary for the installation and shipping of the Model 4271A 1MHz Digital LCR Meter. Included are initial inspection procedures, power and grounding requirements, environmental information, and instructions for repackaging for shipment.

2-3. INITIAL INSPECTION.

2-4. This instrument was carefully inspected both mechanically and electrically before shipment. It should be free of mars or scratches and inperfect electrical order upon receipt. To confirm this, the instrument should be inspected for physical damage in transit, and its electrical performance should be tested using the procedure outlined in Paragraph 5-7. If there is damage or deficiency, see the warranty inside the front cover of this manual.

2-5. POWER REQUIREMENTS.

2-6. The Model 4271A can be operated from any ac voltage source of 100V, 120V, 220V or 240V $(\pm\ 10\%)$

at 48 to 66Hz (see Figure 2-1). Power dissipation is 80VA maximum.

2-7. GROUNDING REQUIREMENTS.

- 2-8. To protect operating personnel, the National Electrical Manufacturer's Association (NEMA) recommends that the instrument panel and cabinet be grounded. The Model 4271A is equipped with a three-conductor power cable which, when plugged into an appropriate receptacle, grounds the instrument. The offset pin on the power cable is the ground wire.
- 2-9. To preserve the protection feature when operating the instrument from a two-contact outlet, use a three-prong to two-prong adapter (HP Part No. 1251-0048) and connect the green pigtail on the adapter to power line ground.

2-10. ENVIRONMENTAL REQUIREMENTS.

2-11. The Model 4271A should not be operated where the ambient temperature range exceeds 0°C to 50°C (32°F to 122°F) or stored where the ambient temperature range exceeds -40°C to 70°C (-40°F to 153°F).

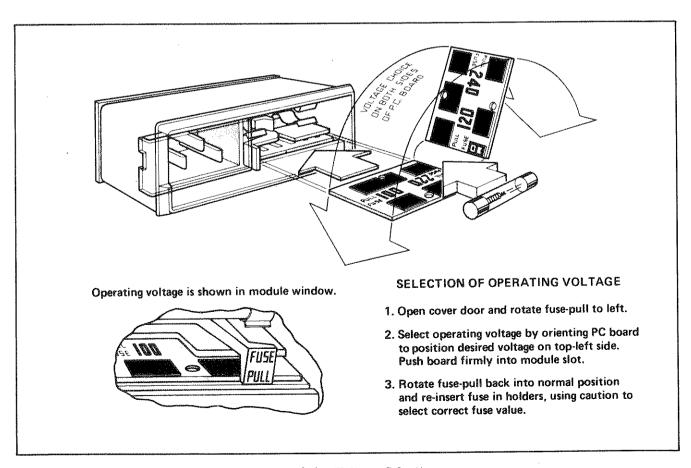


Figure 2-1. Voltage Selection.

The Model 4271A requires no fan (cast side frames are heat sinks). Instrument can be rack mounted with normal considerations for venting.

2-12. RACK INSTALLATION.

2-13. The Model 4271A is ready for bench operation as shipped from the factory. Additional parts necessary for rack mounting are packaged with the instrument. To convert for rack installation, refer to Figure 2-2 and proceed as follows:

- a. Remove tilt stand.
- Remove feet (press the foot-release button, slide foot toward center of instrument, and lift off).
- c. Remove adhesive-backed trim strips.
- d. Attach filler strip along bottom edge of front panel.
- e. Attach flanges to front end of sides (larger corner-notch toward bottom of instrument). Instrument is now ready to mount in standard rack.

CAUTION

AMBIENT TEMPERATURE IN RACK DURING OPERATION SHOULD NOT EXCEED A MAXIMUM OF 122°F (50°C). BE SURE INSTRUMENT POSITION IN RACK PERMITS AIR CIRCULATION. IF NECESSARY, USE BLANK PANELS (HP TYPES 12680B THRU 12685B).

2-14. REPACKAGING FOR SHIPMENT.

2-15. The following paragraphs contain a general guide for repackaging the instrument for shipment. Refer to Paragraph 2-16 if the original container is to be used; 2-17 if it is not. If you have any questions, contact your nearest -hp- Sales and Service Office.

Note

If the instrument is to be shipped to Hewlett-Packard for service or repair, attach a tag to the instrument identifying the owner and indicating the service or repair to be accomplished. Include the model number and full serial number of the instrument. In any correspondence, identify the instrument by model number and full serial number.

- 2-16. Place instrument in original container with appropriate packing material and seal with strong tape or metal bands. If original container is not available, one can be purchased from your nearest -hp-Sales and Service Office.
- 2-17. If original container is not to be used, proceed as follows:
 - a. Wrap instrument in heavy paper or plastic before placing in an inner container.
 - Place packing material around all sides of instrument and protect panel face with cardboard strips.
 - c. Place instrument and inner container in a heavy carton or wooden box and seal with strong tape or metal bands.
 - d. Mark shipping container "DELICATE INSTRU-MENT", "FRAGILE", etc.

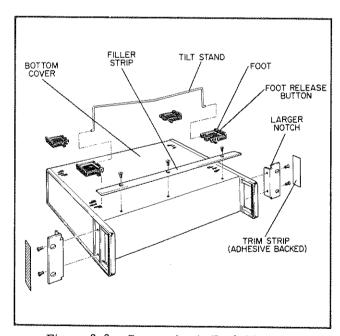


Figure 2-2. Conversion to Rack Mounting.

SECTION III OPERATION

3-1. INTRODUCTION.

3-2. In this section, the operation of the Model 4271A 1MHz Digital LCR Meter is described and certain recommended operating considerations are treated. The section includes an explanation of front and rear panel controls and connectors, major operating characteristics, operating procedures for the 4271A (and its options) and other required information for effective use of the instrument.

3-3. APPLICATIONS.

3-4. The Model 4271A accurately measures the capacitance, inductance, resistance, conductance and dissipation factors of capacitors and inductors in general use. While the 4271A has a very wide range of application, it is particularly suitable for measurement of capacitances of semiconductor devices, especially a variable capacitance diode. The instrument also provides for measurement applications requiring a DC bias voltage and for processing and recording the measured data. Thus, a wide variety of available features increase the applications versatility of the instrument.

3-5. MEASURING LIMITS.

3-6. The measuring limits of the 4271A are shown in Table 1-1 Specifications. However, as you will learn from a study of the operation of the instrument, the specifications do change depending upon settings of FUNCTION and TEST SIG LEVEL of 4271A. These measuring limits should be well understood when measuring a sample with the 4271A. Measurements taken which are beyond these limits are ambiguous as measured values.

3-7. FRONT/REAR PANEL DESCRIPTIONS.

3-8. Descriptions of both front panel and rear panel controls, functions and connectors are given in Figure 3-1. The understanding of these controls and functions is essential for obtaining correct measurements with the 4271A.

3-9. PREOPERATION.

- 3-10. Before LINE switch is turned to ON and measurements attempted, perform following procedures:
 - a. Checkline voltage selector card in power module on the rear panel. Set selector card to correct position for local AC line voltage. Install fuse of proper current rating (refer to paragraph 2-5).
 - b. Connect power cord to instrument. When using an outlet without GROUND terminal, a connector adapter (HP P/N 1251-0048) should be used for safety.

c. Set front panel controls as follows:

FUNCTION	C-G
RANGE	
TEST SIG LEVEL	
RATE	centered
TRIGGER	INT
DC BIAS VTG (on rear panel) .	OFF
LINE	OFF

d. Turn LINE switch to ON. For accurate measurements allows a warm-up time of≥ 60 min. During this time the measuring rate lamp will periodically turn on and off.

CAUTION

IF A TEST FIXTURE OR A TEST CABLE IS NOT CONNECTED, THE FOUR-TER-MINAL PAIR IS NOT COMPLETED, AND COUNTER AND ANNUNCIATORS WILL DISPLAY AMBIGUOUS READINGS. THIS IS NOT A TROUBLE.

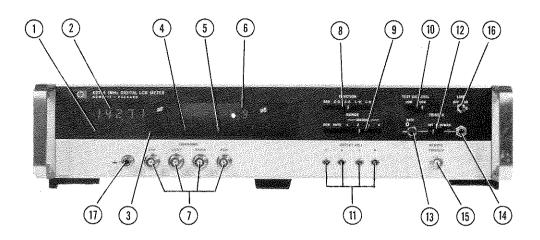
- e. Set OFFSET adjustment as required for sample being measured. Refer to paragraph 3-13.
- Connect sample to test fixture or to test leads. Read displays.

3-11. CONNECTION OF DUT (Device Under Test).

3-12. The unknown terminals are ${\rm H}_{\rm CUR}$, ${\rm L}_{\rm CUR}$, HPOTEN and LPOTEN which configure a four-terminal pair measurement arrangement as shown in Figure 3-2. When a four-terminal pair connection arrangementisemployed, current flow from H_{CUR} terminal through DUT to L_{CUR} terminal does not generate a magnetic field around the test cables since current is supplied through the center conductor coaxial cable and returns through its outer conductor. Thus an emf which might cause an error is not generated in the potential cables (voltage leads). This permits accurate measurements (e.g. even with very small inductances) without the influence of measurement cables. In practice, the four-terminal pair is converted to a 3-terminal pair or to a 2-terminal pair near the DUT. The residual impedance and stray admittance which remain in part of the connection after conversion can be compensated for by the OFF-SET Adjustment (described later).

3-13. OFFSET ADJUST.

3-14. The Model 4271A has a remarkable feature in that a zero adjustment can be performed for every test fixture. Zero offset adjustments (using the Model 16022A Test Fixture-furnished with instrument) are described in Paragraphs 3-15 through 3-18.



- Measuring Rate Lamp. Lights during measuring. During hold time lamp is extinguished.
- 2. C/L Display. Capacitance or inductance display with decimal point and unit. If this display shows "-200", C/L and G/R/D displays have no meaning.
- OUT OF RANGE Lamp. Lights when either C/L or G/R/D or both exceed the specified maximums. When this lamp lights, display indication has no meaning.
- 4. UNBAL Lamp. Lights when the bridge section is not balanced. When this lamp lights, the display indication has no meaning.
- D→G, R Lamp. Lights when the C-D or L-D mode selected and display of C or L is less than approximately 1000. When this lamp lights, set FUNCTION switch to C-G or L-R.
- 6. G/R/D Display. Conductance, resistance or dissipation factor display with decimal point and unit. If this display shows "-200", C/L and G/R/D displays have no meaning.

- 7. Unknown Terminal. Provides connections for 4-terminal pair. Instrument does not function properly unless test leads are connected to these terminals.
- 8. FUNCTION. Selects measurement functions:

C-D: Capacitance & Dissipation Factor.

C-G: Capacitance & Conductance.

L-R: Inductance & Resistance.

L-D: Inductance & Dissipation Factor.

REM: Remote Control (Optional).

9. RANGE. Selects measurement ranges:

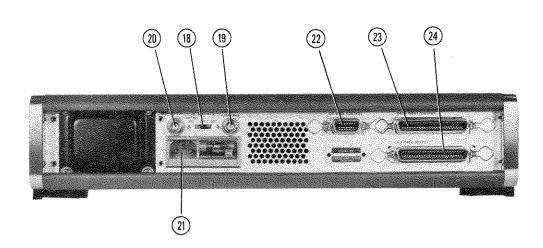
REM: Remote Control (Optional). AUTO: Automatic Range Selection.

MANUAL: 1, 2, 3 or 4.

10. TEST SIG LEVEL.

C measuring mode: Selects test signal level, HIGH (500mV) and LOW (20mV). On range 4, test signal level is limited to 20mV.

L measuring mode: Selects test signal level, HIGH ($50\,\mu\text{A}$ to 5mA) and LOW ($2\,\mu\text{A}$ to 2mA). On range 1, test signal level is limited to 2mA.



- 11. OFFSET ADJ./ Compensates for residual inductance, resistance, stray capacitance or residual conductance of test fixture. The variable ranges are approximately 1pF, 1μ °C, 100nH and 0.1Ω.
- TRIGGER (INT, REM/MAN). Selects triggering mode of measurement cycle. INT is internal triggering. REM/MAN is for remotely controlled triggering or for manual (pushbutton) triggering.
- RATE. Selects the repetition rate of measurement. Maximum rate is in full counter clockwise position.
- Trigger Button (Manual). For Manual triggering. When this button is pushed, measurement is held. When button is released, instrument is triggered.
- 15. REMOTE TRIGGER. Connector for external triggering fixture.
- 16. LINE (OFF/ON). AC Power Switch.
- 17. Ground. Instrument ground terminal.

- DC BIAS VTG (INT/OFF/EXT). Selects bias mode. INT is for internal bias. EXT is for external bias. OFF is for no bias.
- DC Bias Input (EXTERNAL). Input connector for external bias voltage. Maximum input ±200Vdc.
- 20. DC Bias MONITOR. Connector for DC bias voltage monitoring. If necessary to monitor voltage across DUT (device under test) use a DVM, float input and connect DVM ground to 4271A ground terminal.
- 21. AC Power Input. AC receptacle. Accepts female connector. Voltages of 100, 120, 220, or 240V (±10%) may be used (set voltage selector card to correct position).
- DC BIAS CONTROL. Input Connector (J10). Input connector for internal bias (OPT 001) control. (For details see paragraph 3-55).
- 23. DATA INPUT/OUTPUT Connector (J11). Output connector for option 003, 004, 005. (For details see paragraph 3-61).
- 24. C/L DATA OUTPUT Connector (J12). Output connector for option 002. (For details see paragraph 3-60).

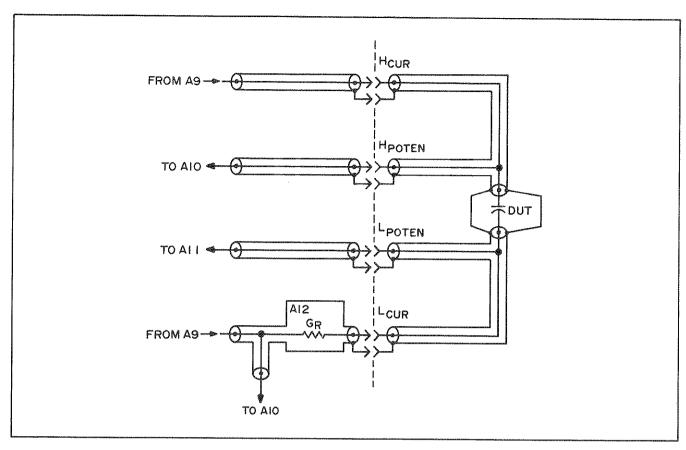


Figure 3-2. Four-Terminal Pair Configuration (C Measurements).

Table 3-1. C and G Displays Near 05 After Zero Adjustment.

FUNCTION	RANGE	LEFT SIDE DISPLAY	RIGHT SIDE DISPLAY	ANNUNCIATOR
	AUTO	0 ± 1 (1) count pF		
	1	0 ± 1 (1) count pF		
C - D	2	0 ± 2 (3) counts pF	.0001 D	D→ G, R
	3	0 ± 2 (3) counts pF		
	4	0 ± 3 (3) counts nF		
DOTTO THE REPORT OF THE PROPERTY OF THE PROPER	AUTO	0 ± 1 (1) count pF	0 ± 1 (1) count μυ	
	1	0 ± 1 (1) count pF	0 ± 1 (1) count $\mu\mho$	
C - G	2	0 ± 2 (3) counts pF	0 ± 3 (4) counts m ប	
	3	0 ± 2 (3) counts pF	0 ± 3 (4) counts m ប	
	4	0 ± 3 (3) counts nF	0 ± 4 (4) counts m	

() is at LOW level.

Note

Zero adjustment is done in like manner for other test fixtures. The stray admittance $G_0 + j\omega C_0$ and residual impedance $R_0 + j\omega L_0$ exist on the actual measuring terminals besides the impedance or admittance of DUT. The stray Co produces an error in low capacitance and high inductance measurements and also in residual L_0 on low inductance and high capacitance measurements. C and G OFFSET ADJUST compensates for the current flow through Co and Go. L and R OFFSET ADJUST compensates for the voltage drop generated by Lo and Ro. Offset adjustment must be performed independently at both "Low" test level and at "High" test levels. After adjustment, measurement tolerances are satisfied.

- 3-15. Zero Admittance.
- 3-16. Set controls and functions as follows:

FUNCTION	
TEST SIG LEVEL .	HIGH (LOW)
TRIGGER	INT
	fully ccw
	OFF
	Do not connect any-
	thing to test fixture.

Adjust C or G OFFSET ADJUST controls (front panel) for C (capacitance) and G (conductance) while observing the counter display. Set for zero display.

Note

The adjustment potentiometer for C is 10-turn control and the potentiometer for G is a 3/4-turn control.

Displays near 00 after completing the zero adjustment for C and G are shown in Table 3-1. A zero adjustments when TEST SIG LEVEL is set to LOW level should be done in like manner.

- 3-17. Zero Impedance.
- 3-18. To adjust instrument for zero impedance, set controls and functions as follows:

FUNCTIONL-R
RANGE 1
TEST SIG LEVEL HIGH (LOW)
TRIGGER INT
RATE Fully ccw
DC BIAS VTG OFF
Unknown Short test fixture.

The zero adjustment for L (Inductance) and R (Resistance) is done while observing counter displays.

Note

The potentiometer for L is a 10-turn pot. The potentiometer for R is a 3/4 turn control.

The displays near 0Ω after completing zero adjustments are shown in Table 3-2. A zero adjustment when TEST SIG LEVEL is set to LOW level should be done in like manner. The variable ranges of zero

Table 3-2. L and R Displays Near 0Ω After Zero Adjustment.

FUNCTION	RANGE	LEFT SIDE DISPLAY	RIGHT SIDE DISPLAY	ANNUNCIATOR
	AUTO	0 ± 1 (1) count nH		
	1	0 ± 1 (1) count nH		
L - D	2	0 ± 4 (6) count μH	.0001 D	D → G, R
	3	0 ± 4 (6) count μH		
	4	0 ± 4 (6) count μ H		
	AUTO	0 ± 1 (1) count nH	0 ± 1 (1) count Ω	
	1	0 ± 1 (1) count nH	0 ± 1 (1) count Ω	****
L - R	2	0 ± 4 (6) count μ H	0 ± 3 (4) count Ω	
	3	0 ± 4 (6) count μ H	0 ± 3 (4) count Ω	
	4	0 ± 4 (6) count μ H	0 ± 3 (4) count k Ω	

RANGE L G 1 -. 100 \sim . 100 Ω $-20.0 \sim 10.0 \, \mathrm{nH}$ -. 200 \sim . 200 pF $-.30 \sim .20 \mu v$ 2 -.030 ~ .010 nH $-.10 \sim .10 \Omega$ $-1.00 \sim .20 \text{ pF}$ -.3 ~ .2 μυ 3 <> 0 ≈ 0 $-1.0 \sim .2$ рF ~0 4 ≈ 0 20 ~≥0 ≈ 0

Table 3-3. Variable ranges of zero adjustment.

adjustments for C, G, L and R are shown in Table 3-3.

3-19. DISPLAY.

3-20. Counter displays show value of sample when being measured (after zero adjustments). Simultaneously the decimal point, unit and polarity (only minus is displayed) may be read. The counter is full 4-digit plus overrange of 100%. The display may read from approximately -100 to the maximum value When display is less than approximately -100, the display instantaneously changes to -200 (and never becomes less than -200). When "UNBAL" lamp is lit, the measured value displayed on front panel is ambiguous as a measured value. "OUT OF RANGE" lamp is lit, both C/L & G/R/D displays have no meaning. The "D→G, R" lamp lights when measured value of C or L becomes less than about +1000 (FUNCTION set to C-D or L-D). If "D - G, R" is lit, measured value of D has no meaning. C/L display becomes measured value when C/L and G/R displays do not show 0000. When "D → G, R" is lit, FUNCTION should be changed to C-G or L-R. Normally 0 display to left of decimal point has no meaning and is blanked. However, when OPT 005 is installed or A28S1 switch is set to unblank position, blanking is not used. When C/L display shows a negative value of more than -100 [e.g. -48pF (or -48 μ H)] it means DUT is inductive (or capacitive).

3-21. ACCURACY.

3-22. The measuring accuracy of the Model 4271A 1MHz Digital LCR Meter is given in Table 1-1, Specifications. Measuring accuracy varies with value of unknown sample being measured and level of test signal (HIGH or LOW). Moreover, accuracy of capacitance changes with value of conductance of measured sample, accuracy of inductance with value of resistance, accuracy of conductance with value of capacitance and accuracy of resistance with the value of inductance, respectively. Each accuracy has a digital error of ± 1 count. Deriviation equation and accuracy diagram is given and shown in Figure 3-3. Accuracy does not vary when dc bias voltage is applied or a dc bias current applied to unknown sample.

3-23. ANNUNCIATORS.

3-24. "UNBAL" Lamp.

3-25. "UNBAL" lamp is an indicator which shows that bridge is unbalanced. This lamp is turned on and off when the FUNCTION and RANGE are not appropriate for sample being measured, or if value of the sample varies during balancing operation, or if

bridge section of 4271A is faulty and in certain other situations. "UNBAL" lamp is turned on and off at same rate as measuring rate lamp. When "UNBAL" lamp is turning on and off, the counter display has no meaning as a measured value.

3-26. "OUT OF RANGE" Lamp.

3-27. "OUT OF RANGE" lamp lights when the total of C/L or G/R/D display is beyond about 20,000 counts. If "OUT OF RANGE" lamp is lit, RANGE should be switched to higher range.

3-28. "D → G, R" Lamp.

3-29. "D \rightarrow G, R" lamp is turned on when count of C/L counter is less than 1000 (approximately) and FUNCTION is set to C-D or L-D. When "D \rightarrow G, R" lamp lights it means that FUNCTION C-D should be set to C-G and L-D to L-R.

3-30. OPERATIONAL CHECK.

3-31. An operational check of the Model 4271A may be done with its front panel controls as outlined and discussed in the following paragraphs.

3-32. Measuring Rate Lamp. The on-off period of lamp is generally determined by setting of RATE control, but its period is also slightly affected by FUNCTION setting and value of sample. The on-off period of the measuring rate lamp for RATE control midrange and extreme settings is as follows:

Table 3-4. Measuring Rate.

RATE setting	Period
Fully ccw.	Approximately .2 sec.
Centered.	Approximately 1 sec.
Fully cw.	Approximately 3 sec.

Note

On and off switching continues and is visible even if RATE is set to full ccw.

Turn "ON" time interval is approximately 100msec to 300msec and is slightly varied by FUNCTION setting and value of sample. When TRIGGER mode

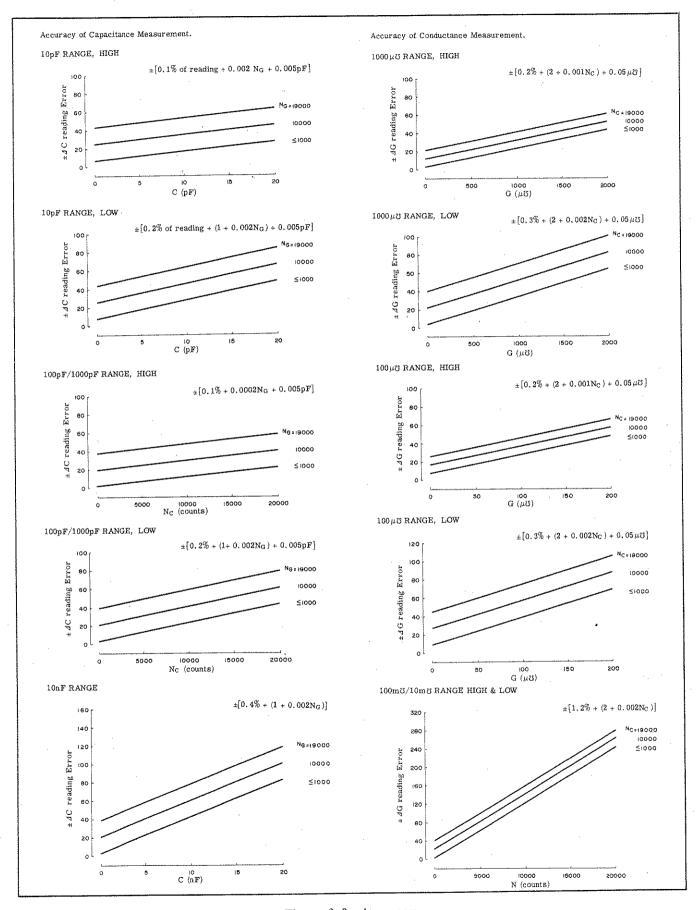


Figure 3-3. Accuracy.

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	w .			
		·		
				* ,

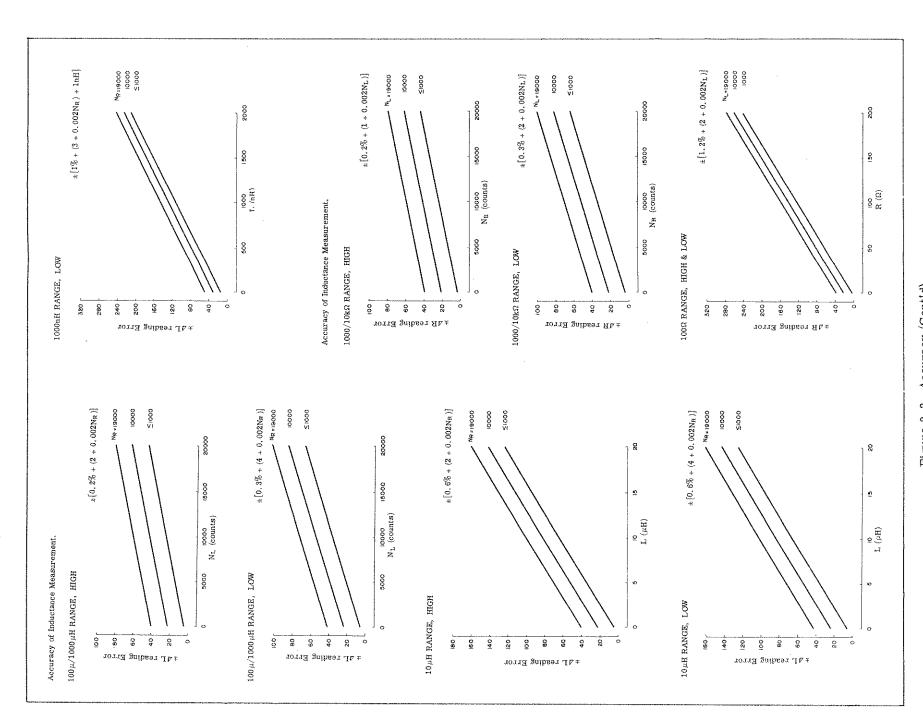


Figure 3-3. Accuracy (Cont'd).

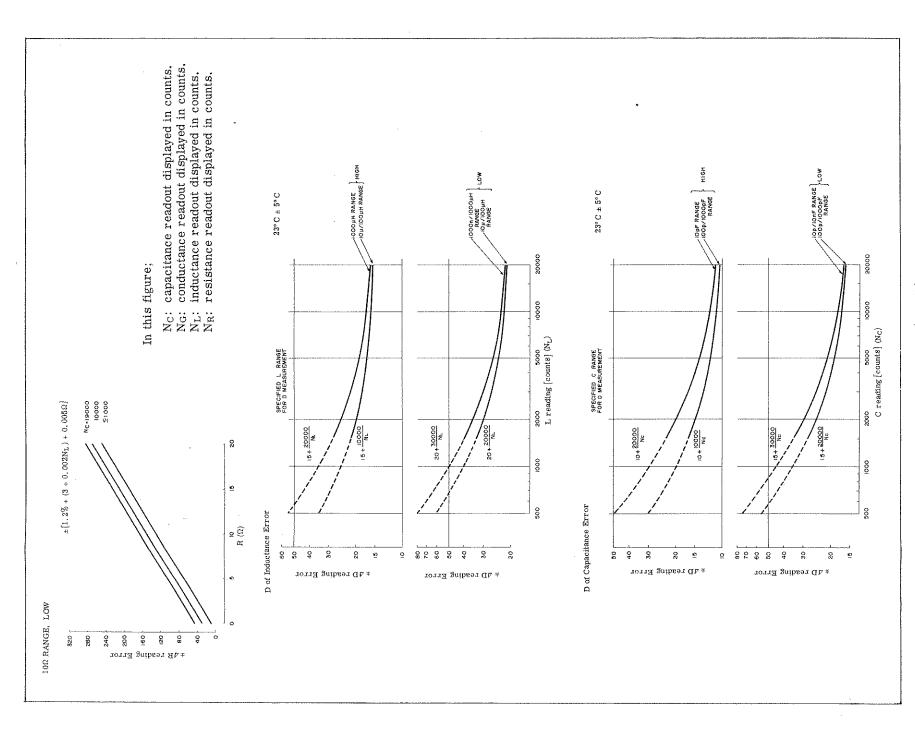


Figure 3-3. Accuracy (Cont'd).



Table 3-5. Decimal Points and Units.

FUNCTION	RANGE	LEFT SIDE DISPLAY	RIGHT SIDE DISPLAY			
1		00.000 pF				
	2	000.00 pF				
C - D	3	0000.0 pF	.0000 D			
	4	00.000 nF				
	1	00.000 pF	000.00 μσ			
C - G 2 3 4	2	000.00 pF	0000.0 μτ			
	3	0000.0 pF	00.000 m			
	4	00.000 nF	000.00 m t			
	1	0000.0 nH	00.000 Ω			
	2	00.000 $\mu\mathrm{H}$	000.00 Ω			
L - R	3	000. 00 $\mu\mathrm{H}$	0000.0 Ω			
	4	0000.0 μ H	00.000 kΩ			

switch is set to REM/MAN position, measuring rate lamp is turned on (once only) when manual trigger button is depressed and released. Measured value is then displayed and held. Unless manual trigger button is again depressed and released, the measuring rate lamp does not light and a measurement is not taken.

3-33. Decimal Point/Unit Display. The decimal points and units of display are checked by FUNCTION and RANGE settings as shown in Table 3-5. Other controls positions are arbitrary. No sample may be connected for this test.

3-34. Annunciators. The three annunciators: "OUT OF RANGE", "UNBAL" and "D→G, R" may be checked by turning them on which is done with these respective, control settings:

a. "OUT OF RANGE" lamp.

FUNCTION								L-R
RANGE								Any position.
Unknown								Onen

b. "UNBAL" lamp.

FUNCTION.						 						С	-G
RANGE													
Unknown						 					S	h	ort

'c. "D→G, R" lamp.

FUNCTIONL-D
RANGE Any position.
TEST SIG LEVEL HIGH or LOW
Unknown Short

Note

"UNBAL" lamp is turned on and off at the same rate as measuring rate lamp. Other annunciator lamps light continuously.

3-35. OFFSET ADJ. The OFFSET ADJ. potentiometers may be turned to determine whether their variable range is appropriate (test is independent of sign polarity). Here is how controls are operated to make test:

Note

C and L potentiometers are 10-turn devices; G and R potentiometers are 3/4-turn devices. Adjustments for (C and G) and (L and R) slightly interact with each other.

a. C and G variable range (compensating values) settings:

FUNCTION
RANGE
TEST SIG LEVEL HIGH or LOW
TRIGGER INT
RATE Fully ccw
DC BIAS VTG (on Rear Panel) OFF
Test Fixtures Attach 16022A Test
Fixtures.
Unknown Open

Compensating Range:

													1pF
G.,	 	 		 		•		٠	,	٠		٠.	$1 \mu \sigma$

		e.		
٠.				
	·			

Check variable range of C or G OFFSET by turning C and G potentiometers for minimum reading of C and G displays. For this test (only) variable range check is independent of polarity [minus (-) or plus (no sign)] of readings.

b. L and R OFFSET check settings:

FUNCTION L-R RANGE 1 TEST SIG LEVEL HIGH or LOW
TRIGGER INT
RATE Fully ccw
Test Fixtures Attach 16022A
Test Fixture.
Unknown Short
Compensating Range:
L 100nH
R 0.1Ω

Note

Check variable range of L or R OFF-SET by turning L and R offset potentiometers for minimum reading of L and R displays. The L offset potentiometer is a 10-turn control.

3-36. FUNCTIONS.

3-37. The Model 4271A has five measuring FUNCTIONS: C-G, C-D, L-R, L-D and REMOTE. In C-G or C-D, the 4271A measures an unknown as a capacitance (C) with parallel conductance, and displays the conductance (G) or dissipation factor (D). In L-R or L-D, the instrument measures an unknown as an inductance (L) with series resistance and displays the resistance (R) or dissipation factor (D). Thus, the 4271A measures a sample regarding it as an equivalent circuit as shown in Figure 3-4(A).

FUNCTION	Measurement Method-Equivalent Circuits							
C-G C-D	G C ($D = \frac{G}{\omega C}$						
L-R L-D	R	$D = \frac{R}{\omega L}$						

Figure 3-4(A). Measurement Method-Equivalent Circuits.

Function	Series Equivalent	Parallel Equivalent
C Measurement	CSR R	The 4271A measures this equivalent.
L Measurement	LSR R The 4271A measures this equivalent.	L _{PL}

Figure 3-4(B). Measured Equivalents of DUT (Device Under Test).

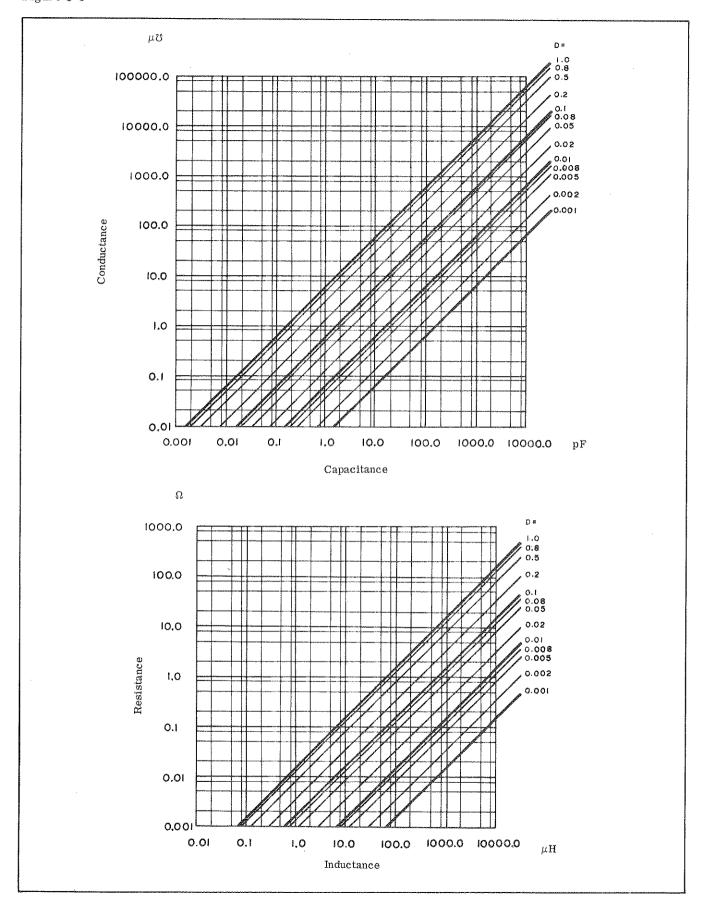


Figure 3-5. Dissipation Factor Conversion Chart.

3-38. D MEASUREMENT [Refer to Figure 3-4 (B)].

3-39. Capacitor or inductor loss is measured as dissipation factor (D). The measurable part of the dissipation factor is 0.0000 to 1.6000. Dissipation factor (D) measuring methods of the 4271A are explained in detail in Section IV Theory. For C measurement, dissipation factor ($D_{\rm C}$) is presented in the following equation:

$$D_{\rm C} = \frac{G}{\omega C_{\rm PL}} \tag{3-1}$$

The value of capacitance ($C_{\rm PL}$) as measured by the 4271A differs from that of a series capacitance ($C_{\rm SR}$) equivalent circuit. The conversion equation is given below:

$$C_{SR} = (1 + D_C^2) \cdot C_{PL}$$
 (3-2)

The difference between $C_{\rm PL}$ and $C_{\rm SR}$ is large when Dc is greater than 0.1, but $C_{\rm SR}$ is within 1% of $C_{\rm PL}$ if Dc is 0.1 or less.

For L measurement, the dissipation factor (D_L) of a sample is measured regarding the sample as a series equivalent circuit. D_L is given as follows:

$$D_{L} = \frac{R}{\omega L_{SR}}$$
 (3-3)

Values of inductance, when measured as in a series equivalent circuit (4271A method), differ from that as measured in a parallel equivalent circuit. The conversion equation is as follows: (See Figure 3-5).

$$L_{PL} = (1 + D_L^2) \cdot L_{SR}$$
 (3-4)

The relation of eq. (3-4) is the same as that of eq. (3-2). If $C_{\rm SR}$, $C_{\rm PL}$ and $D_{\rm C}$ are substituted for $L_{\rm PL}$, $L_{\rm SR}$ and $D_{\rm C}$ respectively, eq. (3-4) can be obtained from eq. (3-1).

The dissipation factor (D), when measured by C-G or L-R FUNCTION, can be calculated by equations (3-1) or (3-3). Figure 3-5 is a conversion diagram between G or R and D.

3-40. RANGING.

3-41. MANUAL Ranging.

3-42. The Model 4271A employs three methods of ranging: (1) MANUAL, (2) AUTO, and (3) REMOTE. In this paragraph MANUAL ranging is described. In any range mode, if counted number by C/L or G/R counter exceeds about 20,000, "OUT OF RANGE" lamp is turned on. At this point, range must be shifted up (if on lower range) or measurement is beyond design range of instrument and may not be performed. The MANUAL range has four positions: 1, 2, 3 and 4. A

Table 3-6. Measuring Span.

RANGE	C - G	C - D	RANGE RESISTOR
1	0.000 - 19.000 pF 0.00 - 190.00 μυ	0.000 - 19.000 pF 0.0000 - 1.6000	10 kΩ
2	0.00 - 190.00 pF 0.0 - 1900.0 μ ប	0.00 - 190.00 pF 0.0000 - 1.6000	1 kΩ
3	0.0 - 1900.0 pF 0.000 - 19.000 m ប	0.0 - 1900.0 pF 0.0000 - 1.6000	100 Ω
4	0.000 - 19.000 nF 0.00 - 190.00 m v	0.000 - 19.000 nF 0.00 - 1.6000	10 Ω

RANGE	L - R	L - D	RANGE RESISTOR
1	0.0 - 1900.0 nH 0.000 - 19.000 Ω	0.0 - 1900.0 nH 0.000 - 1.6000	10 Ω
2	0.000 - 19.000 μH 0.00 - 190.00 Ω	0.000 - 19.000 μH 0.000 - 1.6000	100 Ω
3	0.00 - 190.00 μH 0.0 - 1900.0 Ω	0.00 - 190.00 μH 0.0000 - 1.6000	1 kΩ
4	0.0 - 1900.0 μH 0.000 - 19.000 kΩ	0.0 - 1900.0 μH 0.0000 - 1.6000	10 kΩ

manual range is selected by positioning slide switch on front panel to match value of unknown. Table 3-6 shows measuring span for each RANGE and FUNCTION and selected range resistor.

3-43. AUTO and REMOTE Ranging.

- a. Auto ranging. In AUTO mode setting of RANGE switch, a range appropriate for measuring the value of sample is automatically selected by an Auto Range Control Circuit in the 4271A. Range selected by Auto ranging is determined by larger part of imaginary part (C/L) and the real part (G/L) of measured sample. For example, is in C-G FUNCTION capacitance displayed is 100, 00pF and conductance is 1700, $0\mu\sigma$, selected range is determined by value of G (17000counts). Auto ranging control is accomplished as follows: If counted number of both C/L and G/R counters is between 1600 and 18000 counts, an optimum range has been selected and actual range will be determined by the higher count. If counted number is greater than 18000 (either C/L or G/R counter) the range is shifted up (for example, from 3 to 4). And, in like manner, if less than 1600, range is shifted down (for example, from 3 to 2).
- Remote ranging. REMOTE ranging is used for external range control by (for example) OPT.
 005 Calculator Interface. The RANGE switch on front panel is set to REM position.

3-44. MEASURING RATE.

3-45. Measuring rate is decided by setting of RATE control. Clockwise rotation results in a lower rate and counterclockwise rotation produces a higher rate. The RATE control is functional only when TRIGGER mode is set to INT position. If TRIGGER mode is set to REM/MAN position, internal rate setting by

RATE control is disabled. When TRIGGER is set to REM/MAN, a measurement can be taken and measured value displayed by depressing and releasing Manual Trigger button. If an external trigger source is connected to REMOTE TRIGGER terminal, measurements at an arbitrary measuring rate can be performed

Note

When 4271A is externally triggered with pulse generator, period of pulses should be set to longer than measuring time. Figure 3-6 shows that measuring time of 4271A is time interval between generation of reset pulse and end pulse.

3-46. TEST FIXTURES.

- 3-47. Four (4) kinds of test fixtures are available for use with the Model 4271A1MHz Digital LCR Meter. The following paragraphs explain the purpose of each fixture and give a brief description.
- 3-48. Model 16021A Test Fixture. The Model 16021A Test Fixture is illustrated in Figure 1-2. The purpose of this fixture is to calibrate the Model 4271A with a standard capacitor or a standard resistor. Full procedure is outlined in Section V. A type GR 900-WN short Circuit Termination (0Ω) is used when making offset adjustment for L and R. The fixture includes cables for L_{CUR} , L_{POTEN} , H_{POTEN} and H_{CUR} unknown connections to panel connectors. The unknown is connected to fixture through a type GR-900 $^{\odot}$ Connector. A remote triggering switch at fixture is connected through a cable to REMOTE TRIGGER BNC on front panel.
- (3-49, Model 16022A Test Fixture. The Model 16022A Test Fixture is illustrated in Figure 1-2. This is

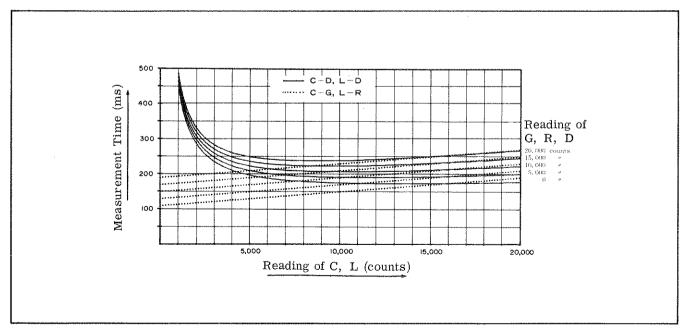


Figure 3-6. Measuring Time.

a general purpose fixture for connecting L, C or R unknowns to Model 4271A. The fixture is supplied with inserts for both vertical and axial lead connections. Second set of inserts is stored in fixture housing. Turn fixture over and open door for access. The insert terminals consist of the required 4-terminal pair connections and a shield plate. Cabling includes connections to L_{CUR}, L_{POTEN}, H_{POTEN} and H_{CUR} panel connectors. A remote triggering switch bar is connected thru a fifth cable to REMOTE TRIGGER on front panel. A C-G offset adjustment can be made without a DUT (device under test) inserted into terminals. However, when making L-R offset adjustment, insert a small thick copper plate between the terminals (short). The copper plate still will have some very small inductance and resistance which will produce a slight residual error but this is usually negligible.

3-50. Model 16023A DC Bias Controller. See Figure 1-2. The Model 16023A DC Bias Controller is used to control internal bias provided by the instrument when the instrument is equipped with option 001 (Internal DC Bias). The fixture has 3 rotary switches to control bias from 0.0V to 39.9V in 0.1V steps. A remote triggering bar is connected thru the multicable connector to furnish remote triggering (panel switch is set to REM/MAN).

Note

Trigger should always be set to REM/MAN when using 16023A DC BIAS controller. It is possible, if INT trigger is used, that an incorrect voltage may be supplied when BIAS control rotary switches are operated.

3-51. Test Leads.

- a. Model 16032A Test Leads are used for connecting 4271A to four-terminal device or usermanufactured test fixture which has BNC connectors. An accessory metal terminal shield/conductor grounding bracket is furnished with these leads. Operational checks of 4271A can be performed by shorting center conductors of H_{CUR} and H_{POTEN} terminals and of L_{POTEN} and L_{POTEN} terminals, respectively, for FUNCTION C-G. Shorting center conductors of 4 terminals to each other permits operational check of L-R FUNCTION.
- b. Model 16033A Test Leads are used for connecting 4271A unknown terminals to sample to be measured. As small coaxial connectors and slender and flexible coaxial cables are used in the construction of these leads, connecting to device to be measured can easily be done. These leads include an accessory metal terminal shield/connector grounding bracket by which outer conductors of cables are shorted to each other. Operational checks can be performed the same as with Model 16032A.

3-52. DC BIAS.

3-53. Capacitance measurements with DC bias can be made when a bias voltage is supplied in either of two ways:

- a. External bias.
- b. Internal bias (option 001).

Note

A bias current option for inductance measurement is not offered.

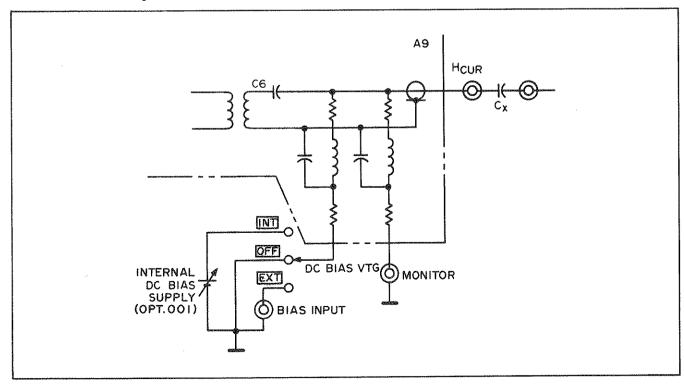


Figure 3-7. Bias Circuit.

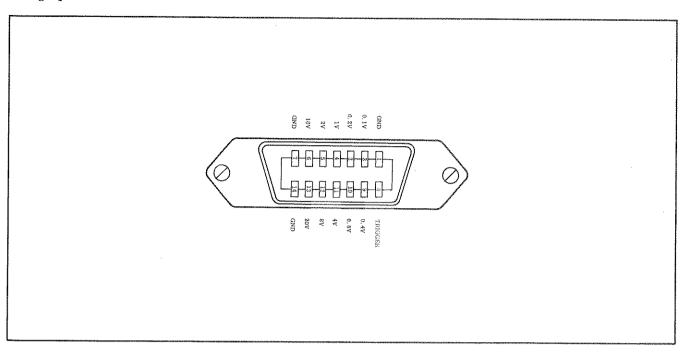


Figure 3-8. Bias Voltage Control Jack.

If external bias is furnished, the standard 4271A can be used to make capacitance measurements with bias. If an internal bias voltage is desired, the instrument should be equipped with option 001 (Internal DC Bias). The following two paragraphs discuss capacitance measurements with external and with internal bias, respectively.

3-54. External DC Bias.

a. Connect dc voltage source supplying external bias voltage to EXT INPUT (rear panel).

Note

A capacitor should be connected across dc bias voltage supply to lower its impedance at 1MHz.

- b. Set DC BIAS VOLTAGE switch to EXT.
- If monitoring is required for precise setting of dc bias, connect dc voltmeter to MONITOR (rear panel).
- d. Supply dc bias voltage and measure the capacitance.

Note 1

Maximum permissible EXT input dc bias is ± 200 V.

Note 2

Set the DC BIAS VOLTAGE to OFF except when supplying dc bias voltage. When DC BIAS VOLTAGE is set to OFF, voltage at H_{CUR} terminal is zero.

Note 3

A basic presumption of DC BIAS circuit design (refer to Figure 3-7) is that no dc bias current is drawn by DUT (Device Under Test). If even a very small current is drawn by DUT, actual voltage across DUT and supplied voltage become somewhat different, actual voltage is that measured at MONITOR terminal (series resistance of bias circuit is 480Ω).

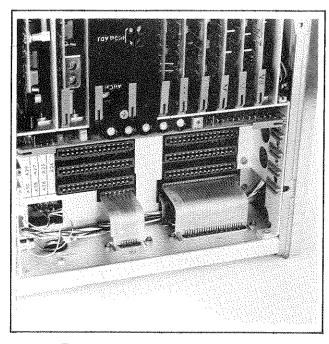


Figure 3-9 Connection Board.

3-55(A). Internal DC BIAS (option 001). Internal DC BIAS is possible by equipping 4271A with option 001 which adds A21 board to instrument. The main applications feature gained by dc bias option is the additional capability of instrument to measure characteristics of variable capacitance diodes. A user designed or HP Model 16023A DC Bias Controller is required when making dc bias measurements (see paragraph 3-50). Bias voltage is applied to capacitor being measured. When bias is switched at the 16023A, internal bias controls apply voltage at new setting to next measurement. If bias voltage is changed during a measurement, application of the bias is delayed until beginning of next measurement cycle.

3-55(B). Installation and Use of Internal Bias.

a. Installation.

- 1. Remove top cover from 4271A.
- Connect connector jack with connection board to rear panel of 4271A (See Figure 3-9).
- 3. Plug A21 board into A21 female receptacle (near left rear).

Note

Optional board A21 must be plugged in place of board number noted on chassis.

- 4. Normally, adjustments are not requied but when bias voltage set is out of specifications, do adjustments according to paragraph 5-37.
- 5. Replace cover.

b. Use.

 Connect a bias controller such as Model 16023A or equivalent user designed controller to DC BIAS CONTROL on rear panel.

Note

Refer to Figure 3-8 for Model 16023A Connector details. All data (including trigger signal) through control connector are transfered to 4271A in ground true mode. See also paragraph 3-50 for other 16023A information.

Note

16023A can not be used with A22 board (OPT 005 Calculator Interface).

- Set DC BIAS VTG switch (on rear panel) to INT.
- 3. Set TRIGGER switch to REM/MAN. In REM/MAN initiation of a measurement cycle is triggered either from an external signal

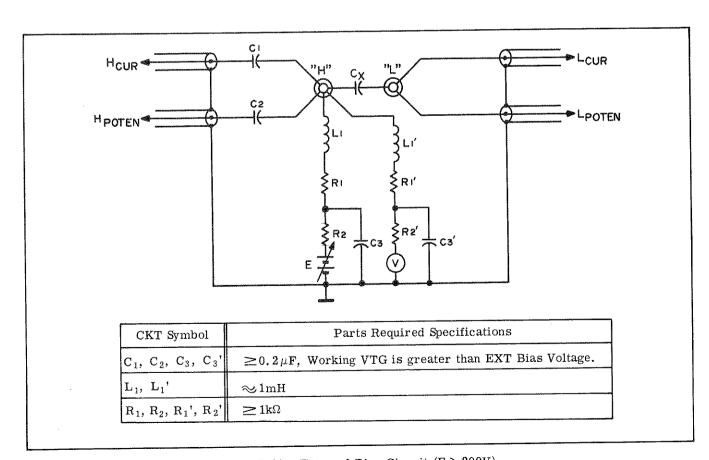


Figure 3-10. External Bias Circuit ($E \ge 200V$).

or by pushing trigger button (manually) Display is held between triggers.

c. Calculator Interface.

 Option 001 (DC Bias) can be combined with Option 005 Calculator Interface Option. A bias controller such as Model 16023A is not needed as control signals are fed to 4271A from calculator.

3-56. How to supply more than 200Vdc Bias.

- a. External dc bias applied to the DC BIAS CONTROL connector on the rear panel is limited to ±200 volts.
- b. To use bias voltages greater than 200 volts an external circuit is used. Figure 3-10 shows such a recommended circuit. The bias voltage is limited to maximum working voltages of the unknown capacitor $C_{\rm X}$ and the blocking capacitors $C_{\rm 1}$ and $C_{\rm 2}$.

CAUTION

DC BIAS VTG SWITCH ON REAR PANEL MUST BE IN OFF POSITION.

c. To monitor the voltage another filter section consisting of L_1 ', R_1 ', R_2 ' and C_3 ' is added as shown in Figure 3-10 for connection voltmeter.

CAUTION

USE EXTREME CAUTION WHEN WORK-ING WITH CHARGED CAPACITORS, FLOATING OR UNGROUNDED CIR-CUITRY.

3-57. Method of applying a dc bias current to an inductor.

- a. The bias current superposed in an inductor being measured with the 4271A must not flow into the instrument.
- Figure 3-11 shows a recommended circuit for inductor current biasing, measuring requirements and suggested procedures.

CAUTION

DC BIAS VTG SWITCH ON REAR PANEL MUST BE IN OFF POSITION.

3-58. DATA RECORDING.

3-59. When a Model 4271A is equipped with option 002 (C/L BCD OUTPUT), option 003 (G/R/D BCD OUTPUT), option 004 (Parameter Serial BCD OUTPUT), all data (depending upon options selected) measured by the instrument becomes available at rear panel connectors for recording. The following

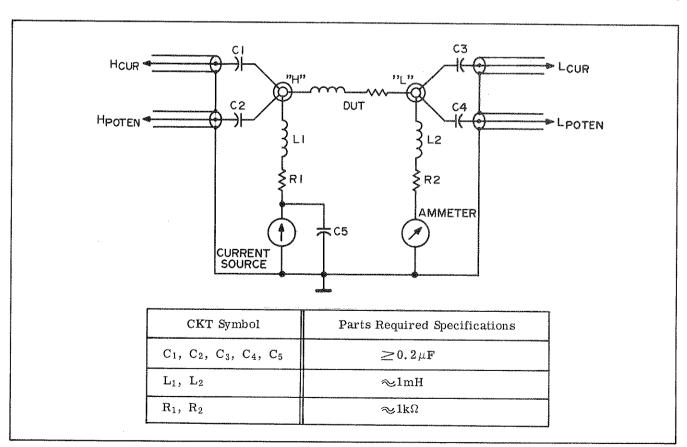
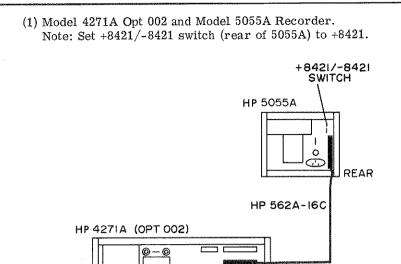
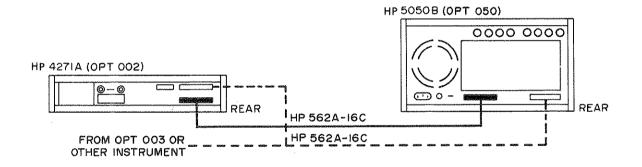


Figure 3-11. DC Current Bias Circuit for Inductors.



(2) Model 4271A Opt 002 (and 003) and Model 5050B Opt 050 Recorder.

REAR



(3) Model 4271A Opt 002 and Model 5050B Opt 051.

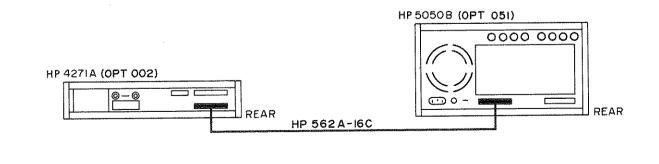


Figure 3-12. C/L BCD OUTPUT (OPT 002).

Table 3-7. Data Format (OPT 002).

	,,,,	Column	L.	A STATE OF THE STA
8	7	4, 3, 2, 1		
Unit	Magnification of Data	Warning Signal	Data or Symbol	C/L Data

Unit (column 8)

4271A	Co	onnecto	Printed				
Display	15	16	40	41	letter		
pF	Н	L	L	L	1		
nF	Н	H	L	L	3		
nН	Н	L	H	L	5		
$\mu { m H}$	Н	Н	H	L	7		

Warning Signal (Column 6)

4271A	Co	nnecto	Printed		
Display	11	12	36	37	letter
''OUT OF RANGE'' or "UNBAL''	L	L	Н	Н	V
Blank	н	Н	Н	Н	*

Magnification of Data (Column 7)

4271A Display		Connec	Printed		
	13	14	38	39	letter
$0000.0(10^{-1})$	Н	L	L	L	1
000.00 (10 ⁻²)	L	н	L	L	2
00.000 (10 ⁻³)	H	Н	L	L	3

Data or Symbol (Column 5)

4271A		Conn	Printed		
Display	9	10	34	35	letter
1	H	L	L	L	1
-	Н	Н	L	H	na.
Blank	Н	Н	H	Н	*

Data (Column 1 - 4)

HP 4271A		1	Printed		
Display	1	2	4	8	letter
0	L	L	L	L	0
1	H	L	L	L	1
2	L	Н	L	L	2
3	H	H	L	L	3
4	L	L	H	L	4
5	H	L	Н	L	5
6	L	H	H	L	6
7	Н	H	н	L	7
8	L	L	L	H	8
9	H	L	L	H	9

paragraphs provide more detailed information on recording options. Description and theory for each option is presented in Section VII.

3-60. C/L BCD OUTPUT (Option 002).

- a. Installation.
 - 1. Remove top cover from 4271A.
 - Connect connector jack with connection board to rear panel of 4271A (See Figure 3-8).
 - Plug A23 Board into A23 female receptacle (near left rear).

Note

A23 board must be plugged in place of board number noted on chassis.

- 4. Replace cover.
- 5. No adjustments are required.
- b. HP recorders Model 5055A and Model 5050B-OPT050, OPT051 may be connected to a Model 4271A equipped with option 002. All measured data can be recorded including data taken under biased conditions (except recording of the bias voltage itself).
- c. Refer to Figure 3-12 for typical recording connection configurations. As shown in (1) and (3) of the figure, recording is limited to that supplied by option 002 of the 4271A. In (2), option 003 can be added to 4271A to record additional data. Then the 5050B OPT. 050 recorder can record the information carried from DATA

 ${\tt INPUT/OUTPUT}$ connector as well as that from C, L DATA OUTPUT connector.

- d. Data formats are given in Table 3-7.
- e. Pin connections for option 002 and recorder are shown in Figure 3-13.
- f. Figure 3-14 is a timing diagram for option 002 and recorder (if necessary, also refer to Section VII paragraph 7-8).

3-61. G/R/D BCD OUTPUT (OPT 003).

3-62. Refer to Figure 3-15.

- a. Installation.
 - 1. Remove top cover from 4271A.
 - 2. Connect connector jack with connection board to rear panel of 4271A (see Figure 3-9).
 - Plug A24 board into A24 female receptacle (near left rear).

Note

A24 board must be plugged in place of board number noted on chassis.

- 4. Replace cover.
- 5. No adjustments are required.
- b. HP recorder Model 5055A, 5050B OPT 051 or 5050B OPT 050 may be used to record data from a 4271A equipped with OPT 003. Data measured with bias voltage can also be recorded (except for the bias voltage itself).

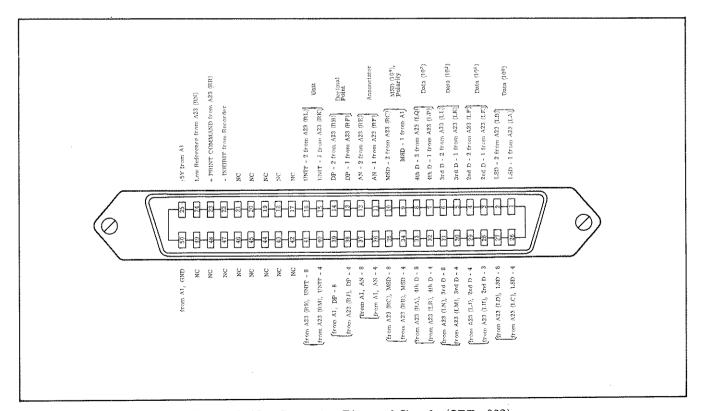


Figure 3-13. Connector Pins and Signals (OPT. 002).

Table 3-8. Data Format (OPT 003).

Column							
8	7	6	5	4, 3, 2, 1			
Unit	Magnification of Data	Warning Signal	Data or Symbol	G/R/D Data			

Unit (Column 8)

4271A		Conne	Printed		
Display	15	16	40	41	letter
D	L	L	L	L	0
μυ	L	H	L	L	2
mʊ	L	L	Н	L	4
Ω	L	H	H	L	6
kΩ	L	L	L	H	8

Warning Signal (Column 6)

4271A		Connec	Printed		
Display	11	12	36	37	letter
"OUT OF RANGE" or "UNBAL"	L	L	Н	Н	V
D → GR	Н	L	н	Н	A
Blank	H	H	Н	H	*

Magnification of Data (Coulmn 7)

	4271A		Connec	Printed		
	Display	11	12	36	37	letter
1	$00.0(10^{-1})$		L	L	L	1
	$0.00(10^{-2})$		Н	L	L	2
	.000 (10 ⁻³)	H	H	L	L	3
0.0)000 (10 ⁻⁴)	L	L	H	L	4

Data or Symbol (Column 5)

4271A		Connec	Printed		
Display	9	20	34	35	letter
1	H	Li	L	L	1
-	Н	н	L	Н	-
Blank	H	H	н	Н	*

Data (Column 1 - 4)

HP 4271A		I	Printed		
Display	1	2	4	8	letter
0	L	L	L	L	0
1	H	L	L	L	1,
2	L	Н	L	L	2
3	Н	H	L	L	3
4	L	L	H	L	4
5	Н	${f L}$	H	L	5
6	L	H	н	L	6
7	Н	H	H	L	7
8	L	L	${f L}$	H	8
9	Н	L	L	Н	9

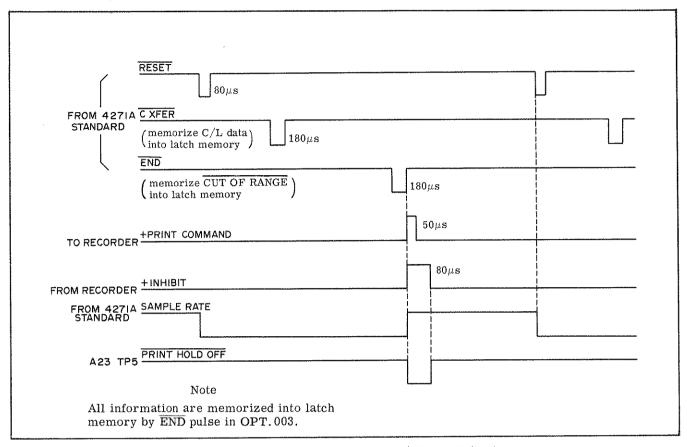


Figure 3-14. Timing Diagram (OPT. 002/003).

- c. In (2) of Figure 3-15, the 4271A is equipped with both options 002 and 003 and C/L data can be recorded by employing A1J2 of the 5050B OPT 050. See also Table 3-8 and Figure 3-16.
- d. The timing sequency for OPT 003 is the same as for OPT 002 except all data is stored in latch memory with END signal. See Figure 3-14.
- 3-63. Parameter Serial BCD OUTPUT (OPT 004).
 - a. Installation.
 - 1. Remove top cover from 4271A.
 - 2. Connect connector jack with connection board to rear panel of 4271A (see Figure 3-9).
 - 3. Set switch S₁ on A25 board to required position; C, G or C/G. In C position, C capacitance or inductance values measured by 4271A are transferred to recorder. G position allows transfer of only conductance, resistance or dissipation factor data and C/G position transfers both capacitance or inductance and loss component.
 - 4. Plug A25 and A26 boards into female recept-tacle (near left rear).

Note

A25 and A26 boards must be plugged in place of board number noted on chassis.

5. Replace cover.

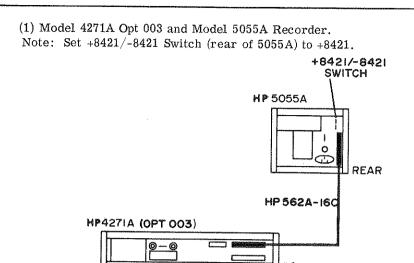
- 6. No adjustments are required.
- b. Option 004 is used to (alternately) transfer C/L data and G/R/D data in a parallel BCD code. Refer to Figure 3-17. Recorder Models 5055A, 5050B OPT 051 and 5050B OPT 050 may be used with a Model 4271A equipped with option 004. Data measured with bias voltage can also be recorded (except for bias voltage itself).
- The timing for option 004 is shown in Figure 3-19.
- d. See also Table 3-9 and Figure 3-18.

3-64. DATA PROCESSING (OPT 005).

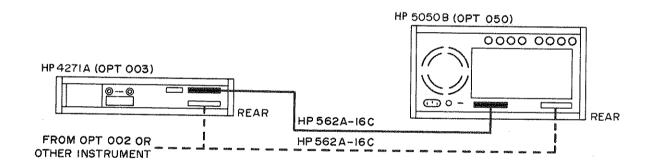
3-65. When a Model 4271A is equipped with opt 005 (Calculator Interface), its functions and measurement capabilities including proper processing of the measured data from the 4271A can be controlled by a calculator (for example, by an HP Model 9810A or Model 9820A Calculator).

3-66. Calculator Interconnections.

- a. Installation.
 - 1. Remove top cover from 4271A.
 - 2. Connect connector jack with connection board



(2) Model 4271A Opt 003 and Model 5050B Opt 050.



(3) Model 4271A Opt 003 and Model 5050B Opt 051.

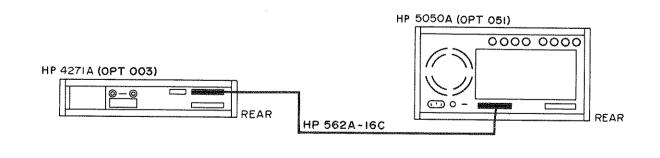


Figure 3-15. G/R BCD OUTPUT (OPT 003).

Table 3-9. Data Format (OPT 004).

		Column	1	41.54
8	7	6	5	4, 3, 2, 1
Unit	Magnification of Data	Warning Signal	Data or Symbol	Data

Unit (Column 8)

4271A	(Connec	Printed		
Display	15	16	40	41	letter
рF	L	Н	Н	H	1
nF	L	L	H	н	3
nH	L	H	L	H	5
$\mu \mathbf{H}$	L	L	L	Н	7
D	H	H	H	H	0
μ℧	Н	L	Н	Н	2
тÜ	H	н	L	Н	4
Ω	н	L	L	Н	6
$\mathbf{k}\Omega$	Н	H	H	L	8

Data or Symbol (Column 5)

4271A	(Connec	Printed		
Display	9	10	34	35	letter
1	L	H	н	H	1
-	L	L	H	L	-
Blank	L	L	r	L	*

Magnification of Data (Column 7)

4271A	(Connec	Printed		
Display	13	14	38	39	letter
0000.0 (10 ⁻¹)	L	H	H	Н	1
000.00 (10 ⁻²)	H	L	H	н	2
00.000 (10 ⁻³)	L	L	Н	н	3
0,0000 (10 ⁻⁴)	H	H	L	Н	4

Data (Column 1 - 4)

4271A		В	CD		Printed
Display	1	2	4	8	letter
0	Н	н	н	Н	0
1	L	н	H	Н	1
2	Н	L	Н	Н	2
3	L	L	Н	Н	3
4	H	Н	L	H	4
5	L	Н	L	Н	5
6	H	L	L	н	6
7	L	L	L	Н	7
8	Н	Н	H	L	8
9	L	H	Н	L	9

Warning Signal (Column 6)

4271A	(Connec	Printed		
Display	11	12	36	37	letter
"OUT OF RANGE" or "UNBAL"	Н	Н	L	L	v
"D->G, R"	L	Н	L	L	A
Blank	L	L	L	L	*

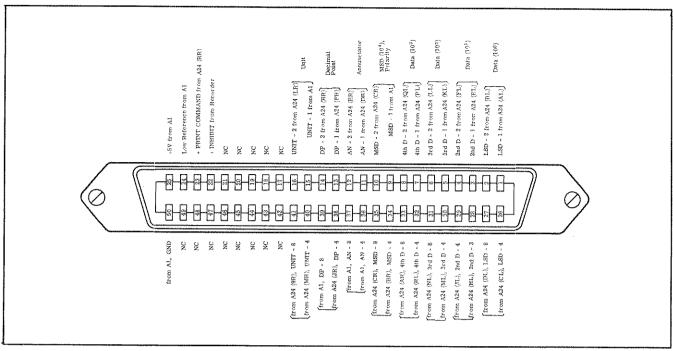


Figure 3-16. Connector Pins and Signals (OPT. 003).

Table 3-10. Pin Connections for 11202A Cables & Connector.

	Table 3-10. Pin Connection	mis for 11202A Caples & C	omector.
SIGNAL	PIN NO. OF CONNECTOR	Н	P 11202A
	HP P/N 1251-0086	PIN NO.	COLOR OF WIRE
DO - 0	1	16	BLK
DO - 1	2	15	BRN
DO - 2	26	14	RED
DO - 3	27	13	ORG
DO - 4	3	12	YEL
DO - 5	4	11	GRN
DO - 6	28	10	BLU
DO - 7	29	9	VIO
DI - 0	45	T	WHT/BLK
DI - 1	44	S	WHT/BRN
DI - 2	43	R	WHT/RED
DI - 3	42	P	WHT/ORG
CTL	24	Н	WHT/GRA
STP	40	J	WHT/BLK/RED
I/O	33	F	WHT/BLK/BRN
FLAG	49	С	GRA
GND	50	U	WHT/BLK/ORG
GND	50	v	WHT/BLK/YEL

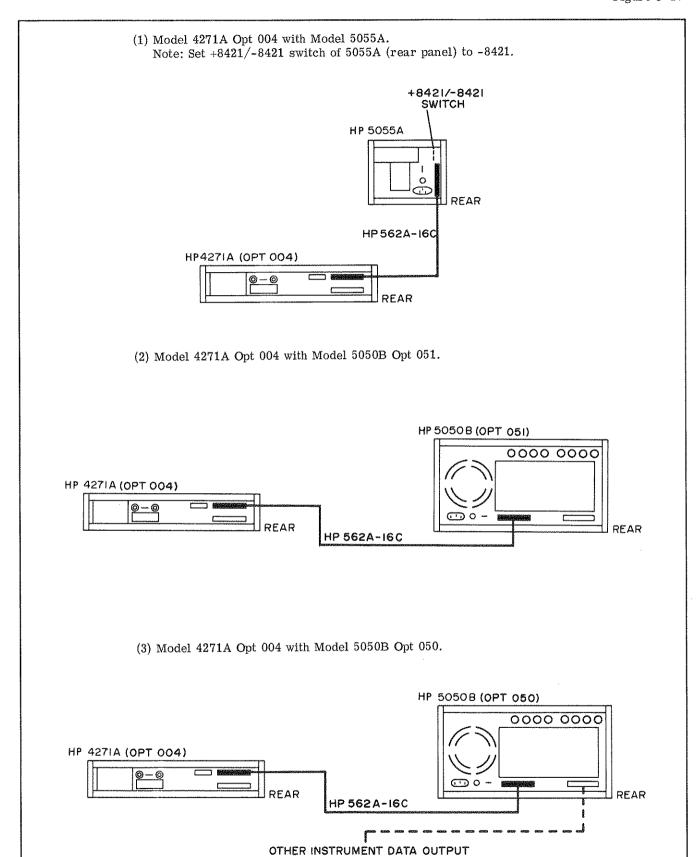


Figure 3-17. Rapameter Serial BCD OUTPUT (OPT 004).

to rear panel of 4271A (see Figure 3-9).

3. Plug A22, A27 and A28 boards into their female receptacles (near left rear).

Note

A22, A27 and A28 boards must be plugged in place of board numbers noted on chassis.

- 4. Replace top cover.
- 5. No adjustments are required.
- b. The instrumentation interconnection setup for measuring and processing with an instrument equipped with OPTION 005 is shown in Figure 3-20.

Note

Pin connections for interconnecting cable accessory Model 11202A and connector DATA INPUT/OUTPUT (male) are given in Table 3-10.

- c. Option 005 considerations:
 - If RANGE and FUNCTION are manually set and internal bias is not used, board A22 (Remote Control) can be deleted from option 005 group (A27 - Data Output Register and A28 - Data Output Control remain in 4271A).

- If measured values of sample with internal bias applied are desired, option 001 should be added to instrument (as well as option 005).
- 3. When FUNCTION and RANGE settings are to be fed to 4271A from calculator, the FUNCTION and RANGE switches are set to their REM (remote) positions.
- 4. Table 3-11 shows INPUT/OUTPUT format at calculator connector DATAINPUT/OUT-PUT for opt. 005.
- 5. Figure 3-21 shows pin numbers and signals.
- 6. Figure 3-22 provides a timing diagram.
- 7. Remote Control. Figure 3-22 shows how setting signals for RANGE, FUNCTION and DC BIAS VTG from the calculator to Model 4271A are sent by the CTL signal from calculator. A 4-bit RANGE signal is sent to 4271A in the time interval between receipt of CTL at option 005 and returning FLG to calculator. A 2-bit FUNCTION signal, DC BIAS VTG signal, CR (carriage return) and LF (line feed) signals are also sent to the 4271A.
- 8. Data transfer. Figure 3-22 Data transfer shows how the SP (shift pulse) signal generated by $\overline{\text{CTL}}$ signals enables transfer of 4271A data in serial form to calculator.

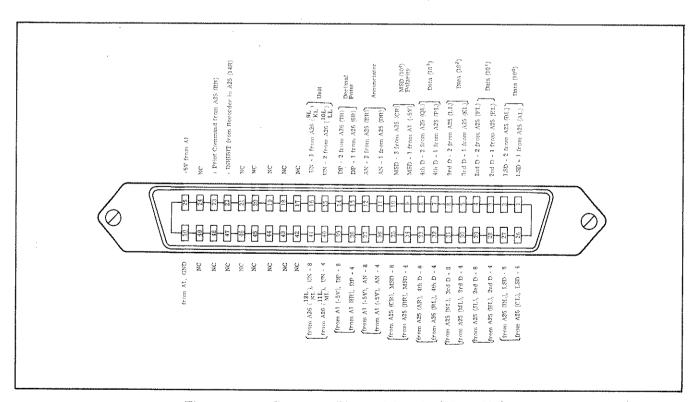


Figure 3-18. Connector Pins and Signals (OPT. 004).

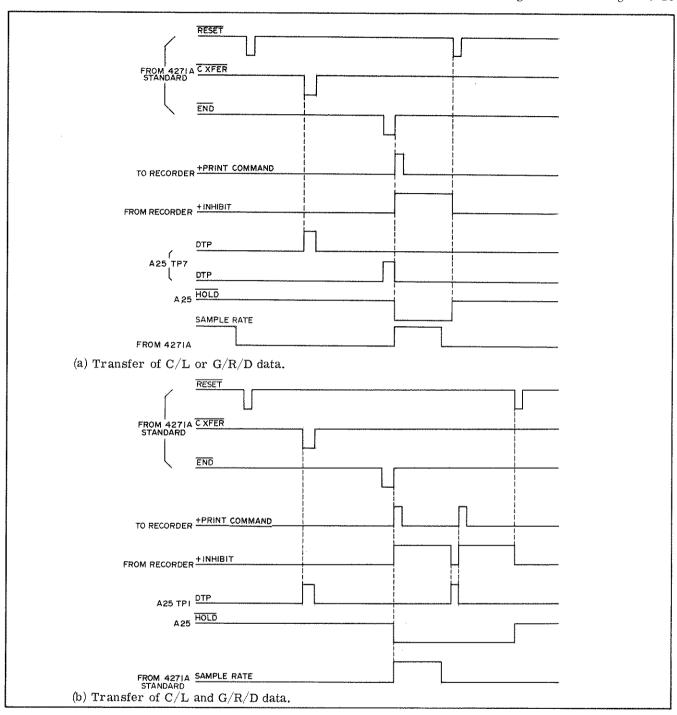


Figure 3-19. Timing Diagram: OPT 004.

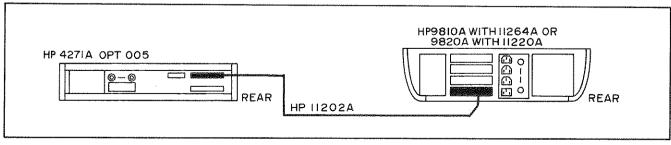


Figure 3-20. Calculator Interface: OPT 005.

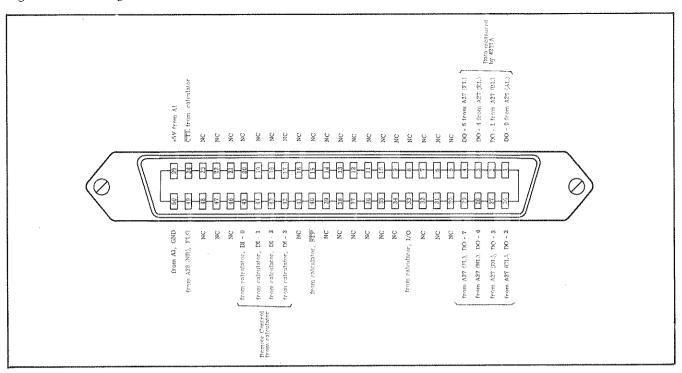


Figure 3-21. Connector Pins and Signals OPT 005.

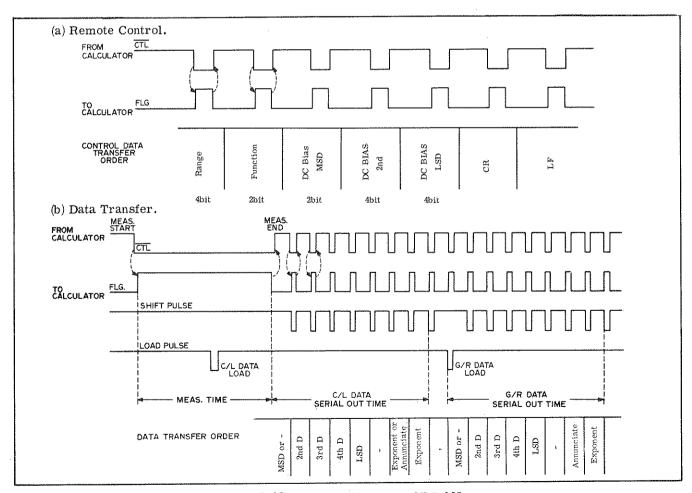


Figure 3-22. Timing Diagram: OPT 005.

Table 3-11. Input/Output Format for OPT 005.

(a) Output Format.

Connector Pin 4271A 29 28 Display 27 3 1 Н L H L Η L L H H H H H L \mathbf{L} 0 H H H Н H H L \mathbf{L} 1 Η L 2 H Н L \mathbf{L} H H H \mathbf{L} L L H H 3 L L H H H Η H L 4 H H L L H H H 5 \mathbf{L} H L L H H L \mathbf{L} H 6 H \mathbf{L} L \mathbf{L} H Η \mathbf{L} H L 7 \mathbf{L} \mathbf{L} Η Η L L L 8 Η H H L H H L 9 Η H \mathbf{L} L H \mathbf{L} H Η H Н \mathbf{L} L \mathbf{L} H H H L L \mathbf{L} L

(b) Input Format.

10=11	(Connec	tor Pir	ì	
42'(1A	4271A Setting		43	44	45
	AUTO	H	Н	Н	H
	1	\mathbf{L}	Н	Н	H
RANGE	2	H	L	н	H
	3	L	L	H	H
	4	42 43 44 O H H H L H H H L H	H		
	C - D	AUTO H H H H 1 L H H 2 H L H 3 L L H 4 H H L - D H H - G L H - R H L - D L L 0 H H H 1 L H H 2 H L H 3 L L H 4 H L H 5 L H 6 H L L 7 L L 8 H H H			
	C - G	L	Н		
FUNCTION	L - R	H	L		
	L - D	L	L		
	0	Н	Н	Н	Н
	1	L	н	Н	н
	2	H	L	н	H
	3	L	L	н	Н
DC BIAS	4	Н	Н	L	H
VOLTAGE	5	L	н	L	H
	6	H	L	L	Н
	7	L	L	L	H
	8	H	Н	н	L
	9	L	Н	H	L

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SECTION IV THEORY OF OPERATION

4-1. INTRODUCTION.

4-2. This section contains the theory of operation for the Model 4271A 1 MHz Digital LCR Meter. Paragraph 4-3 describes basic principles. Paragraph 4-14 covers functional description of the basic operation of the Model 4271A and employs a simplified block diagram. In paragraph 4-25 a block diagram description is presented for describing instrument operation in detail. Refer to schematic diagram in Section VIII for full circuit details. Options are discussed in Section VII.

4-3. OPERATING PRINCIPLES.

4-4. The HP Model 4271A is comprised of three major circuit sections (see Figure 4-1). The Bridge Section, here a voltage ($V_{\rm variable}$) proportional to value of DUT (device under test) and a voltage ($V_{\rm ref}$) proportional to the Range Resistance are developed and transmitted to the measurement section. In the measurement section, the value of the DUT is measured as a ratio of $V_{\rm variable}$ to $V_{\rm ref}$. This value is presented to and displayed by the Digital Control and Display Section controls the Bridge and Measurement Sections.

4-5. BRIDGE SECTION.

4-6. A simplified diagram of the Bridge Section is shown in Figure 4-2. Figure 4-2 is the simplified circuit for a C-G (C-D) measurements.

4-7. In making C-G (C-D) measurements, the constant voltage $V_{\rm ref}$ is applied to the DUT and $V_{\rm var}$ to range resistor $G_{\rm R}$. The $V_{\rm var}$ is a variable voltage

and is proportional to the values of C_X and G_X when the unbalance current i_d becomes zero (bridge is balanced). Derivation of $V_{\rm var}$ is given by the following equation:

$$V_{\text{var}} = -V_{\text{ref}} \cdot \left(\frac{G_X}{G_R} + j \frac{\omega C_X}{G_R} \right)$$
 (4-1)

 V_d has to be accurately zero for $V_{\rm ref}$ and $V_{\rm var}$ to be accurate. To do this a bridge technique is used in the $4271\,A.$

4-8. For L-R (L-D) measurements, $V_{\rm ref}$ is applied to range resistor and $V_{\rm var}$ to $H_{\rm CUR}$ terminal on front panel. Thus, the current flowing through DUT is determined by the values of $V_{\rm ref}$ and the range resistor and, therefore, becomes a constant current. As the voltage $V_{\rm var}$ across the DUT is the product of the above constant current and the impedance of DUT, $V_{\rm var}$ is proportional to the value of DUT:

$$V_{\text{var}} = -V_{\text{ref}} \cdot \left(\frac{R_{X}}{R_{R}} + j \frac{\omega L_{X}}{R_{R}} \right)$$
 (4-2)

 $(R_X + j\omega L_X)$ is a sample.

Equations (4-1) and (4-2) are of the same type. This shows that the measurement method is same for C-G and L-R measurements. As the bridge circuit in the 4271A uses the four-terminal method, leadwires can be extended to the measuring point. The measuring error can thus be minimized.

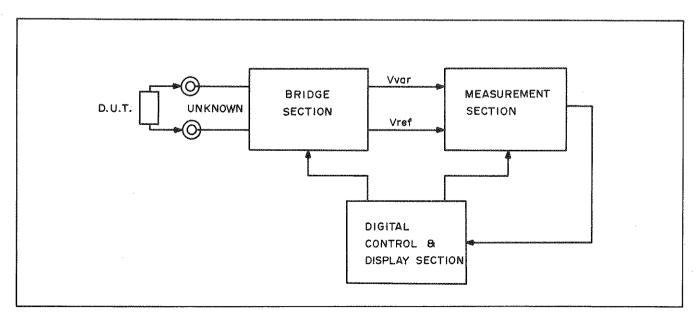


Figure 4-1. Block Diagram of 4271A Principles.

4-9. MEASUREMENT SECTION.

4-10. The Measurement Section employs the dual slope type DVM measuring technique. Figure 4-3 is a simplified block diagram of the measurement section. The C-G measurement equation is then:

$$V_{\text{var}} = -V_{\text{ref}} \cdot \left(\frac{G_{X}}{G_{R}} + j \frac{\omega C_{X}}{G_{R}} \right)$$
 [See (4-1)]

Switches $S_{\rm V},~S_{\rm G},~S_{\rm X_1}$ and $S_{\rm X_2}$ are closed and two integrators are charged for the constant time T_1 (20ms). The charges $q_{\rm C/L}$ and $q_{\rm G/R}$ in their respective integrators are:

$$q_{C/L} = -k_1 \frac{\omega C_X}{G_R} G_S V_{ref} T_1$$
 (4-4)

$$q_{G/R} = -k_2 \frac{G_X}{G_R} G_S V_{ref} T_1$$
 (4-5)

After charging for T_1 , switches S_r , S_G , S_{X1} and S_{X2} are closed and $q_{C/L}$ and $q_{G/R}$ are discharged until the outputs of the integrators become 0 volts. When the discharge time of the C/L integrator is T_2 :

$$-K_1 \frac{\omega C_X}{G_R} V_{ref} G_S T_1 + K_1 V_{ref} \omega C_S T_2 = 0$$
(4-6)

$$\frac{\mathbf{T}_2}{\mathbf{T}_1} = \frac{\mathbf{G}_S}{\mathbf{G}_R} \cdot \frac{1}{\mathbf{C}_S} \quad \mathbf{C}_X \tag{4-7}$$

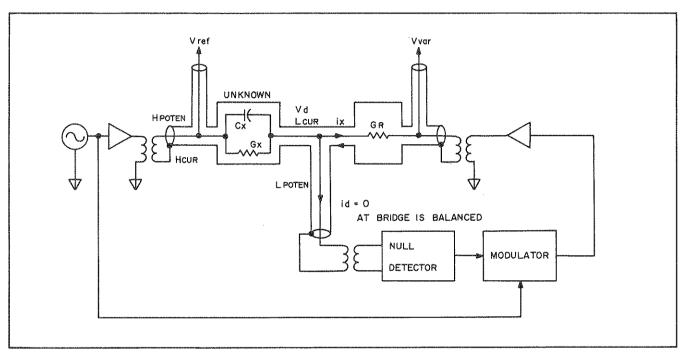


Figure 4-2. Simplified Block Diagram of Bridge Section.

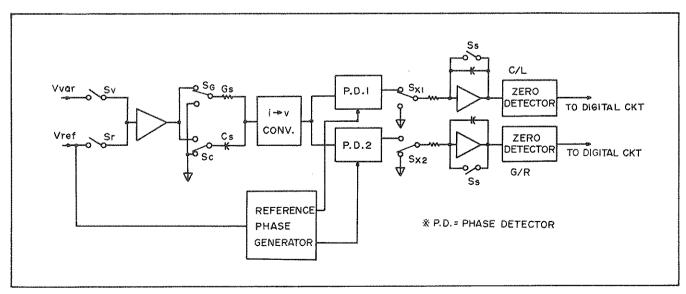


Figure 4-3. Measurement Section.

Thus, the value of C_X is known by counting and displaying time T_2 . When the discharge time of G/R integrator is T_3 :

$$-K_2 \cdot \frac{Gx}{G_R} \cdot V_{ref} \cdot G_S T_1 + K_2 V_{ref} \cdot G_S \cdot T_3 = 0$$

$$(4-8)$$

$$\frac{\mathbf{T}_3}{\mathbf{T}_1} = \frac{1}{G_{\mathbf{R}}} \cdot G_{\mathbf{X}} \tag{4-9}$$

 G_X becomes known by counting and displaying time T_3 . The coefficients K_1 and K_2 do not cause a measurement error. Applying equation (4-2) instead of (4-1) to the above enables L_X and R_X measurements to be made instead of those for C_X and G_X . To avoid an error caused by interference between simultaneous (C-G) and (L-R) measurements, each measurement should be performed independently.

4-11. D-Measurements. Switches S_r , S_C , and S_{X_1} are closed and the C/L integrator is charged during time T_4 . After charging, switches S_V , S_G , S_{X_1} and S_{X_2} are closed and the charge of the C/L integrator is discharged until the output of C/L integrator becomes 0 volts. During discharge time T_5 , G/R integrator is simultaneously charged. Therefore:

$$V_{\text{ref}} \cdot \omega C_S \cdot T_4 - V_{\text{ref}} \cdot \frac{\omega C_X}{G_R} \cdot G_S \cdot T_5 = 0$$
(4-10)

Switches S_r , S_G and S_{X_2} now close and the charge of G/R integrator is discharged until the output of G/R integrator becomes zero volts. This discharge time is T_6 , and:

$$-V_{\text{ref}} \frac{G_{X}}{G_{R}} \cdot G_{S}T_{5} + V_{\text{ref}} G_{S}T_{6} = 0$$
 (4-11)

From the above two equations:

$$\frac{T_6}{T_4} = \frac{C_S}{G_S} \cdot \frac{G_X}{C_X} = \frac{\omega C_S}{G_S} \cdot \frac{G_X}{\omega C_X} = \frac{D_X}{D_S}$$
(4-12)

When $C_S=100 pF$, $G_S=1 mV$ and $\omega=2 \pi \cdot 10^6$ rad., from the above equation:

$$D_{S} = \frac{G_{S}}{\omega C_{S}} = \frac{10^{-3}}{2\pi \cdot 10^{6} \cdot 100 \cdot 10^{-12}} = 1.5920$$
(4-13)

To directly display the value of $D_{\rm X}$ from the time $T_6, \ T_4$ is set to the time corresponding to 15920 clock pulses.

- 4-12. Digital Control/Display Section.
- 4-13. The Digital Section counts and displays time interval from Measurement Section and executes timing control, range control, etc. of the Bridge and Measurement sections.
- 4-14. FUNCTIONAL DESCRIPTIONS.
- 4-15. Analog Section.
- 4-16. Figure 4-20 is a simplified block diagram of the Model 4271A. This diagram is composed of blocks representing board assemblies. Outputs of A4 Oscillator are sent to A9 Power Amplifier, A8 Modulator and A13 Reset/Clock Pulse Generator.

LPOTEN terminal on front panel of 4271A is connected All Current Detector to All Current Detector. detects and amplifies unbalance current of bridge which is the difference of current flow between DUT and range resistor of A12. The output of All Null Detector is sent to A8 Modulator as an unbalance voltage signal. A8 Modulator controls the amplitude and phase of a modulated voltage to drive the unbalance voltage to be zero volts. This modulated voltage and the constant voltage from A4 Oscillator are applied through switches to the two power amplifiers of A9, respectively. One output of A9 Power Amplifier is fed to H_{CUR} terminal and the other to the range resistor of A12. Range resistors of A12 are switched by the range control signal from A16 Function/Range Control. VD which is the voltage of HPOTEN terminal and VR which is the voltage across the range resistor are sent to A10 Buffer Amplifier/Gs, Cs CKT. and VR are applied to A6, 7 Phase Detector/Integrator through switches, C_S/G_S circuit and amplifier which are controlled by the signal from A15 Step Control. A6 and A7 convert measured quantity to time interval by the dual slope technique and the time interval signal is sent to Al4 Gate/Transfer Control. The reference phase signals required in phase detectors of A6 and A7 are generated by Reference Phase Generator.

4-17. DIGITAL SECTION.

- 4-18. Board A13 is the Reset/Clock Pulse Generator. It produces 500kHz clock pulses generated by a 1MHz sine wave and operates whenever the power switch is on. During the sampling time reset pulses are generated.
- 4-19. In A14 Gate/Transfer Pulse Control the counter reset signal and gate signal are transmitted to A18 Counter. A 400 μ sec time span is generated. A switch control signal is generated and transmitted to A6, A7 Integrators. A step shift signal is transmitted to A15 and with the step signal from A15, the transfer pulses are transmitted to A18 Counter and A19 Display.
- 4-20. In A15 Step Control, the step counter is advanced by the step shift signal from A14. The step signals generated by the step counter control switches of A10 Buffer Ampl. & C_S , G_S Ampl. A15 receives integrator zero detect signal from A6/A7 or over flow signal from A18 and transfers "0" detect signal to A14.
- 4-21. In A16 Function and Range Control, range and function signals are generated by range and function signals from A2 Front Panel (or Remote) and transmitted to A17 Auto Range and Lamp Driver. The range switch signal is transmitted to A12 Reference Resistor.
- 4-22. A17 Auto Range/Lamp Driver, lights the unit lamps of A19 Display by decoding function and range signals from A16. The control signal for autoranging is generated by signals from A13, A15 and A18 and transfered to A13 and A16.
- 4-23. In A18 Counter, by the enabling gate signal

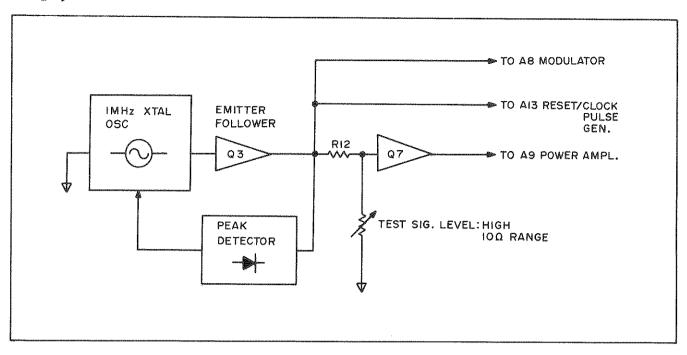


Figure 4-4. Block Diagram of A4 Board.

from A14, clock pulses are counted in the decimal system. Meaningless digits are blanked depending upon position of Range and Function control settings. The overflow signal is transmitted to A15, A16 from the A18 counter. Also produced is the 10000 count detect signal and the 15920 count detect signal which are transmitted to A14 to control charge time of integrator.

4-24. In A19 Display, LED-ICs are used. Each of the ICs includes a BCD to decimal decoder and a latch memory.

4-25. CIRCUIT DESCRIPTION.

4-26. Beginning with 4-27 a circuit description of the schematic operation of every board (A3 thru A19) is presented along with an accompanying simplified block diagram. For all additional details, see schematics in manual section VIII or refer to the timing diagram discussion in this section.

4-27. OSCILLATOR (A4).

4-28. Figure 4-4 is a block diagram of the A4 Oscillator. The output circuit of the 1MHz Quartz Oscillator is an Emitter Follower. The signal from Q3 Emitter controls the peak detector to stabilize output level of the oscillator. This 1MHz signal is transmitted to A8 Modulator, to A13 Reset/Clock Pulse Generator and also transmitted to A9 Power Amplifier through Emitter Follower Q7.

4-29. REFERENCE PHASE GENERATOR (A5).

4-30. Refer to Figure 4-5 for block diagram of A5 Reference Phase Generator. At the Phase Shifter U2 and U3, the signals for phase detecting $e\phi_{G/R}$ and $e\phi_{C/L}$ are generated and are transmitted to A6/A7

Integrators. If a Low signal comes, Q1 and Q2 are turned off and the input signal is amplified 25 times. In the low signal does not come, Q1 and Q2 are turned on and the input signal is amplified 1 time.

4-31. C/L (G/L) INTEGRATOR (A6 & A7).

4-32. Figure 4-6 is the block diagram of the A6C/L or A7 G/\bar{R} Integrator. The output signal from A10 Buffer Ampl. and Cs, Gs Ampl. is phase detected by the $e\,\phi_{C/L}$ (e $\phi_{G/R}$) signal which is generated in the $A\bar{\bf 5}$ Reference Phase Generator. Charging and discharging of capacitor C15 is done by operating the switches with Sx, Sy from A14 Gate/Transfer Pulse Control. The output of the integrator is compared to zero volts by the zero level detector. When the output of the integrator becomes zero, a zero detect signal istransmitted to A15 Step Control. The switch Q13 for discharging C15 is controlled by Ss from A15 (see paragraph 4-57). An auto offset adjustment is performed to remove the offset voltage of U2 and phase detector by Q8 and C8.

4-33. MODULATOR (A8).

4-34. Figure 4-7 is the block diagram of A8 Modulator. The null out signal from A11 Current Detector is divided into their real parts and imaginary parts by the $e\phi_{\rm C/L}$ signal and $e\phi_{\rm G/R}$ signal and are transmitted to the Modulator. Two signals, one phase synchronized with the reference signal and one 90° phase shifted, are generated prior to modulating. The signal which has same phase is modulated with the real part; the signal which has a 90° shifted phase is modulated with the imaginary part. These modulated signals are summed by the Summing Amplifier. The summed signal is filtered by the Tuning Amplifier to remove the third harmonic and transmitted to A9 Power Amplifier through Emitter Follower Q17.

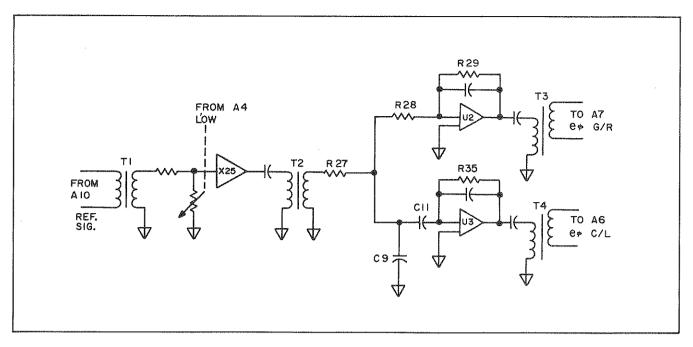


Figure 4-5. Block Diagram of A5 Board.

4-35. POWER AMPLIFIER (A9).

4-36. Figure 4-8 is the block diagram of A9 Power Amplifier. The output signals from A4 Osc and A8 Modulator are amplified. When FUNCTION is set to C, switches K1, K2 and K3 are as shown in Figure 4-9. If FUNCTION is set to L, all switches are reversed. The test signals from A4 and modulated output from A8 are amplified. One is transmitted to A12 Reference Resistor through T_2 . The other is transmitted through a resistor and T_1 to remove noise when the function is set to L. The signal for offset adjustment

is transmitted through P1. The signal to the front panel connector is transmitted through P2. This assembly also contains the circuit for DC bias.

4-37. BUFFER & C_S/G_S AMPLIFIERS (A10).

4-38. Figure 4-9 is the block diagram of A10 Buffer Ampl. and C_S, G_S Ampl. During a C measurement time, a reference signal, and during L measurement time, the unknown signal are transmitted from "H_{POTEN}" connector on the front panel through J2. During a C measurement time, an unknown signal and during a L

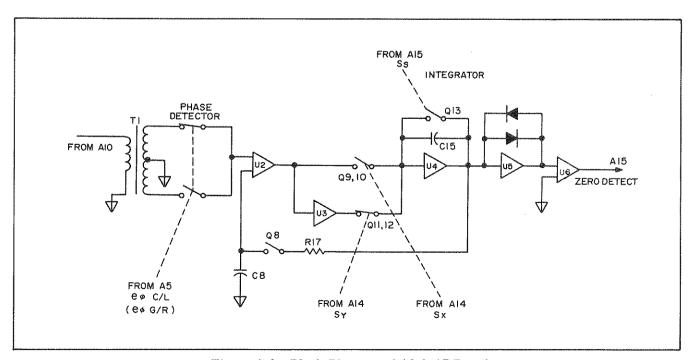


Figure 4-6. Block Diagram of A6 & A7 Board.

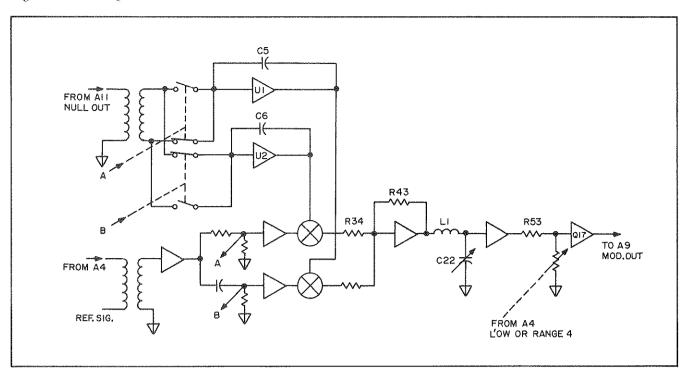


Figure 4-7. Block Diagram of A8 Board.

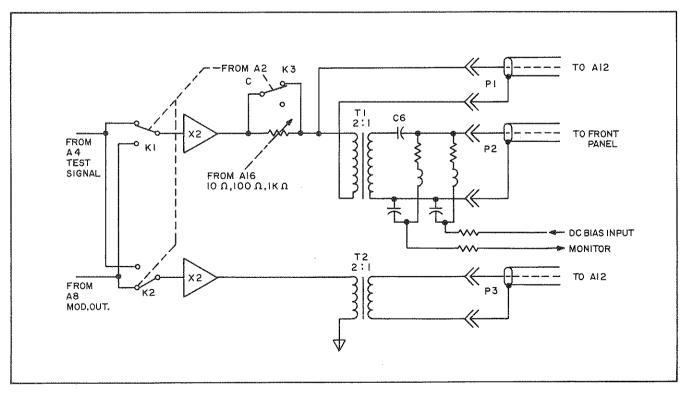


Figure 4-8. Block Diagram of A9 Board.

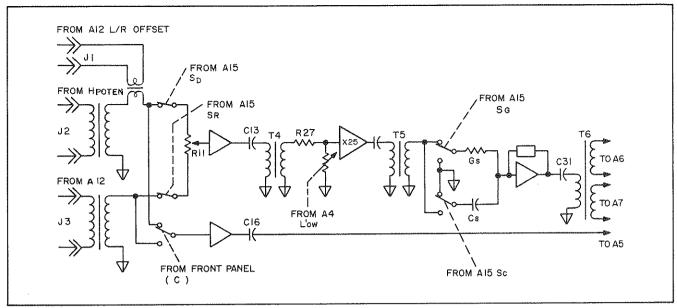


Figure 4-9. Block Diagram of A10 Board.

measurement time, a reference signal is transmitted from A12 Reference Resistor through J3. The S_D and S_R signals from A15 determine whether a reference signal or an unknown signal is fed to A6 & A7 Integrators. After amplification, these signals are transmitted to $G_{\rm S}/C_{\rm S}$ Amplifier through T_6 . Since the $G_{\rm S}/C_{\rm S}$ Amplifier signal passes through T_6 , it is changed in amplitude and phase. In this manner, C/L and G/R become measurable. See paragraph 4–57 TIMING DIAGRAM.

4-39. NULL DETECTOR (A11).

4-30. Figure 4-10 is a block diagram of the A11 Null Detector. The signal from the "LPOTEN" connector on Front Panel is fed to Current Detector. The feedback

impedance of the Current Detector is varied with the range signal from A16. The output of the Current Detector is attenuated when low signal does not come from A4 and fed through its amplifier and T2 to the limit amplifier. At the limit amplifier, the signal is changed to a square wave, then back to a sine wave by a tuning filter and fed to the A8 Modulator. When the output voltage is between 150 and 250mV an "UNBAL" signal is fed to A13.

4-41. Rs & OFFSET CKT (A12).

4-42. Figure 4-11 is the block diagram of A12-Rs and Offset Circuit. In this board, selection of range resistor and adjustment of offset are accomplished. Range resistors are selected by K1, K3, K4 and Q4

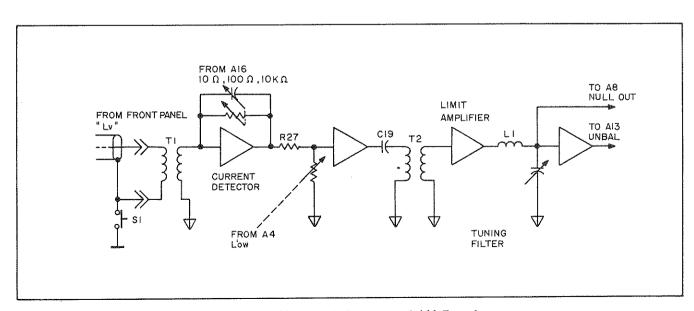


Figure 4-10. Block Diagram of All Board.

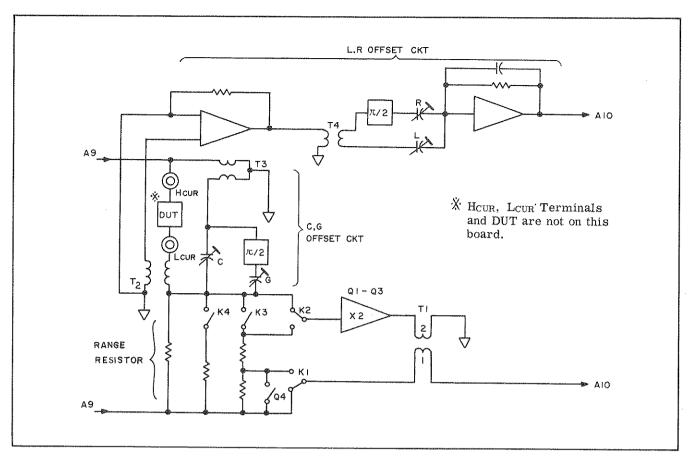


Figure 4-11. Block Diagram of A12 Board.

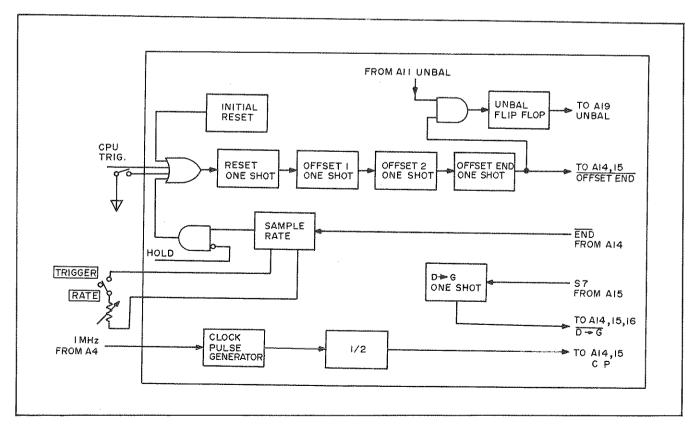


Figure 4-12. Block Diagram of A13 Board.

which are controlled with signals from A16 (Range & Function Control). A16 is controlled from the front panel with the RANGE and FUNCTION switches. Q1, Q2, Q3 and T1 form a circuit which is used to accurately detect exact voltage drop across range resistor. This voltage, which is $E_{k_1}-E_{k_2}$, is transmitted to A10 through transformer T1 and compensates for the voltage drop which is caused by residual resistance or wiring resistance. The Offset Circuit compensates for stray capacitance, residual conductance (when the DUT is a capacitor), residual inductance and residual resistance of DUT. The C/G Offset Circuit compensates for leakage current and produces a reverse current to the leakage current. The L/R Offset Circuit detects the current which flows through DUT and generates a compensating voltage and which is added to voltage from the HPOTEN terminal.

4-43. RESET/CLOCK PULSE GENERATOR (A13).

4-44. The Block Diagram of A13 Reset/Clock Pulse Generator is shown in Figure 4-12. The reset one shot multivibrator is triggered by initial reset one shot multivibrator output, Remote Trigger signal or CPU Trig signal and generates a reset pulse with a pulse width of $50\,\mu{\rm sec}$. This reset pulse is fed to A14, A15 and A17 boards and resets the 4271A to its initial conditions. An offset 1 one shot multivibrator is triggered by the reset pulse and generates a pulse of 30msec pulse width during which an offset adjustment in the Analog Section is executed. The output of offset 1 one shot triggers offset 2 one shot multivibrator, the output of which is fed to A5, A15 and A17

boards. The time interval for offset 2 is 20msec. An offset end pulse ($4\,\mu s$ wide) is generated by output of offset 2 one shot and is fed to A14 and A15 boards as a step start command. After completion of a measuring cycle, an end pulse is transferred from A14 board and triggers the sample rate generator. At the clock pulse generator, a 1MHz signal from A4 oscillator is shaped into a square wave by a differential comparator and its frequency divided into 500kHz by a 1 bit binary counter. The 500kHz clock pulse (CP) is used throughout the 4271A.

4-45. GATE/TRANSFER PULSE CONTROL (A14).

4-46. The Block Diagram of A14 Gate/Transfer Pulse Control is shown in Figure 4-13. A 2msec one shot multivibrator is triggered by a 15,920 or 10,000 signal from the A18 board, a "0" detect signal from A15 board, or an offset end signal from A13 board and the output enables generation of GATE and step shift signals. The Gate Signal controls the counter on the A18 board and the step shift signal is used as the clock pulse of the step counter on A15 board. An 800 $\mu sec FF$ generates a time span of $800 \mu sec$ under the condition that Sr signal is at high level. The switching of S_X and S_Y is controlled by the outputs of the 800 μ sec FF and 2msec FF. The output of 800 μ sec FF is also used as a gate signal for minus sample meas-The C Transfer, G Transfer and End signals are generated by a transfer pulse generator whose inputs are the step signals (step 5, step 6, and step 8) from A15 board.

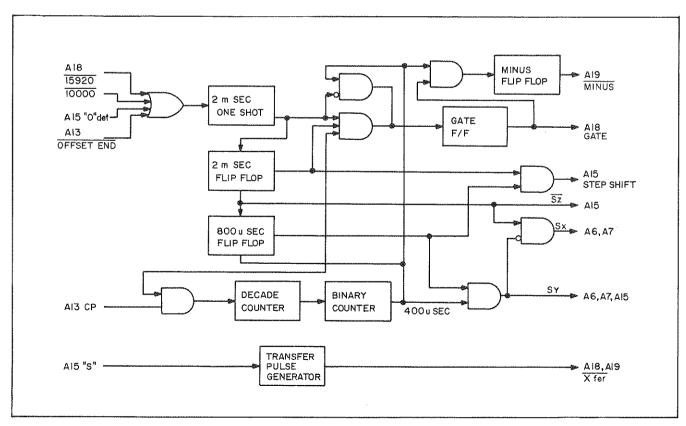


Figure 4-13. Block Diagram of A14 Board.

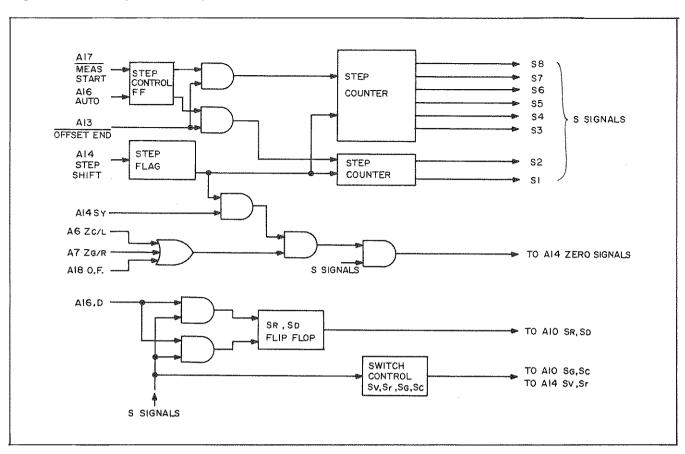


Figure 4-14. Block Diagram of A15 Board.

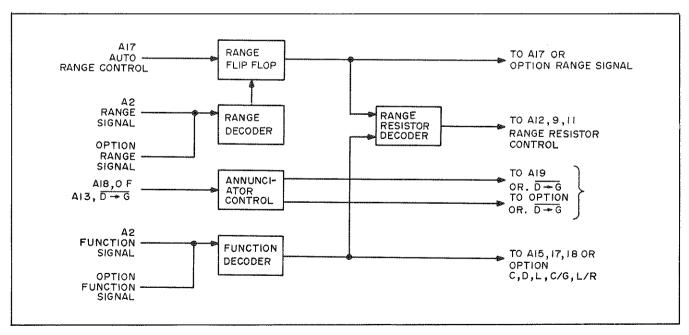


Figure 4-15. Block Diagram of A16 Board.

4-47. STEP CONTROL (A15).

4-48. The Block Diagram of A15 Step Control is shown in Figure 4-14. Step counter starts from step 1 when AUTO range is selected or from step 3 when MANUAL range is selected and advances to step 8. Each step signal, which is the high turning state of each digit of step counter, is used as a control signal for switching according to each step. Z C/L (output of A6 C/L Integrator is 0 volt) and Z G/R (output of A7 G/R Integrator is 0 volt) signals from A6 or A7 board are gated by step signals and fed to A14 board as an "0" detect signal. Switch control signals of $S_{\rm R}$, $S_{\rm D}$, $S_{\rm G}$, $S_{\rm C}$, $S_{\rm V}$ and $S_{\rm T}$ are generated by step signals and D (D Measurement) signal. Refer to Paragraph 4-57 for timing sequence.

4-49. FUNCTION/RANGE CONTROL (A16).

4-50. The Block Diagram of A16 Function/Range Control Board is shown in Figure 4-15. Range signals from A2 or option board are decoded by Range Decoder. Function signals from A2 (or option board) are decoded into function signals of C, D, C/G and L/R, by the function decoder. Range signals and Function signals are decoded into a range switch signal for A12 by range resistor decoder. By annunciation control when OF (over flow) signal or D—•G signal is fed to A16, Out of Range or D—•G signal is generated and fed to A19.

4-51. AUTO RANGE/LAMP DRIVER (A17).

4-52. Figure 4-16 is the Block Diagram of A17 Auto Range/Lamp Driver board. The driver signal to light the unit lamp on A19 and decimal point control signal to determine decimal point position on the display are generated by unit lamp driver/decimal point decoder with range and function signals from A16. An auto range control signal is generated by input signals of

1,600 and 18,000 counts from A18, select range signal and gate signal from A15, and fed to A15, A16.

4-53. COUNTER (A18).

4-54. Figure 4-17 is the block diagram of A18 Counter. The CP (clock pulse) is counted by the decade counter and binary counter with gate signal from A14. This count is transmitted as BCD information to A19. A 10,000 detect signal and 15,920 detect signal are generated and transmitted to A14. Meaningless digits are blanked with the blanking control as commanded by the sample rate signal from A13, transfer pulses from A14 and decimal point control signals from A17. An OF (over flow) signal is generated by the binary counter.

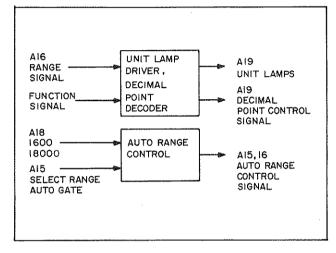


Figure 4-16. Block Diagram of A17 Board.

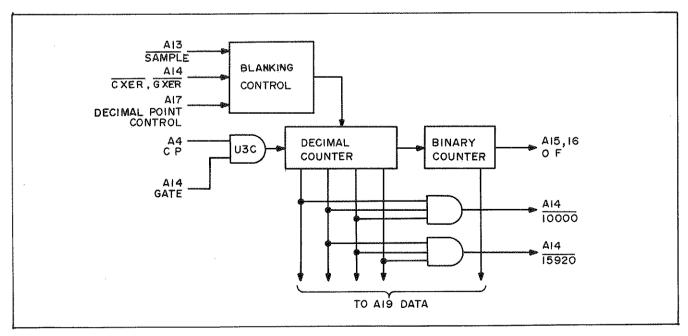


Figure 4-17. Block Diagram of A18 Board.

4-55. DC POWER SUPPLY (A3).

4-56. Figure 4-18 is the block diagram of A3 DC Power Supply. The ground terminal of the +50V, 20V, -20V, +12V and -12V supply is the "A. GND" (ground for analog circuit) and the ground terminal of +5V supply is "D. GND" (ground for digital circuit). Ground terminals of analog boards connect with A. GND. Ground terminals of digital boards connect with D. GND. D. GND also connects with A. GND on the A3 board, and they, in turn, are connected to the chassis. When the +12V and +5V outputs increase beyond 25V and 6.7V, respectively, the voltage protector circuit opens fuse F1. In addition, if the output of the +12V and +5V supplies are accidentally shorted, a current protector circuit opens the +12V and +5V outputs by turning off Q2 and Q3, respectively.

4-57. TIMING DIAGRAM DISCUSSION.

4-58. The dual slope type DVM which is used in the Model 4271A individually integrates the real parts (G/R) and imaginary parts (C/L) of the measured voltage. This interaction is performed alternately to avoid mutual interaction. When the AUTO range is selected, C/L and G/R are initially charged together and discharged to select the suitable range. C/L and G/R are again charged together, C/L is discharged and counted and then G/R is charged and discharged and counted. Before discharging, the integrator charges for 400 $\mu \rm sec$ to measure small values correctly (see Figure 4-19).

4-59. For descriptive purpose refer to Figure 4-19. When the power switched to on, there is about 2sec hold time until the output of OSC becomes stable. After this hold time a reset pulse is generated by the reset one shot and all the logic circuits are reset. An offset 1 pulse (30msec) is generated with the reset pulse and during this time (30msec) the offset adjustment of A6, A7 is performed. After offset adjustment

the offset 2 pulse (20msec) is generated. An offset end pulse $(4\mu sec)$ is generated by the output of offset 2 pulse and with this pulse a 2msec hold signal is generated. During this time the outputs of the integrators are driven to zero. At this moment, step 1 begins. In step 1 S_G, S_V, S_X signals are turned on to integrate the unknown signal through G_S of A10. charge time is set at 10000 counts (20msec). the detect signal of 10000 counts is generated, a 2ms hold signal is generated and step 2 starts and Sx is turned off. During step 2, S_G, S_C, S_r, signals are turned on to discharge with reference signal. A 800 μ sec time span after the 2msec hold time protects the zero detector from mis-operating because of switch-The gate of counter is opened after ing transients. 800 µsec time span. After gate is opened, the two integrators are discharged with reference signal and counting is performed until the output of the integrators become zero and a "0" detect signal is generated (at the end of the count). That is to say, the range is set by the larger of C/L or G/R. If the count in step 2 is between 1602 and 18040, a "start measure" signal is generated; if not, a "range shift" signal and an "up shift" or "down shift" signal are generated If a "start measure" signal is generated, the offset adjust by offset 1 is performed again and step 3 begins. If a "range shift" signal is generated, the offset 1, offset 2, and step 1 begin again (on another range). Beginning with step 3, an actual measurement is performed.

4-60. Steps 3 to 5 are the C/L measuring cycle. Step 3 is as same as step 1 (sometimes the range is different). In step 3, the unknown signal is charged up during 10000 counts. A2msec hold is performed and then step 4 starts. After the 2msec Hold, the integrator is charged with the reference signal for 400 $\mu \rm sec$ through Gs of A10 (Sy is on). The Sy is turned off and Sx is turned on. The G/R Integrator is discharged with reference signal until output of the integrator becomes zero. During this discharging, a

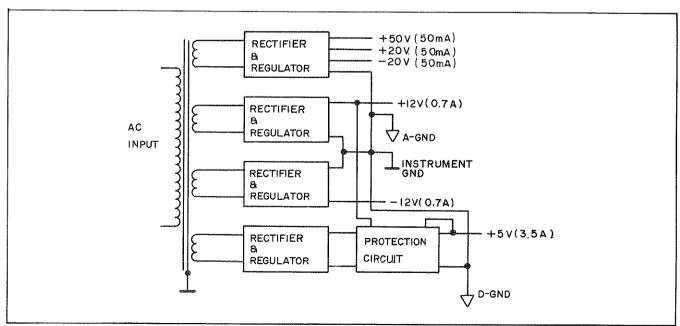


Figure 4-18. Block Diagram of A3 Board.

small portion of C/L, which originated when G/R was charged, flows away. This is the compensation cycle. After compensation cycle, a 2msec hold time is used again. After the hold time, $S_{\rm Y}$ is turned on, C/L integrator is charged through $C_{\rm S}$ of A10 with the reference signal for 400 $\mu{\rm sec}$. $S_{\rm X}$ is turned on and C/L Integrator is discharged with reference signal after $S_{\rm X}$ is turned on. The gate of counter is opened until output of C/L Integrator becomes zero and number of the counts is displayed with C/L transfer pulse.

4-61. Steps 6, 7, 8 are the G/R measuring cycle. This cycle is as same as the C/L measuring cycle except that C/L is exchanged for G/R.

4-62. D MEASUREMENT.

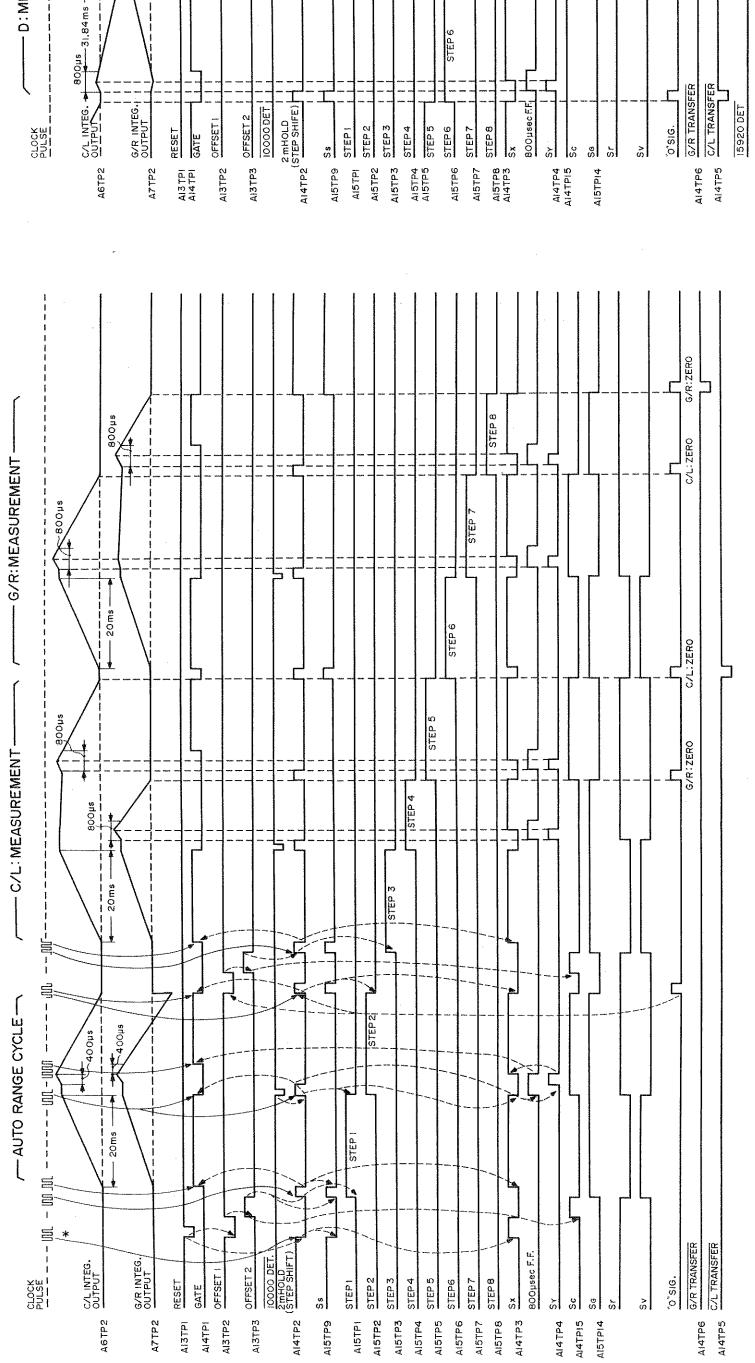
4-63. In D measurements the first to fifth steps are

performed the same as for G or R measurements. After the 2msec hold time of sixth step, Sy signal is at high level for $400 \mu sec.$ The integrators are charged up through Gs of A10 board by reference signal After this $400\,\mu\mathrm{sec}$, Sy signal becomes low level and Sx signal becomes high level and charging starts. As soon as it passes 400 µsec (after Sx signal is at high level), the Gate is opened and continues to remain open for 15920 counts of counter. Immediately after the 15920 counts signal is detected, a 2msec hold signal is generated and seventh step starts. In seventh step, G/R integrator is integrated through Gs of A10 board by unknown signal until output of C/L integrator becomes 0 volt. As integrated value of G/R integrator has D information, the G/R integrator is discharged by reference signal in either step and its discharging time is counted and displayed. The display of the value of D is performed by G/R transfer pulse which is also used as an END pulse.



-800µs

- D: MEASUREMEUT



1 I STEP8

STEP 7

* ARROWS FROM CLOCK PULSES MEAN TO SYNCHRONIZE WITH CLOCK PULSE

Figure 4-19. Timing Diagram.

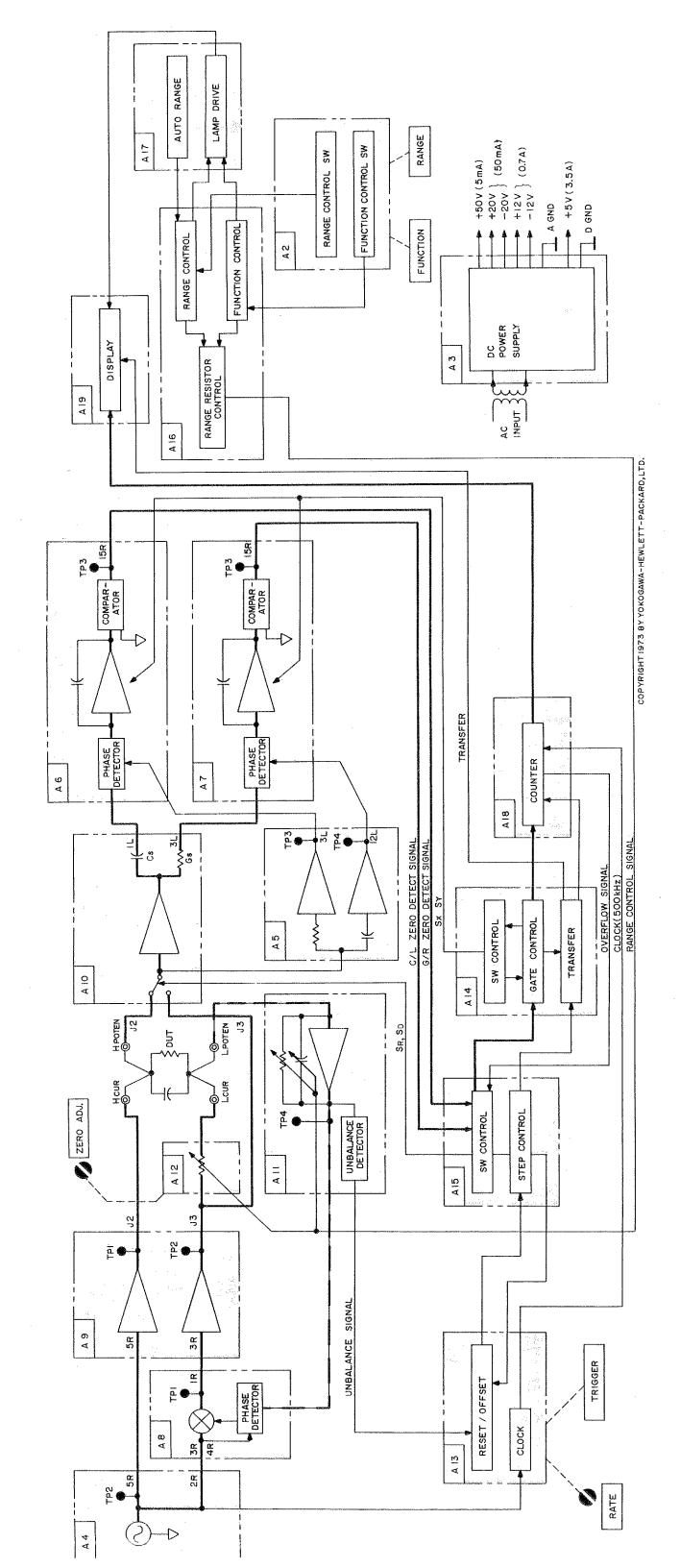
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Section IV Model 4271A

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Section IV Figure 4-20

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Table 5-1. Recommended Test Equipment.

HARACTERISTICS RECOMMENDED MODEL
General Radio 1405 - E 1405 - B 1406 - D 1406 - A 1407 - D
General Radio 900 - WN 1442 - G 900 - W100 1442 - N
HP P/N 0160 - 2218
HP P/N 9140 - 0137 9140 - 0129
HP P/N 0698 - 3157 0698 - 4020 0698 - 3186 0757 - 0346
0pF - 180pF Vernier. HP Model 4440B
MHz, Voltage 3μV - 3V. HP Model 312A
put - Imp. >10MΩ. HP Model 3490A
, Voltage > 5V. HP Model 3310A
., Frequency 10MHz. HP Model 180A /1801A /1821A
HP Model 10525T
me 1µsec. HP Model 214A.
$mcy \approx 2$ - 3Hz. HP Model 3310A
HP Model 16021A 16022A 16023A
HP Model 4440B
ET-1467
$ ext{ET-1467}$ Impedance $1 ext{M}\Omega$. HP $5300 ext{ w}/5301 ext{A}$

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