TELEDYNE LECROY
Everywhereyoulook™

quantumdata™ 980
48G Protocol Analyzer / Generator module
for HDMI® Testing
Deep Analysis & Generation of Fixed Rate Link (FRL) with Forward Error Correction (FEC)
Now Supports Optimized Video Timing (OVT) Formats

Key Features

- View incoming FRL and TMDS (encrypted or unencrypted) video frames and video metadata and timing in real time
- Use generator or analyzer in three (3) and four (4) lane configurations at all lane rates: 3Gbps, 6Gbps, 8Gbps, 10Gbps and 12Gbps (48Gbps aggregate)
- Video generator function supports TMDS and FRL for video resolutions up to 8K and 10K resolutions compression including NEW Optimized Video Timing (OVT) formats
- Certified "Test Device Approved for Dolby Labs, Inc." for HDMI and eARC Dolby audio generation & analysis including Dolby Vision Source Led tests
- Evaluate 4K and 8K HDR10 UHCTVs with HDR Lab
- View captured FRL and TMDS data elements graphically in Event Plot and in Data Decode table; use searching and filtering to find data
- View FRL packet mapping into Character Blocks and Character Block mapping into Super Blocks
- Verify Display Stream Compression (DSC) on FRL, DSC capable sources or sinks
- UPDATES Run FRL & DSC source & sink compliance tests
- View embedded TMDS video, protocol and metadata elements, in FRL stream
- Monitor of FRL Link Training transactions in the Auxiliary Channel Analyzer (ACA) utility to show SCDC reads and writes over the DDC channel
- Run pixel error test on incoming TMDS streams
- Passively monitor DDC channel in TMDS or FRL mode (FRL mode requires custom cable)
- Passively monitor TMDS video and metadata (without HDCP) and DDC between a source and sink (requires both Tx and Rx licenses)
- View Lane Error Counts and Reed Solomon Counts in the SCDC CED registers
- Verify the eARC common mode channel on either an eARC Tx or Rx device
- Run eARC compliance tests on an eARC Tx or Rx device; all tests supported
- Run HDCP 2.3 source compliance tests
- UPDATES Run HDMI TMDS source and sink compliance tests
- Run Gaming-VRR, Fast VActive and QMS-VRR tests
- Run HDR10+ Source Side Tone Mapping (SSTM) tests on UHDTVs
- Tests Power Cable Assemblies (PCA) for power requests
- Run test automation for compliance tests with the API

The Teledyne LeCroy quantumdata 980 48G Protocol Analyzer / Generator module for HDMI 2.1a Testing is equipped with HDMI Tx and Rx ports supporting HDMI Fixed Rate Link and FEC capture analysis and decode up to 48Gbps (12Gbps/Lane). The HDMI Rx analyzer port provides visibility into the Fixed Rate Link packetization—super blocks, character blocks and FRL packets and underlying TMDS video, protocol, control and metadata elements. The HDMI Tx video generator port transmits Fixed Rate Link video streams with embedded TMDS video, protocol, control and metadata elements. Supports Display Stream Compression (DSC) for testing both sources and sinks (including compliance testing). Supports FRL source and sink compliance testing. The module also supports the link training functions of the source and sink functions in the FRL mode in both 3 and 4 lane configurations. Enhanced Audio Return Channel (eARC) compliance testing is also supported for eARC Tx and eARC Rx devices.

FRL Analysis & Generation

The 980 48G Protocol Analyzer / Generator module provides video generation and deep analysis test features necessary to test the development of your HDMI 2.1 TMDS and FRL-capable source and sink devices. These features enable developers to identify and resolve interoperability problems early in the product life cycle. The enhanced FRL generator enables transmission of FRL and TMDS video streams through the HDMI Tx port. Supports user-selection of resolution (including 8K), frame rates, colorimetry, chroma sampling and color space.

eARC Testing

The 980 48G Protocol Analyzer / Generator module supports functional testing and compliance testing of enhanced Audio Return Channel sources Tx devices (e.g. UHD TV) and eARC Rx, devices e.g. sound bar).

Operation

The 980 48G Protocol Analyzer / Generator module supports video generation and analysis of the FRL/FEC HDMI data streams through the user friendly 980 Manager which presents the data in an easy to understand way.

FIXED RATE LINK (FRL) ANALYSIS

Capture and Decode (FRL & FEC)

The 980 48G Protocol Analyzer / Generator module captures and decodes incoming HDMI® 2.1 streams (encrypted or unencrypted) that have been packetized with Fixed Rate Link packet structures. These FRL-related data elements are depicted graphically in the Event Plot . The decoded data and the raw data is shown in table form in the Data Decode window.

The Forward Error Correction (FEC) characters are also shown as appended on the Character Blocks. The module reports the Lane Error Counts and the FEC Reed Solomon Corrections Count in the SCDC CED registers.

The underlying TMDS video and protocol elements such as the active video, data island and preamble blocks, are also depicted and decoded.

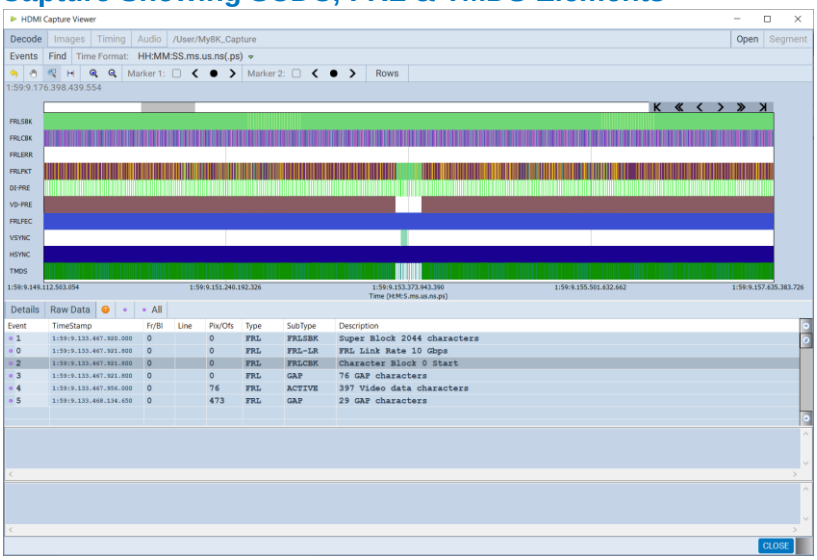
Each element is assigned a precise time stamp. Users can search and filter the FRL captured data by type.

Test Setup for Source Test

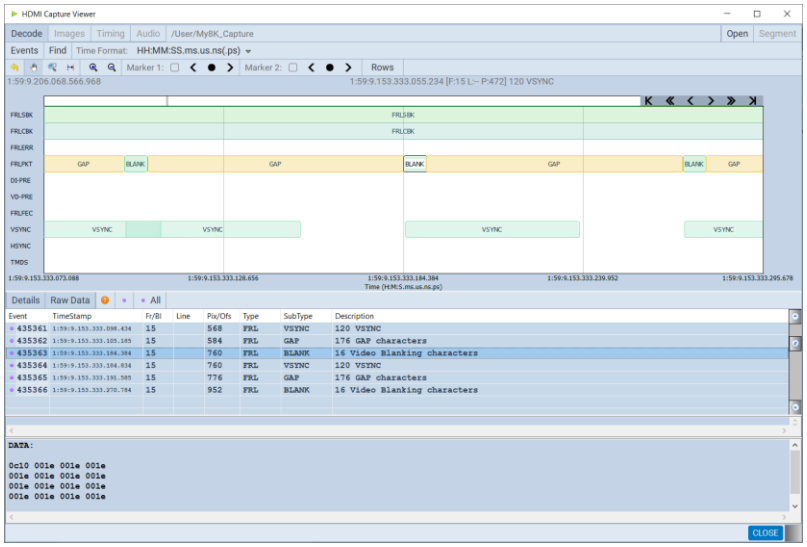
Real Time Analysis

The module's Real Time analysis feature enables you to monitor the incoming TMDS and FRL video and metadata, data islands and InfoFrames including High Dynamic Range (HDR) InfoFrames. A status bar at the top of the window provides an at-a-glance view of the essential incoming video parameters.

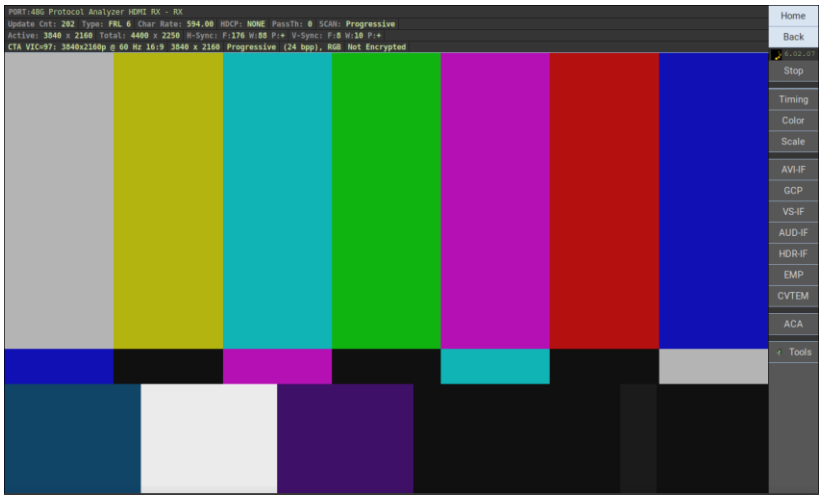
Capture Showing SCDC, FRL & TMDS Elements



Capture with FRL Elements & TMDS Video & Data Islands



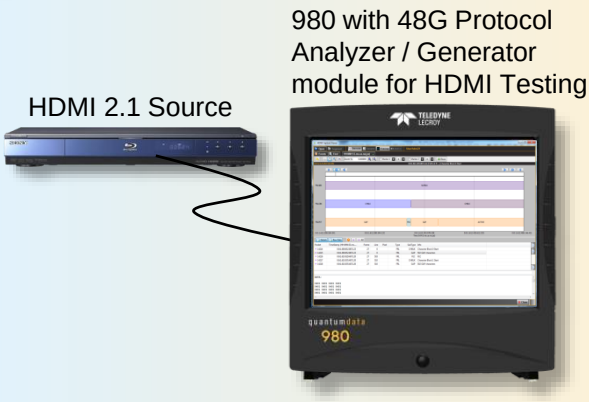
Real Time Analysis



FIXED RATE LINK (FRL) LINK TRAINING ANALYSIS

Link Training

The 980 48G Protocol Analyzer / Generator module supports Link Training configuration. The module emulates an HDMI 2.1 sink indicating the max FRL rate in the HF-VSDB of the EDID and various other essential link training parameters in the SCDC control registers.

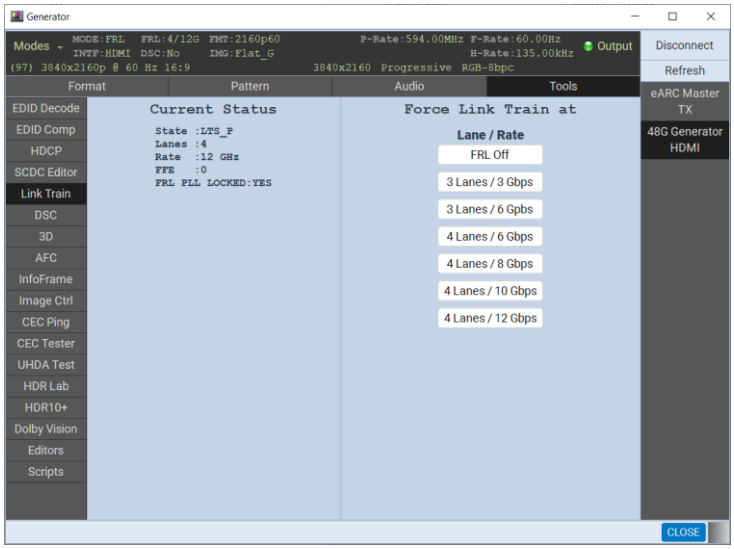


Test Setup for Source Test

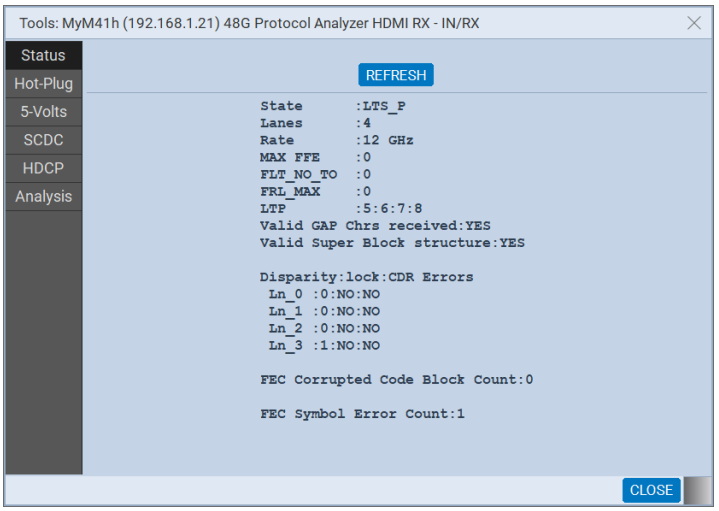
Auxiliary Channel Analyzer

You can use the 980 48G Protocol Analyzer / Generator module to monitor the Link Training transactions—EDID exchange and reads and writes to the SCDC registers over the DDC channel--with the Aux Channel Analyzer (ACA) utility. This enables you to verify link training functions to identify potential interoperability problems.

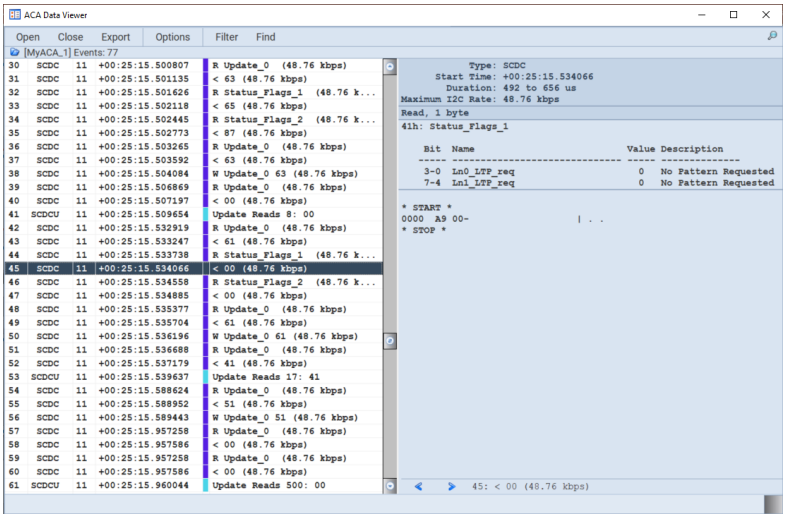
Link Training Status Screen



Analyzer Link Training Status Screen



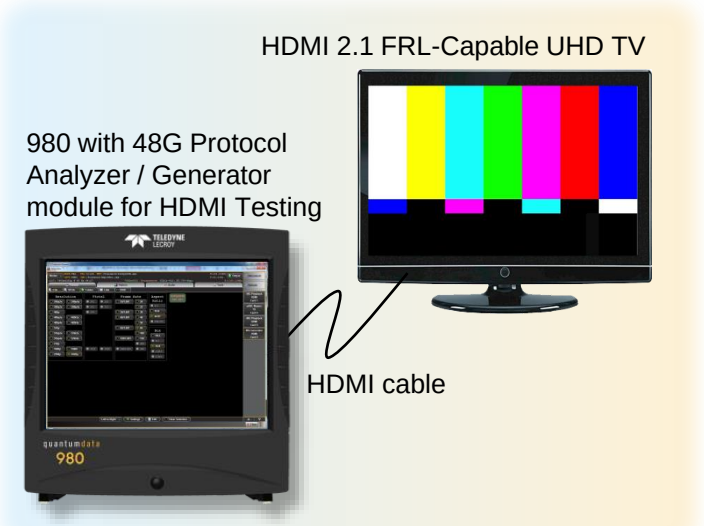
Auxiliary Channel Analyzer (Link Training over DDC)



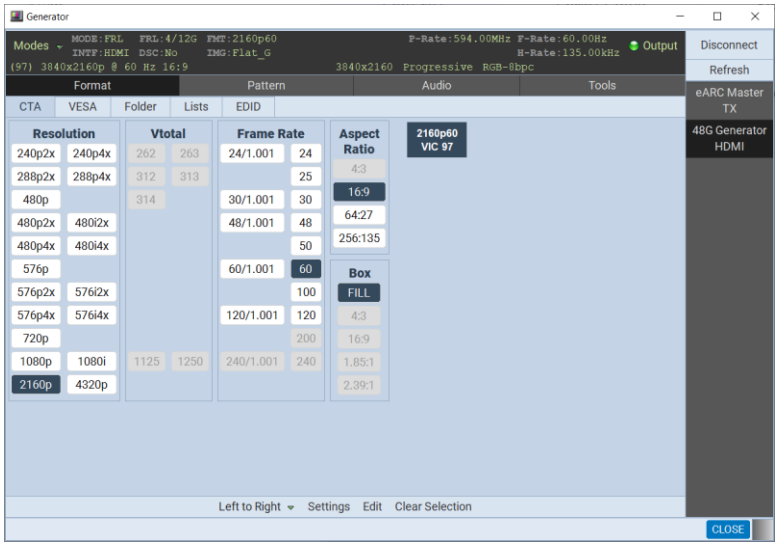
FIXED RATE LINK (FRL) VIDEO GENERATION

FRL Video Generation

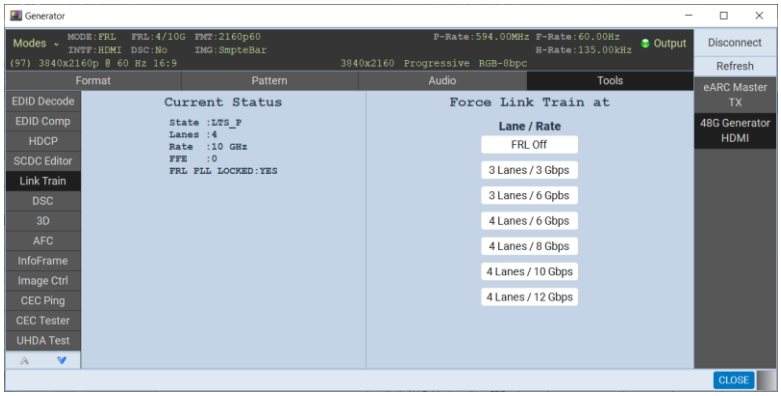
The 980 48G module for HDMI® Testing enables developers of HDMI and TMDS FRL-capable sink devices and silicon makers to run functional tests on their FRL-capable display devices by rendering uncompressed, unencrypted or encrypted FRL streams at up to 8K and 10K video resolutions at lane rates up to 12Gb/s and at an aggregate link rate of 48Gb/s. The enhanced video generator function enables specific selections of video formats, colorimetry, bit depth, chroma subsampling, color space and test patterns.



Selection of FRL and TMDS Video Resolutions



Link Training Configuration



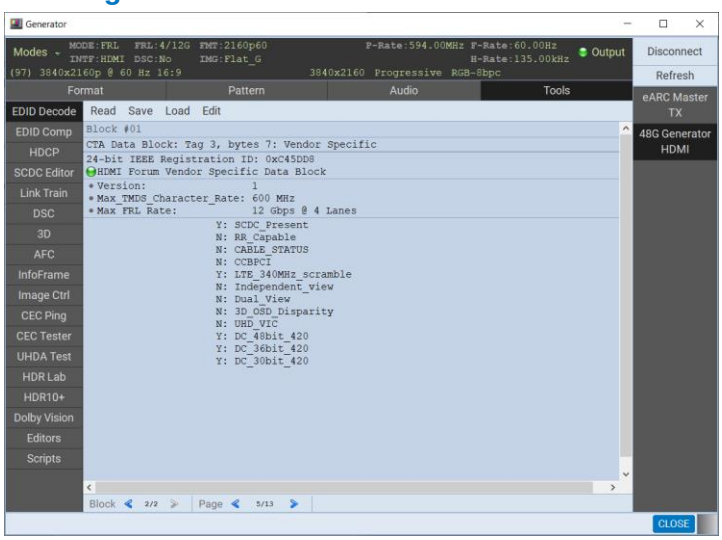
Link Training Configuration

The 980 48G Protocol Analyzer / Generator module ‘s video generation function enables you to configure the lane rate and number of lanes for transmission of the FRL stream.

EDID Read

The 980 48G Protocol Analyzer / Generator module enables you to view the EDID of the connected display (below). You can page through each block and save for later viewing.

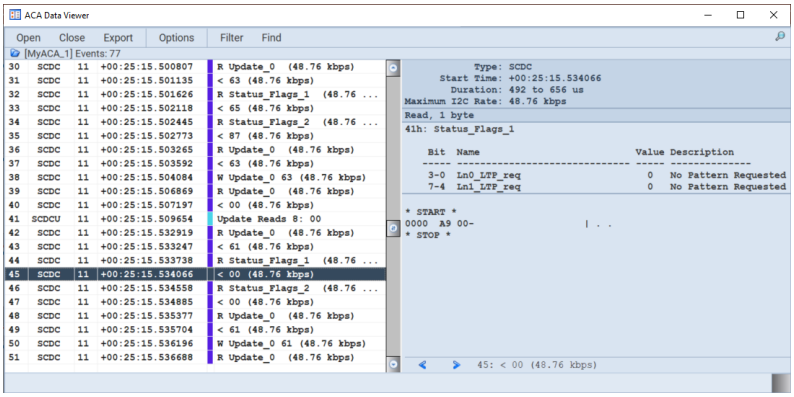
Reading the EDID



Auxiliary Channel Analyzer (ACA)

You can use the 980 48G Protocol Analyzer / Generator module to monitor the Link Training transactions—EDID exchange and reads and writes to the SCDC registers over the DDC channel--with the Aux Channel Analyzer utility. The FRL link training transactions enable developers to verify that their displays are properly conducting their role in the link training process.

Auxiliary Channel Analyzer (Link Training)

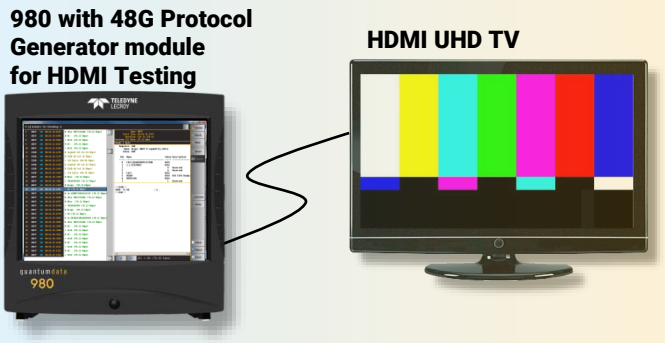


HDR FUNCTIONAL TESTING – HDR LAB, DOLBY VISION, HLG

HDR Lab

The "HDR Lab" test option was developed jointly with industry expert Joe Kane. HDR Lab is a suite of 4K and 8K test patterns and reference images for evaluating HDR10 displays (examples at right) that address the following:

- HDR End-to-End Validation in Post Production – Verifies HDR metadata, color grading and color decoding throughout the post production process.
- HDR Display Test Suite – Verifies various HDR attributes such as: peak brightness, native contrast, average brightness level, signal clipping, and color gamut on an HDR-capable UHD TV using a variety of test patterns.



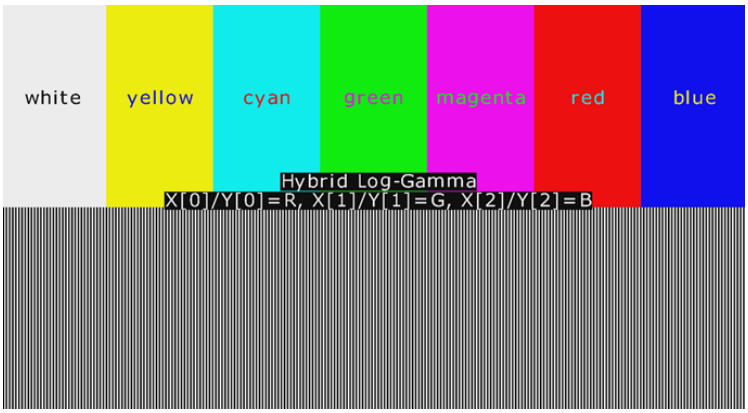
Setup for HDR Functional Tests

Dolby Vision & Hybrid Log Gamma Test Pattern

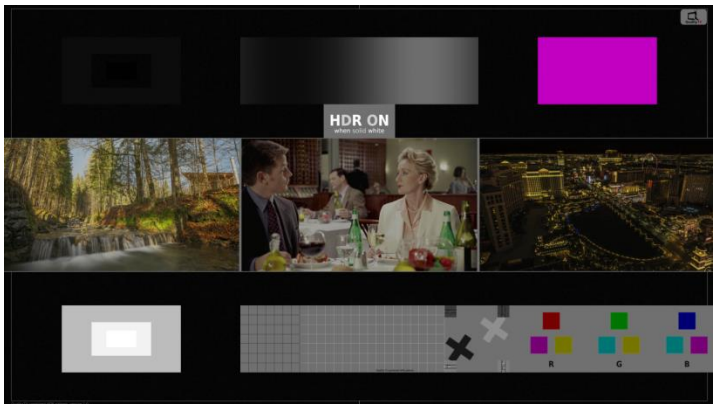
The Dolby Vision test image verifies a Dolby Vision display's Dolby Vision-specific EDID data, its response to the Dolby Vision protocol handshake and its handling of the Dolby Vision signal and metadata. The Dolby Vision test image will be rendered with a checkmark in the proper location if the display has properly interpreted the color space, metadata and checksum correctly.

The Hybrid Log Gamma (HLG) test image provides an assurance that the HLG metadata is not impeding the ability of the display to render the image.

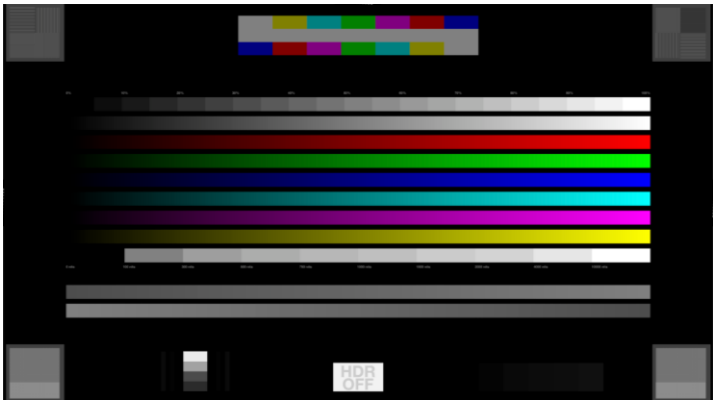
HLG Test Image



HDR Lab (Sample Test Pattern - Combination)

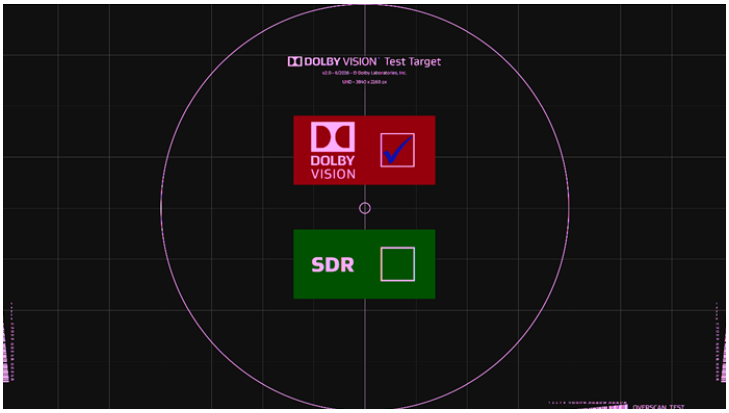


HDR Lab (Sample – Universal Test Pattern)



HDR Lab (Sample Test Pattern – Flower Montage)

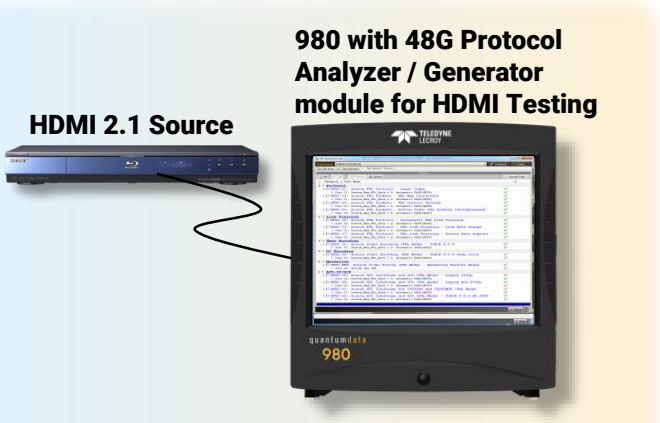
Dolby Vision Test Image



FIXED RATE LINK (FRL) SOURCE COMPLIANCE

FRL & DSC Source Compliance Testing

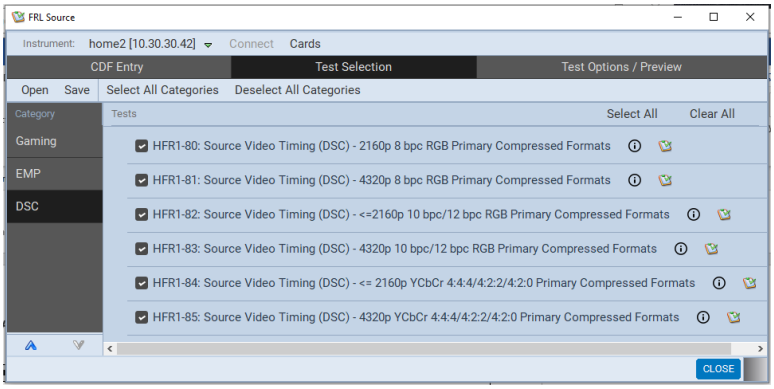
The 980 48G module for HDMI® Testing enables developers of HDMI FRL-capable source devices and silicon makers to run compliance tests on their FRL-capable source devices on unencrypted FRL streams at up to 8K and 10K video resolutions at lane rates up to 12Gb/s and at an aggregate link rate of 48Gb/s. All compliance test data, including the captured data, is exportable and can be disseminated to colleagues and other subject matter experts.



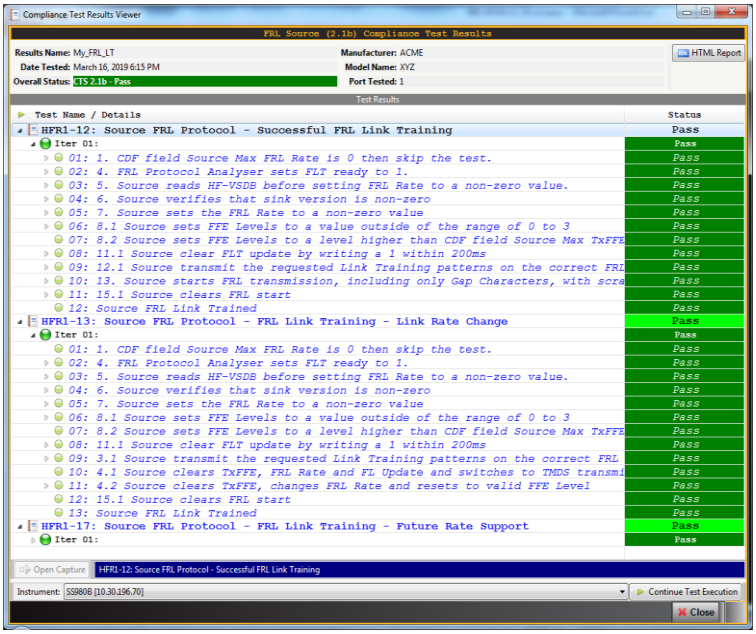
Test Setup for Source Test

Selection of FRL Source Compliance tests

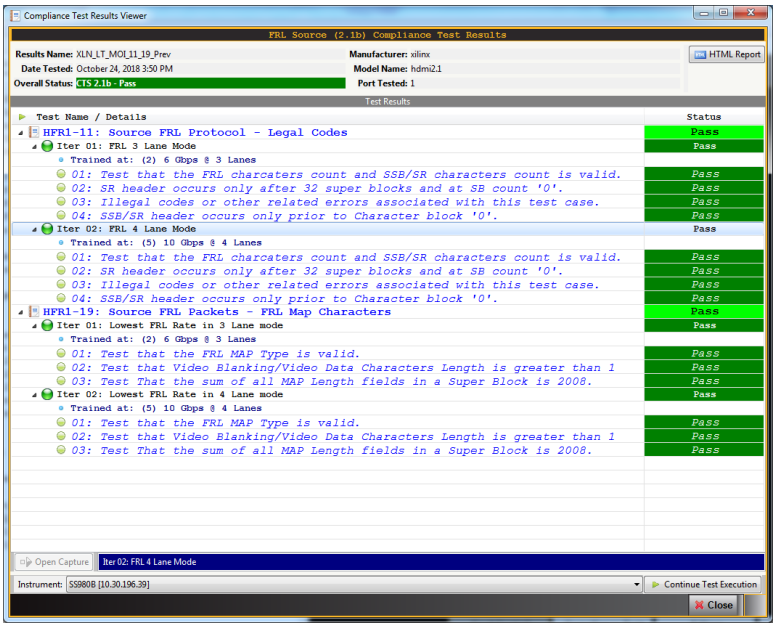
Selection of FRL DSC Source Compliance tests



Sample FRL Source Compliance (Link Training Tests)



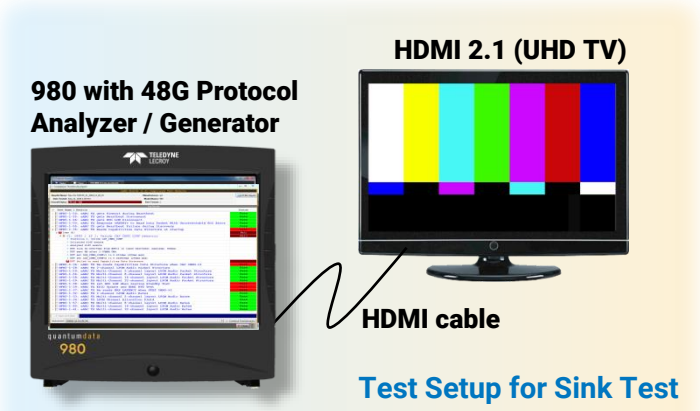
Sample FRL Source Compliance (Protocol Tests)



FIXED RATE LINK (FRL) & DSC SINK COMPLIANCE

FRL & DSC Sink Compliance Testing

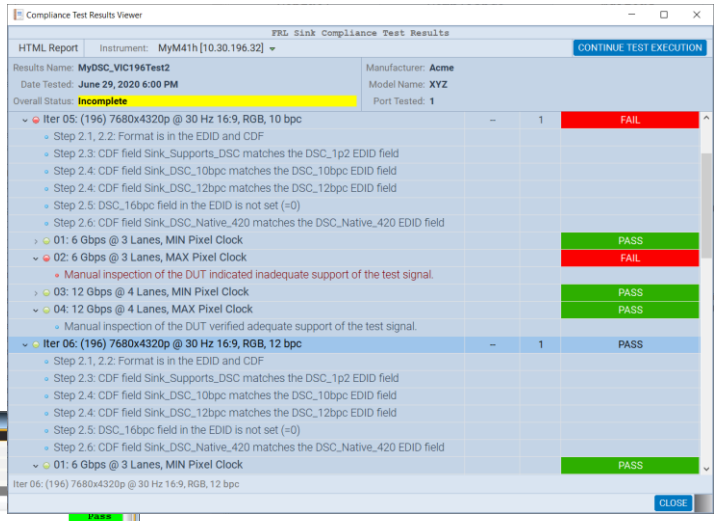
The M41h for HDMI Testing enables developers of HDMI® FRL and DSC-capable sink devices and silicon makers to run compliance tests on their FRL-capable sink devices with FRL streams at up to 8K and 10K video resolutions at lane rates up to 12Gb/s and at an aggregate link rate of 48Gb/s. All compliance test data, including the captured data, is exportable and can be disseminated to colleagues and other subject matter experts. The test patterns and formats necessary to run the DSC sink compliance tests are pre-cached for fast rendering.



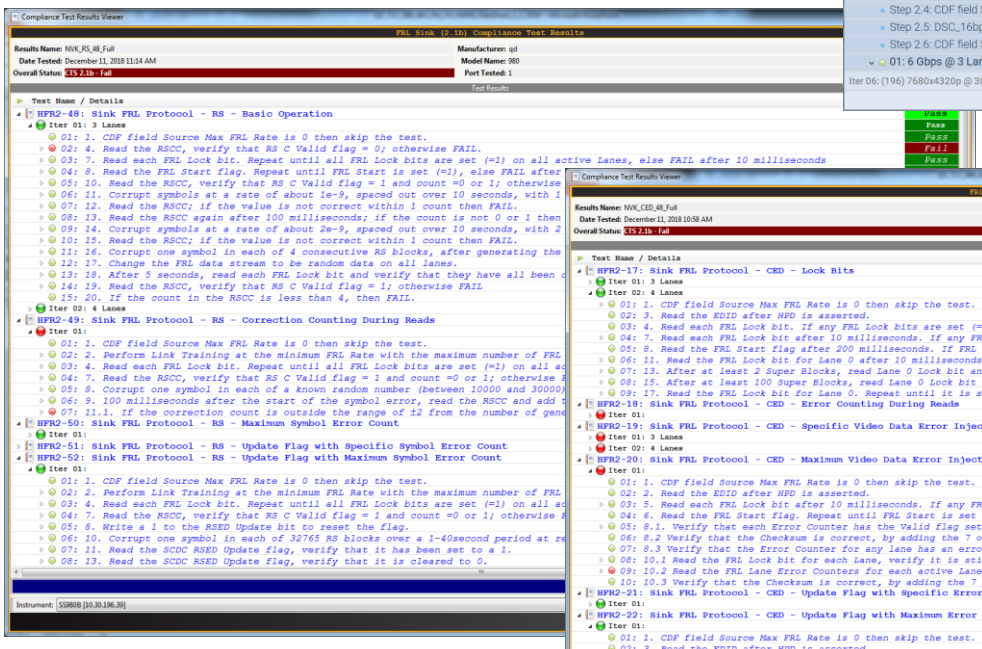
Test Setup for Sink Test

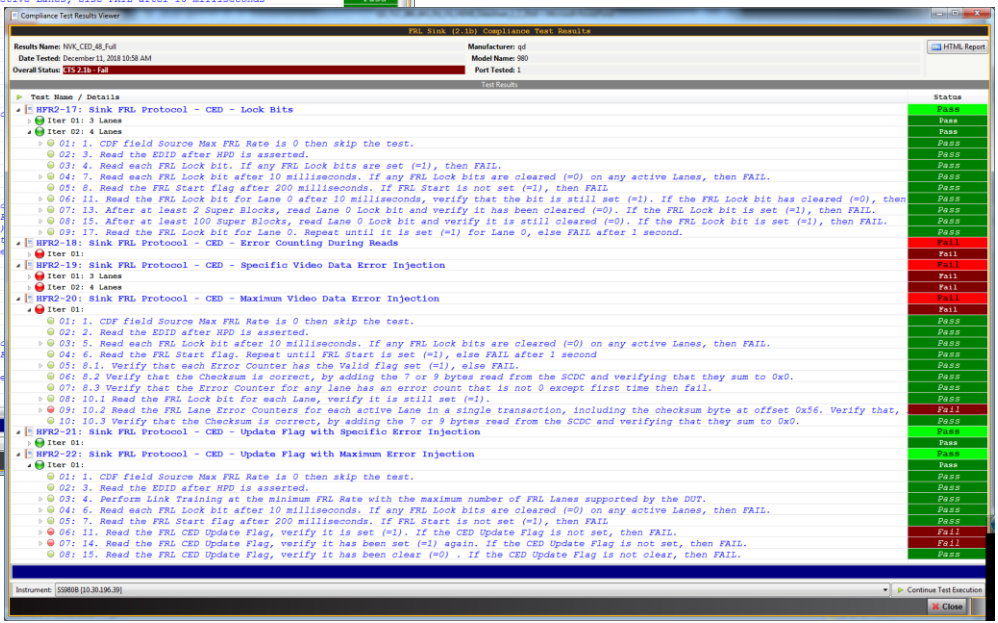
Selection of FRL Sink & DSC Compliance tests

Sample DSC Sink Compliance Test Results



Sample Test Results of FRL Sink Compliance tests

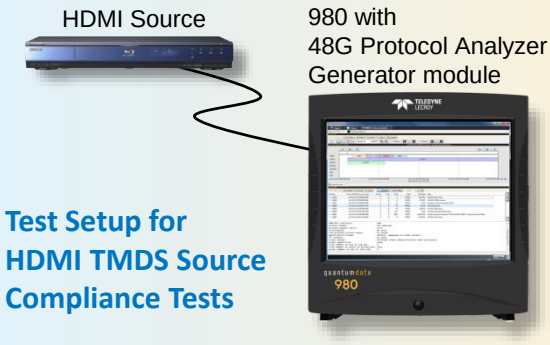




HDMI 2.0 / 1.4 SOURCE/SINK TMDS COMPLIANCE TESTS

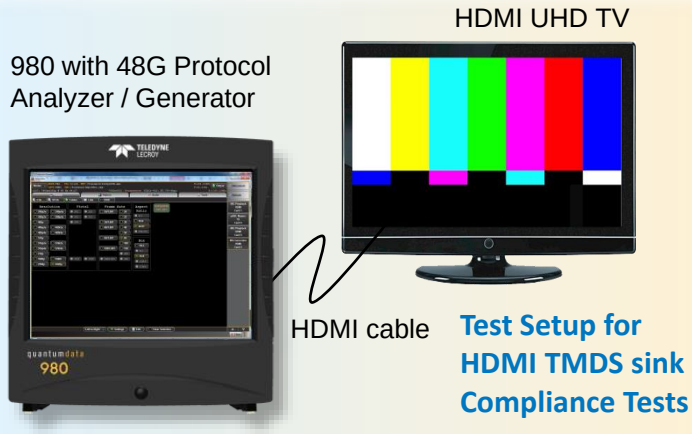
HDMI TMDS Source Compliance

The 980 48G module for HDMI® Testing enables developers of HDMI source devices and silicon makers to run compliance tests on their TMDS source devices on streams at up to 4K video resolutions. All compliance test data, including the captured data, is exportable and can be disseminated to colleagues and other subject matter experts. (Example screens below show samples only.)



HDMI TMDS Sink Compliance

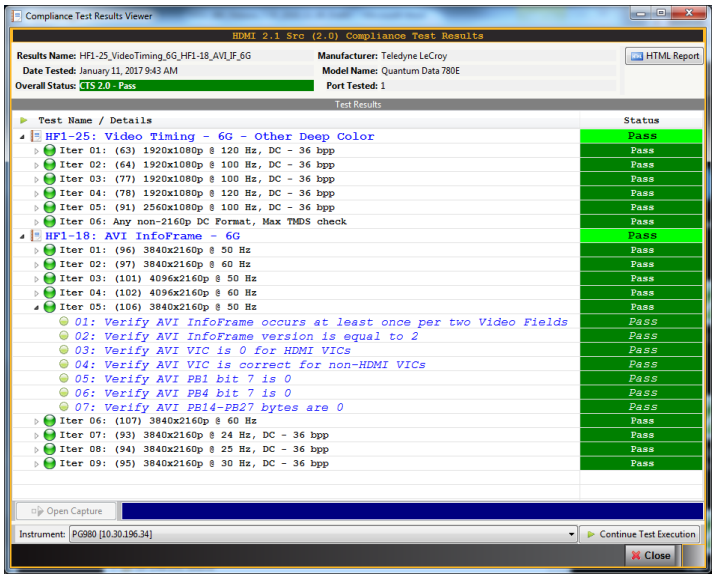
The 980 48G module for HDMI Testing enables developers of HDMI sink devices and silicon makers to run compliance tests on their TMDS sink devices at up to 4K video resolutions. All compliance test data, including the captured data, is exportable and can be disseminated to colleagues and other subject matter experts.



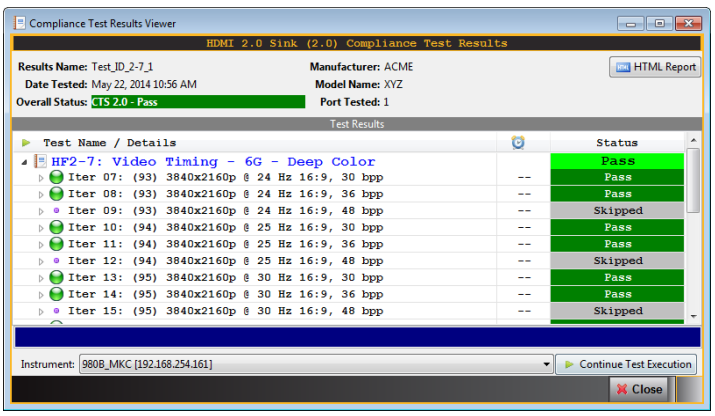
HDMI TMDS Source – Partial List of Supported Tests

HDMI TMDS Sink – Partial List of Supported Tests

HDMI TMDS Test Results – Video Tests



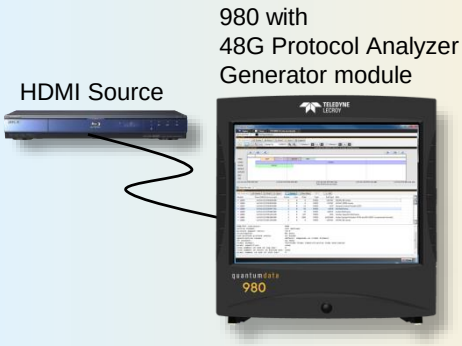
HDMI TMDS Test Results – Video Tests



HDCP 2.3 SOURCE, SINK, REPEATER COMPLIANCE TESTS

HDCP 2.3 Compliance (TMDS)

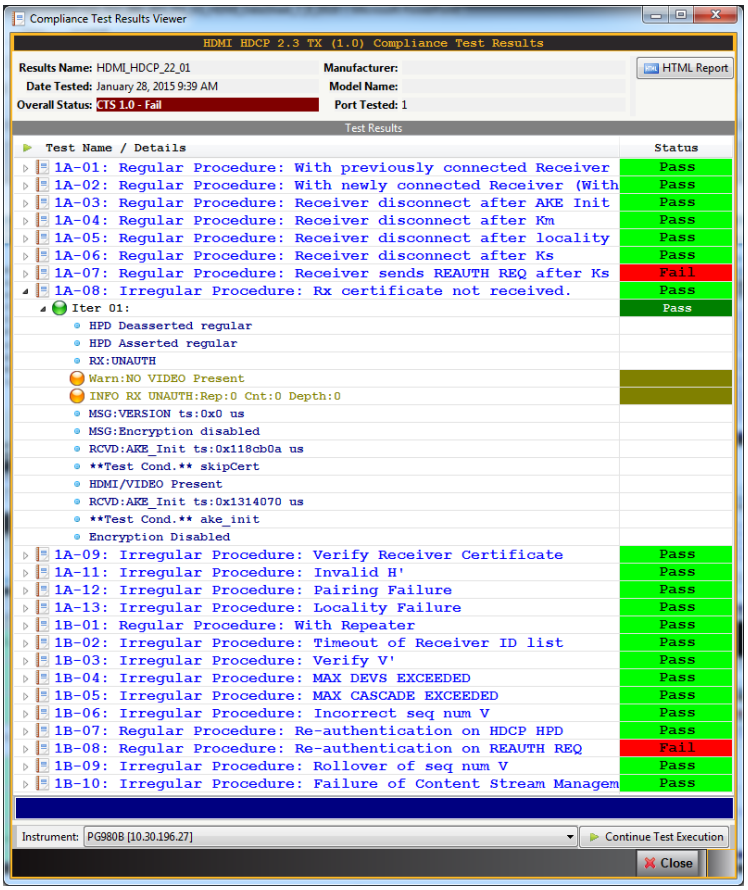
The 980 HDCP 2.3 compliance tests are ideal for pre-testing your HDMI® source, sink or repeater product prior to submission to an Authorized Test Center for approval. Pre-testing provides assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the auxiliary channel analyzer traces logged during the test to help diagnose the cause of compliance test failures. HDCP source test examples are shown.



Test Setup for HDCP Source Compliance Tests

HDCP 2.3 Test Selection – List of Source Tests

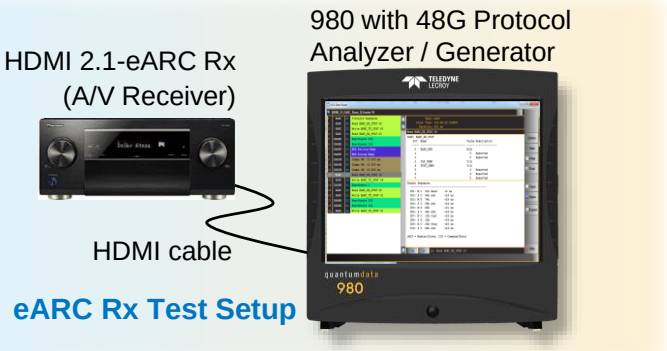
HDCP 2.3 Test Results– Source Tests



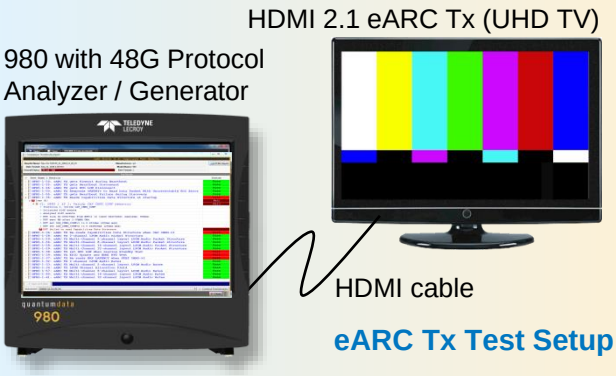
eARC FUNCTIONAL AND COMPLIANCE TESTING

eARC Functional Testing

The 980 48G module is also supports enhanced Audio Return Channel (eARC) Tx/Rx functional testing. The solution provides emulation of an eARC Tx and Rx functions over the eARC Common Mode and Differential mode data channels. Solution supports discovery and disconnect, heartbeat, status and capabilities data structure and transmission over the differential channel. (Sample screen showing monitoring incoming audio stream, right.)



eARC Rx Test Setup

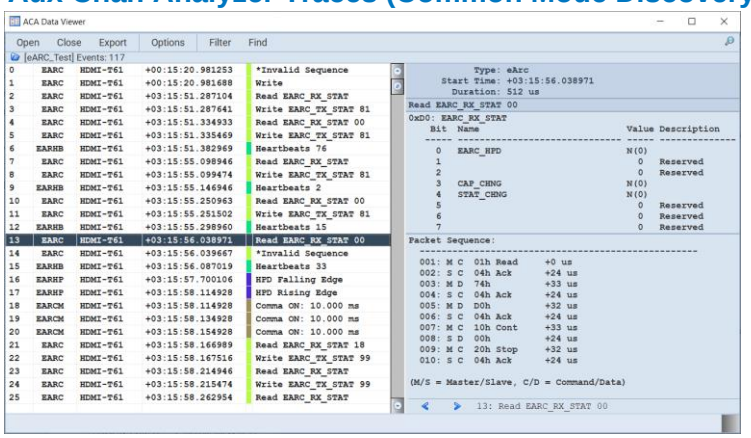


eARC Tx Test Setup

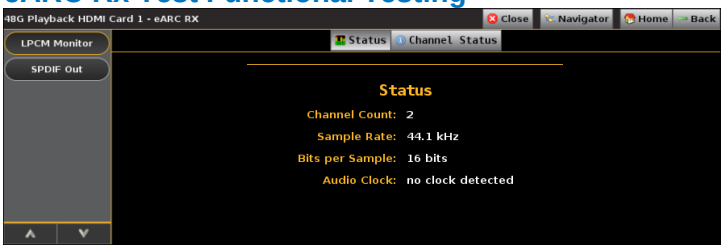
Auxiliary Channel Analyzer (ACA)

The 980 48G module can monitor the Link Training transactions—EDID exchange and reads and writes to the SCDC registers over the DDC channel -with the Aux Channel Analyzer (ACA) utility. Viewing the FRL link training transactions enables developers to verify their displays are properly conducting the link training process properly.

Aux Chan Analyzer Traces (Common Mode Discovery)

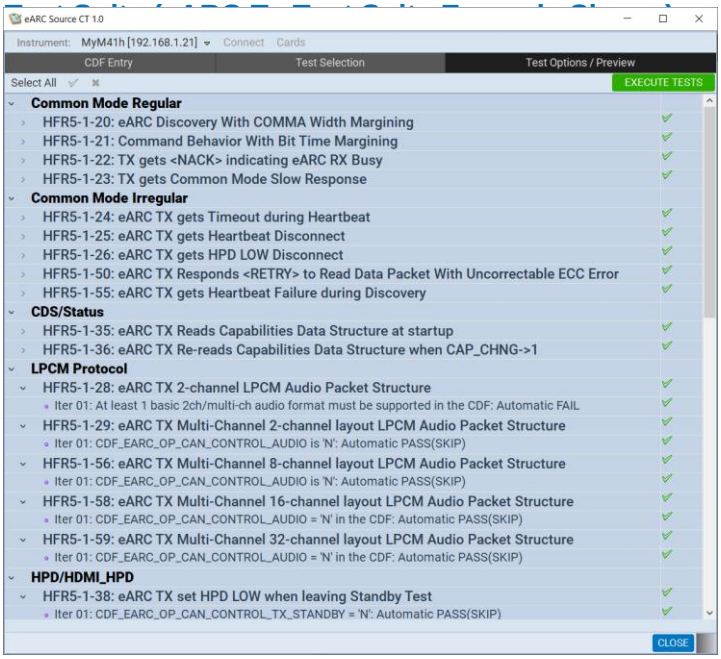


eARC Rx Test Functional Testing

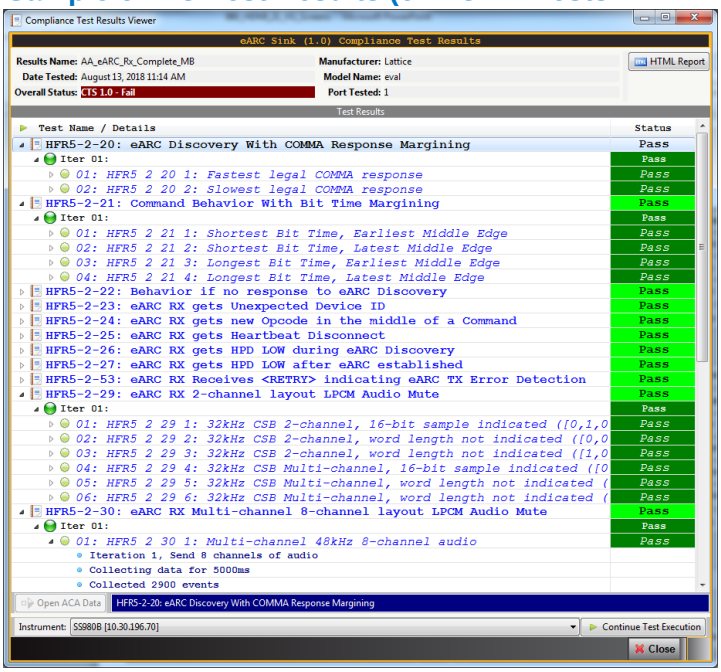


eARC Compliance Testing

The 980 48G module enables developers of HDMI® eARC Tx and Rx devices to run compliance tests on their eARC-capable. The compliance tests run with little or no human interaction. Detailed results are provided for each test to help identify the root cause of failures. The reports can be exported and disseminated to colleagues and other subject matter experts.



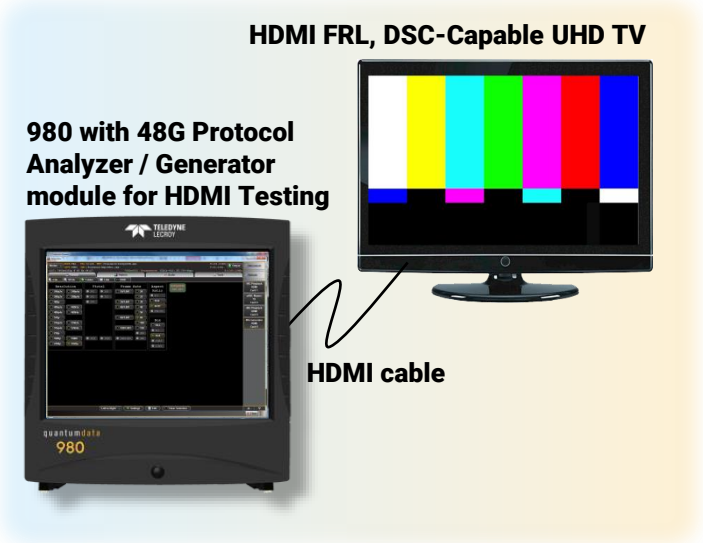
Sample eARC Test Results (eARC Rx Tests



DISPLAY STREAM COMPRESSION (DSC) TESTING

Display Stream Compression Video Generation

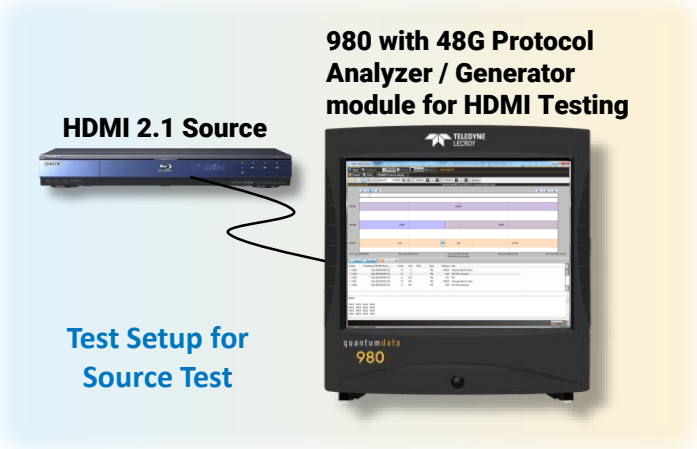
The 980 48G module enables developers of HDMI® DSC-capable sink devices and silicon makers to run Display Stream Compression (DSC) functional and compliance tests on their FRL-capable display devices by rendering compressed, unencrypted or encrypted FRL streams at up to 8K video resolutions at lane rates up to 12Gb/s. The test patterns and formats necessary to run the DSC sink compliance tests are pre-cached for fast rendering.



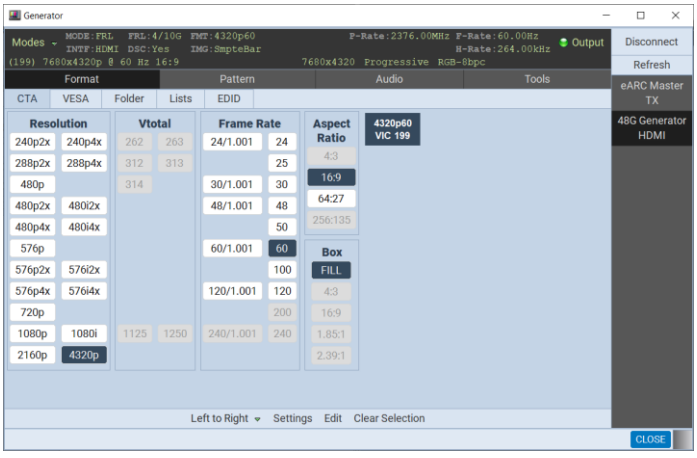
Display Stream Compression Video Analysis

The 980 48G module enables developers of HDMI DSC-capable source devices and silicon makers to run Display Stream Compression (DSC) functional and compliance tests on their FRL-capable source devices by rendering compressed, unencrypted or encrypted FRL streams at up to 8K video resolutions at lane rates up to 12Gb/s. There is a new "No Video" mode that enables you quickly verify the incoming DSC timing and metadata. You can then choose to view the uncompressed video frames.

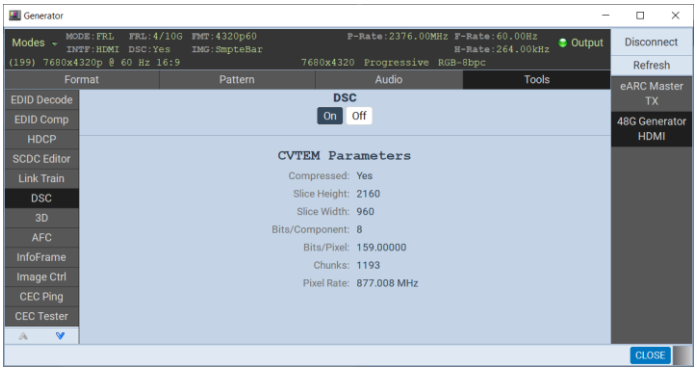
DSC Real Time Analysis



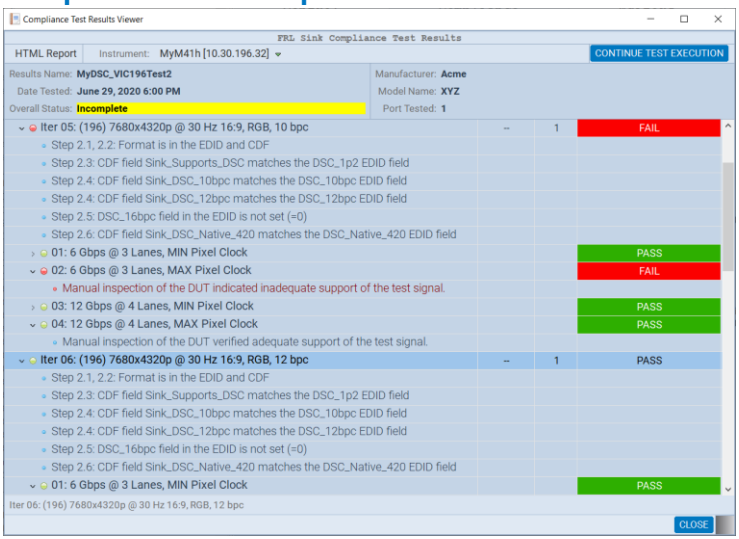
DSC Video Generation Selection



DSC Video Generation Setup



Sample DSC Sink Compliance Test Results



SPECIFICATIONS

HDMI Ports

Version	HDMI® 2.1a
Standard Formats	CEA, VESA
Connector	Rx HDMI Type A; Category 2 Tx HDMI Type A: Category 2 Note: Connectors are not approved Category 3 connectors
Protocols	FRL with FEC, DSC; HDCP 2.3, TMDS
FRL bit rates	3Gbps; 6Gbps; 8Gbps; 10Gbps; 12Gbps (48Gbps aggregate)
Max Reslution	Up to 8K and 10K with DSC compression
Line Code	16b/18b
HDCP	HDCP 1.4 and 2.3
Capture memory	8 GBytes

HDMI 2.1 Protocol Analyzer Features

Fixed Rate Link (FRL)	Captures and Decodes Fixed Rate Link (FRL) and FEC data streams
Forward Error Correction	Displays FEC packets in FRL Character Blocks
FRL Lanes	3 & 4 lane configurations are supported
FRL Link Training Patterns	Supports LTP5 through LTP8
FRL Link Training	Supports link training with an FRL source in accordance with states defined in the HDMI 2.1 specification

HDMI 2.1 Video Generator Features

Fixed Rate Link (FRL)	Transmits Fixed Rate Link (FRL), FEC data streams and TMDS streams.
FRL Lanes	3 & 4 lane configurations are supported
FRL Link Training Patterns	Supports LTP5 through LTP8
FRL Link Training	Supports link training with an FRL sink in accordance with states defined in the HDMI 2.1 specification

HDMI 2.1 Module Options

Video Generator license	Transmits Fixed Rate Link (FRL) and FEC data streams and TMDS streams
Protocol Analysis license	Analyzes Fixed Rate Link (FRL) and FEC data streams and TMDS streams
Passive DDC monitoring	Passive DDC monitoring in FRL mode (requires custom cable)
Functional test for HDR Lab	HDR Lab test patterns and images for testing HDR10 updated for 8K
Functional test for eARC Tx	Emulate eARC Rx to run tests on an eARC Tx common & differential modes
Functional test for eARC Rx	Emulate eARC Tx to run tests on an eARC Rx common & differential modes
Compliance for eARC Tx	Run full compliance test on an eARC Tx (all tests supported) **Note**: HF5-1-51 test requires 980 18G Video Generator which has been discontinued
Compliance for eARC Rx	Run full compliance test on an eARC Rx (all tests supported)
Functional & Comp. DSC source tests	Run functional & compliance tests for Display Stream Compression sources
Functional & Compliance DSC sink	Run functional & compliance tests for Display Stream Compression sinks
Compliance FRL sources	Run full suite of FRL source compliance tests.
Compliance FRL & DSC sinks	Run full suite of FRL & DSC sink compliance tests
Compliance TMDS sources	Run full suite of TMDS source compliance tests
Compliance TMDS sink	Run full suite of TMDS sink compliance tests
Compliance HDCP 1.4 sources	Run full suite of HDCP 1.4 source compliance tests
Compliance HDCP 2.3 sinks	Run full suite of HDCP 2.3 sink compliance tests
Compliance HDCP 2.3 sources	Run full suite of HDCP 2.3 source compliance tests
Compliance HDCP 2.3 repeater	Run full suite of HDCP 2.3 repeater compliance tests

980B Test Platform

Embedded Display	15" diagonal; Resolution: 1024(H); x 768 (V) resolution; 24-bit RGB color
Power	90-264 VAC, 47-63Hz
Weight	23.76 LBS; 10.78 Kg
Size	Height: 15.25 in. (38.7 cm) Width: 14.57 in. (36.5 cm) Depth: 6.29 in. (15.9 cm)
Command Line Control	Ethernet (RJ-45) for external GUI and telnet
Environmental	Operating Temp: 32 to 90 (F); 0 to 32 (C)

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