MU195020A
21G/32G bit/s SI PPG
MU195040A
21G/32G bit/s SI ED
MU195050A
Noise Generator
Operation Manual

11th Edition

- **For safety and warning information, please read this manual before attempting to use the equipment.**
- **Additional safety and warning information is provided within the MP1900A Signal Quality Analyzer-R Operation Manual. Please also refer to it before using the equipment.**
- **Keep this manual with the equipment.**

ANRITSU CORPORATION

Document No.: M-W3915AE-11.0

Safety Symbols

To prevent the risk of personal injury or loss related to equipment malfunction, Anritsu Corporation uses the following safety symbols to indicate safety-related information. Ensure that you clearly understand the meanings of the symbols BEFORE using the equipment. Some or all of the following symbols may be used on all Anritsu equipment. In addition, there may be other labels attached to products that are not shown in the diagrams in this manual.

Symbols used in manual

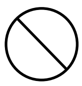
⚠ DANGER This indicates a very dangerous procedure that could result in serious injury or death if not performed properly.

⚠ WARNING This indicates a hazardous procedure that could result in serious injury or death if not performed properly.

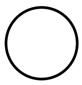
⚠ CAUTION This indicates a hazardous procedure or danger that could result in light-to-severe injury, or loss related to equipment malfunction, if proper precautions are not taken.

Safety Symbols Used on Equipment and in Manual

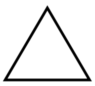
The following safety symbols are used inside or on the equipment near operation locations to provide information about safety items and operation precautions. Ensure that you clearly understand the meanings of the symbols and take the necessary precautions BEFORE using the equipment.



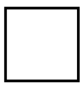
This indicates a prohibited operation. The prohibited operation is indicated symbolically in or near the barred circle.



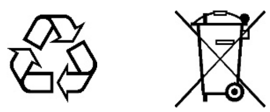
This indicates an obligatory safety precaution. The obligatory operation is indicated symbolically in or near the circle.



This indicates a warning or caution. The contents are indicated symbolically in or near the triangle.



This indicates a note. The contents are described in the box.



These indicate that the marked part should be recycled.

MU195020A 21G/32G bit/s SI PPG
MU195040A 21G/32G bit/s SI ED
MU195050A Noise Generator Operation Manual

19 June 2017 (First Edition)
5 March 2021 (11th Edition)

Equipment Certificate

Anritsu Corporation certifies that this equipment was tested before shipment using calibrated measuring instruments with direct traceability to public testing organizations recognized by national research laboratories, including the National Institute of Advanced Industrial Science and Technology, and the National Institute of Information and Communications Technology, and was found to meet the published specifications.

Anritsu Warranty

Anritsu Corporation will repair this equipment free-of-charge if a malfunction occurs within one year after shipment due to a manufacturing fault, and software bug fixes will be performed in accordance with the separate Software End-User License Agreement, provide, however, that Anritsu Corporation will deem this warranty void when:

- The fault is outside the scope of the warranty conditions separately described in the operation manual.
- The fault is due to mishandling, misuse, or unauthorized modification or repair of the equipment by the customer.
- The fault is due to severe usage clearly exceeding normal usage.
- The fault is due to improper or insufficient maintenance by the customer.
- The fault is due to natural disaster, including fire, wind or flood, earthquake, lightning strike, or volcanic ash, etc.
- The fault is due to damage caused by acts of destruction, including civil disturbance, riot, or war, etc.
- The fault is due to explosion, accident, or breakdown of any other machinery, facility, or plant, etc.
- The fault is due to use of non-specified peripheral or applied equipment or parts, or consumables, etc.
- The fault is due to use of a non-specified power supply or in a non-specified installation location.
- The fault is due to use in unusual environments(Note).
- The fault is due to activities or ingress of living organisms, such as insects, spiders, fungus, pollen, or seeds.

In addition, this warranty is valid only for the original equipment purchaser. It is not transferable if the equipment is resold.

Anritsu Corporation shall assume no liability for damage or financial loss of the customer due to the use of or a failure to use this equipment, unless the damage or loss is caused due to Anritsu Corporation’s intentional or gross negligence.

Note:
For the purpose of this Warranty, "unusual environments" means use:

- In places of direct sunlight
- In dusty places
- Outdoors
- In liquids, such as water, oil, or organic solvents, and medical fluids, or places where these liquids may adhere
- In salty air or in place chemically active gases (sulfur dioxide, hydrogen sulfide, chlorine, ammonia, nitrogen dioxide, or hydrogen chloride etc.) are present
- In places where high-intensity static electric charges or electromagnetic fields are present
- In places where abnormal power voltages (high or low) or instantaneous power failures occur
- In places where condensation occurs
- In the presence of lubricating oil mists
- In places at an altitude of more than 2,000 m
- In the presence of frequent vibration or mechanical shock, such as in cars, ships, or airplanes

Anritsu Corporation Contact

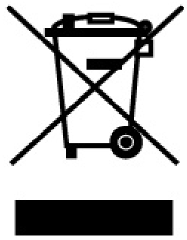
In the event of this equipment malfunctions, please contact an Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file on the PDF version.

Notes On Export Management

This product and its manuals may require an Export License/Approval by the Government of the product's country of origin for re-export from your country.
Before re-exporting the product or manuals, please contact us to confirm whether they are export-controlled items or not.
When you dispose of export-controlled items, the products/manuals need to be broken/shredded so as not to be unlawfully used for military purpose.

Crossed-out Wheeled Bin Symbol

Equipment marked with the Crossed-out Wheeled Bin Symbol complies with council directive 2012/19/EU (the “WEEE Directive”) in European Union.



For Products placed on the EU market after August 13, 2005, please contact your local Anritsu representative at the end of the product's useful life to arrange disposal in accordance with your initial contract and the local law.

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Please carefully read and accept this Software End-User License Agreement (hereafter this EULA) before using (includes executing, copying, installing, registering, etc.) this Software (includes programs, databases, scenarios, etc., used to operate, set, etc., Anritsu electronic equipment, etc.). By using this Software, you shall be deemed to have agreed to be bound by the terms of this EULA, and Anritsu Corporation (hereafter Anritsu) hereby grants you the right to use this Software with the Anritsu specified equipment (hereafter Equipment) for the purposes set out in this EULA.

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3. You are not permitted to reverse engineer, disassemble, decompile, modify or create derivative works of this Software.
4. This EULA allows you to install one copy of this Software on one piece of Equipment.

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To the extent not prohibited by law, in no event shall Anritsu be liable for direct, or any incidental, special, indirect or consequential damages whatsoever, including, without limitation, damages for loss of profits, loss of data, business interruption or any other commercial damages or losses, and damages claimed by third parties, arising out of or related to your use or inability to use this Software, unless the damages are caused due to Anritsu's intentional or gross negligence.

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1. If a fault (bug) is discovered in this Software, failing this Software to operate as described in the operation manual or specifications even though you have used this Software as described in the manual, Anritsu shall at its own discretion, fix the bug, or replace the software, or suggest a workaround, free-of-charge, provided, however, that the faults caused by the following items and any of your lost or damaged data whatsoever shall be excluded from repair and the warranty.
   - i) If this Software is deemed to be used for purposes not described in the operation manual or specifications.
   - ii) If this Software has been used in conjunction with other non-Anritsu-approved software.
   - iii) If this Software or the Equipment has been modified, repaired, or otherwise altered without Anritsu's prior approval.
   - iv) For any other reasons out of Anritsu's direct control and responsibility, such as but not limited to, natural disasters, software virus infections, or any devices other than this Equipment, etc.
2. Expenses incurred for transport, hotel, daily allowance, etc., for on-site repairs or replacement by Anritsu engineers necessitated by the above faults shall be borne by you.
3. The warranty period for faults listed in Section 1 of this Article shall be either 6 months from the date of purchase of this Software or 30 days after the date of repair or replacement, whichever is longer.

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You shall not use or otherwise export or re-export directly or indirectly this Software except as authorized by the laws and regulations of Japan and the United States, etc. In particular, this Software shall not be exported or re-exported (a) into any Japan or US embargoed countries or (b) to anyone restricted by the Japanese export control regulations, or the US Treasury Department's list of Specially Designated Nationals or the US Department of Commerce Denied Persons List or Entity List. In using this Software, you warrant that you are not located in any such embargoed countries or on any such lists. You also agree that you will not use or otherwise export or re-export this Software for any purposes prohibited by the Japanese and US laws and regulations, including, without limitation, the development, design and manufacture or production of missiles or nuclear, chemical or biological weapons of mass destruction, and conventional weapons.

Article 5. Change of Terms

Anritsu may change without your approval the terms of this EULA if the changes are for the benefit of general customers, or are reasonable in light of the purpose of this EULA and circumstances of the changes. At the time of change, Anritsu will inform you of those changes and its effective date, as a general rule 45 days, in advance on its website, or in writing or by e-mail.

Article 6. Termination

1. Anritsu may terminate this EULA immediately if you violate any conditions described herein. This EULA shall also be terminated immediately by Anritsu if there is any good reason that it is deemed difficult to continue this EULA, such as your violation of Anritsu copyrights, patents, etc. or any laws and ordinances, or if it turns out that you belong to an antisocial organization or has a socially inappropriate relationship with members of such organization.
2. You and Anritsu may terminate this EULA by a written notice to the other party 30 days in advance.

Article 7. Damages

If Anritsu suffers any damages or loss, financial or otherwise, due to your violation of the terms of this EULA, Anritsu shall have the right to seek proportional damages from you.

Article 8. Responsibility after Termination

Upon termination of this EULA in accordance with Article 6, you shall cease all uses of this Software immediately and shall as directed by Anritsu either destroy or return this Software and any backup copies, full or partial, to Anritsu.

Article 9. Negotiation for Dispute Resolution

If matters of interpretational dispute or items not covered under this EULA arise, they shall be resolved by negotiations in good faith between you and Anritsu.

Article 10. Governing Law and Court of Jurisdiction

This EULA shall be governed by and interpreted in accordance with the laws of Japan without regard to the principles of the conflict of laws thereof, and any disputes arising from or in relation to this EULA that cannot be resolved by negotiation described in Article 9 shall be subject to and be settled by the exclusive agreed jurisdiction of the Tokyo District Court of Japan.

Revision History:

February 29th, 2020

CE Conformity Marking

Anritsu affixes the CE conformity marking on the following product(s) in accordance with the Decision 768/2008/EC to indicate that they conform to the EMC, LVD and RoHS directive of the European Union (EU).

CE marking

1. Product Model

Plug-in Units: MU195020A 21G/32G bit/s SI PPG
MU195040A 21G/32G bit/s SI ED
MU195050A Noise Generator PG

2. Applied Directive and Standards

When the MU195020A 21G/32G bit/s SI PPG, MU195040A 21G/32G bit/s SI ED, and MU195050A Noise Generator PG are installed in the MP1900A, the applied directive and standards of this unit conform to those of the MP1900A main frame.

PS: About main frame
Please contact Anritsu for the latest information on the main frame types that MU195020A, MU195040A, and MU195050A can be used with.

RCM Conformity Marking

Anritsu affixes the RCM mark on the following product(s) in accordance with the regulation to indicate that they conform to the EMC framework of Australia/New Zealand.

RCM marking

1. Product Model

Plug-in Units: MU195020A 21G/32G bit/s SI PPG
MU195040A 21G/32G bit/s SI ED
MU195050A Noise Generator PG

2. Applied Directive and Standards

When the MU195020A 21G/32G bit/s SI PPG, MU195040A 21G/32G bit/s SI ED, and MU195050A Noise Generator PG are installed in the MP1900A, the applied directive and standards of this unit conform to those of the MP1900A main frame.

PS: About main frame
Please contact Anritsu for the latest information on the main frame types that MU195020A, MU195040A, and MU195050A can be used with.

About This Manual

A testing system combining an MP1900A Signal Quality Analyzer-R, module(s), and control software is called a Signal Quality Analyzer-R Series. The operation manuals of the Signal Quality Analyzer-R Series consist of separate documents for the MP1900A, module(s), and control software, as shown below.

Configuration of Signal Quality Analyzer-R Series Operation

(shaded box) indicates this document.

- MP1900A Signal Quality Analyzer-R Operation Manual
  Describes the basic operations, panel details, and maintenance of the MP1900A, as well as the steps from module installation to the start of use.
- Module Operation Manual
  - MU195020A 21G/32G bit/s SI PPG MU195040A 21G/32G bit/s SI ED MU195050A Noise Generator Operation Manual
    Describes the panel details, how to operate, performance test, maintenance, and troubleshooting of the module to be installed on the MP1900A.
  - MU196020A PAM4 PPG MU196040A PAM4 ED MU196040B PAM4 ED Operation Manual
    Describes the panel details, performance test, maintenance, and troubleshooting of the MU196020A, MU196040A, and MU196040B.
  - MU181000A 12.5GHz Synthesizer MU181000B 12.5GHz 4 port Synthesizer Operation Manual
    Describes the panel details, how to operate, performance test, maintenance, and troubleshooting of the MU181000A and MU181000B.
  - MU181500B Jitter Modulation Source Operation Manual
    Describes the panel details, how to operate, performance test and maintenance of the MU181500B.
  - MU183020A 28G/32G bit/s PPG MU183021A 28G/32G bit/s 4ch PPG Operation Manual
    Describes the panel details, performance test, maintenance, and troubleshooting of the MU183020A and MU183021A.
  - MU183040A 28G/32G bit/s ED MU183041A 28G/32G bit/s 4ch ED MU183040B 28G/32G bit/s High Sensitivity ED MU183041B 28G/32G bit/s 4ch High Sensitivity ED Operation Manual
    Describes the panel details, how to operate, performance test, maintenance, and troubleshooting of the MU183040A, MU183041A, MU183040B, and MU183041B.

Configuration of Signal Quality Analyzer-R Series Operation (Cont'd)

indicates this document.

MX190000A Signal Quality Analyzer-R Control Software Operation Manual

Describes the operation of the software that controls the Signal Quality Analyzer-R Series.

Extended Application Operation Manual

Describes the operation of the extended application for the Signal Quality Analyzer-R Series.

MX183000A High-Speed Serial Data Test Software Operation Manual

Describes the setup and operating procedure of MX183000A.

Table of Contents

Chapter 1 Overview

This chapter describes the overview of the following modules.

- MU195020A 21G/32G bit/s SI PPG (hereafter, MU195020A)
- MU195040A 21G/32G bit/s SI ED (hereafter, MU195040A)
- MU195050A Noise Generator (hereafter, MU195050A)

1.1 Product Overview

The MU195020A, MU195040A, and MU195050A (hereinafter "MP1900A modules") are plug-in modules that can be built into the MP1900A Signal Quality Analyzer-R. The MP1900A modules support the error measurements of PRBS, DATA, Zero-Substitution, and Mixed patterns within the operating frequency range. The combination of MU195020A and MU195050A can generate data to which common mode noise, differential mode noise, and white noise are added. The data is optimal for signal integrity evaluation.
Various option configurations are available for the MP1900A modules. This module is therefore useful for research, development, and production of various types of digital communication equipment, modules, and devices.

The features of the MP1900A modules are as follows:

MU195020A features

- Capable of generating PRBS, DATA, Zero-Substitution, Mixed, PAM4, and Sequence patterns.
- MU195020A-x20 allows channel combination between two channels inside the module (Channel Combination).
  This function enables the generation of multiplexing signal by using Multiplexer (MUX) .
- Multiple MU195020As installed in MP1900A allow channel combination between channels.
  This function allows generating synchronous data corresponding to the applications that require Multi Channel.
- Capable of signal integrity evaluation using 10TAP Emphasis (MU195020A-x11/x21).
- Capable of adding variable ISI using 10TAP Emphasis (MU195020A-x40/x41).

MU195040A features

- Capable of measuring PRBS, Data, Zero-Substitution, Mixed, PAM4, and HSSB Data patterns.
- Provides a large amount of user-programmable patterns (256 Mbits)
- Installing MU195040A-x20 allows 32 Gbit/s data input up to 2ch and enables evaluation of 64 Gbit/s serial communication.
- With input sensitivity of Typ. 25 mVp-p, the MU195040A is the best for signal evaluation.
- Installing MU195040A-x22 enables clock recovery or clock and data recovery.
- Installing MU195040A-x11/x21 enables loss signal evaluation using CTLE (Continues Time Linear Equalizer).

MU195050A features

- Capability of adding common mode noise and/or differential mode noise to input data and outputting it
- Installing MU195050A-x01 enables adding white noise with a band of 10 MHz to 10 GHz.

1.2 Product Configuration

1.2.1 Standard configuration

Table 1.2.1-1, Table 1.2.1-2, and Table 1.2.1-3 below show the standard configurations of the three MP1900A modules respectively.

Table 1.2.1-1 Standard Configuration of MU195020A

Item	Model name/symbol	Product name	Q'ty	Remarks
Mainframe	MU195020A	21G/32G bit/s SI PPG	1	
Accessories	J1632A	Terminator	5	Clock Output, Aux Output × 2, Gating Output × 2
	J1341A	Open	2	Ext Clock Input, AUX Input
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	1	Clock Output
	J1717A	Coaxial Adaptor (SMA-P, SMA-J)	6	Ext Clock Input, Aux Output × 2, Gating Output × 2, AUX Input
	When the MU195020A-x10 is installed:			
	J1632A	Terminator	2	Data Output × 2
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	2	Data Output × 2
	When the MU195020A-x20 is installed:			
	J1632A	Terminator	4	Data Output × 4
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	4	Data Output × 4

Table 1.2.1-2 Standard Configuration of MU195040A

Item	Model name/symbol	Product name	Q'ty	Remarks
Mainframe	MU195040A	21G/32G bit/s SI ED	1	
Accessories	J1632A	Terminator	2	Aux Output × 2,
	J1341A	Open	2	Ext Clock Input
	J1717A	Coaxial Adaptor (SMA-P, SMA-J)	4	Ext Clock Input, Aux Output × 2, AUX Input
	When the MU195040A-x10 is installed:			
	J1341A	Open	2	Data Input × 2, AUX Input
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	2	Data Input × 2 (Supplied separately from the mainframe)
	41KC-6	Precision Fixed Attenuator 6 dB	2	Data Input × 2 (Installed on the mainframe at factory)
	When the MU195040A-x20 is installed:			
	J1341A	Open	4	Data Input × 4, AUX Input
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	4	Data Input × 4 (Supplied separately from the mainframe)
	41KC-6	Precision Fixed Attenuator 6 dB	4	Data Input × 4 (Installed on the mainframe at factory)

Table 1.2.1-3 Standard Configuration of MU195050A

Item	Model name/symbol	Product name	Q'ty	Remarks
Mainframe	MU195050A	Noise Generator	1	
Accessories	J1632A	Terminator	4	Data Output × 4*1
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	4	Data Output × 4*2
	J1717A	Coaxial Adaptor (SMA-P, SMA-J)	2	External Input*2
	J1341A	Open	6	Data Input × 4*1 External Input × 2*1
	J1746A	Skew match pair semirigid cable (K connector, Data Input1)	1 set	Data Input1 × 2*3
	J1747A	Skew match pair semirigid cable (K connector, Data Input2)	1 set	Data Input2 × 2*4
	J1792A	Skew match pair semirigid cable (V-K connector, Data Input1)	1 set	Data Input1 × 2*5

*1: Installed on MU195050A at factory.

*2: It is recommended to keep it connected to the MU195020A connector.

*3: Semi rigid cable to connect Data Output1 of MU195020A and Data Input1 of MU195050A at the shortest length.

*4: Semi rigid cable to connect Data Output2 of MU195020A and Data Input2 of MU195050A at the shortest length.

*5: Semi rigid cable to connect Data Output of MU196020A PAM4 PPG and Data Input1 of MU195050A at the shortest length.

1.2.2 Options

Table 1.2.2-1, Table 1.2.2-2, and Table 1.2.2-3 show the options for the MP1900A modules . All options are sold separately.

Note:

Option name format is as follows:

MU195020A-x x x

Indicates function.
This value is recognized by the MP1900A.

Anritsu management number.
This value is not recognized by the mainframe.

0: Installed at time of shipping
1: Retro-fitted option.
   Must be returned to Anritsu (Japan) when installing.
2: Retro-fitted option.
   Must be returned to an Anritsu Service and Sales office when installing.
3: Retro-fitted option.
   The user can install the option.

Table 1.2.2-1 Options of MU195020A

Model name	Product name	Remarks
MU195020A-y01	32Gbit/s Extension	*1
MU195020A-x10	1ch Data Output	*2, *3
MU195020A-x20	2ch Data Output	*2, *3
MU195020A-y11	1ch 10Tap Emphasis	*1, *4
MU195020A-y21	2ch 10Tap Emphasis	*1, *5
MU195020A-y30	1ch Data Delay	*1, *4
MU195020A-y31	2ch Data Delay	*1, *5
MU195020A-y40	1ch Variable ISI	*1, *4, *6
MU195020A-y41	2ch Variable ISI	*1, *5, *7
MU195020A-z50	Sequence Editor Function	*8

*1: The y in the model name represents 0, 1, or 2.

*2: The x in the model name represents 0 or 1.

*3: Select either of them.

*4: The MU195020A-x10 is required.

*5: The MU195020A-x20 is required.

*6: The MU195020A-y11 is required.

*7: The MU195020A-y21 is required.

*8: The z in the model name represents 0 or 3.

Table 1.2.2-2 Options of MU195040A

Model name	Product name	Remarks
MU195040A-y01	32Gbit/s Extension	*1
MU195040A-x10	1ch ED	*2, *3
MU195040A-x20	2ch ED	*2, *3
MU195040A-y11	1ch CTLE	*1, *4
MU195040A-y21	2ch CTLE	*1, *5
MU195040A-y22	Clock Recovery	*1

*1: The y in the model name represents 0, 1, or 2.

*2: The x in the model name represents 0 or 1.

*3: Select either of them.

*4: The MU195040A-x10 is required.

*5: The MU195040A-x20 is required.

Table 1.2.2-3 Option of MU195050A

Model name	Product name	Remarks
MU195050A-x01	White Noise	*

*: The x in the model name represents 0 or 1.

1.2.3 Optional Accessories

Table 1.2.3-1 shows the optional accessories for the MP1900A modules. All optional accessories are sold separately.

Table 1.2.3-1 Optional Accessories

Model name/ symbol	Product name	Remarks
J1449A	Measurement kit (K connector)	Coaxial cable (K connector) 0.8 m × 2 Coaxial cable 0.8 m × 2 Coaxial cable 1.0 m × 1
J1625A	Coaxial cable 1 m	SMA connector
J1342A	Coaxial cable 0.8 m	APC 3.5 mm connector
J1439A	Coaxial cable (0.8 m, K connector)	K connector
J1632A	Terminator	
J1359A	Coaxial Adaptor (K-P.K-J, SMA)	
41KC-3	Precision Fixed Attenuator 3 dB	
41KC-6	Precision Fixed Attenuator 6 dB	
41KC-10	Precision Fixed Attenuator 10 dB	
41KC-20	Precision Fixed Attenuator 20 dB	
K240C	Precision Power Divider	
J1624A	Coaxial Cable 0.3 m (SMA connector)	SMA connector
J1550A	Coaxial skew match cable (0.8 m, APC 3.5 connector)	APC 3.5 mm connector, Pair cable
J1551A	Coaxial skew match cable (0.8 m, K connector)	K connector, Pair cable
W3915AE	MU195020/40/50A Operation Manual	Printed version, English
Z0306A	Wrist strap	
MZ1834A	4PAM Converter	
MZ1838A	8PAM Converter	
J1678A	ESD Protection Adapter-K	K connector
J1728A	Electrical Length Specified Coaxial Cable (0.4 m, K connector)	
J1741A	Electrical Length Specified Coaxial Cable (0.8 m, K Connector)	
J1742A	Electrical Length Specified Coaxial Cable (0.84 m, K Connector)	
J1735A	Combiner	
J1758A	ISI Board	
G0375A	32Gbaud Power PAM4 Converter	
G0376A	32Gbaud PAM4 Decoder with CTLE	
G0374A	64Gbaud PAM4 DAC	
G0361A	64Gbaud 2-bit DAC with MUX	
J1748A	Power Splitter (1.5G-18GHz)	
Z1964A	Torque Wrench (Right Angle)	

1.3 Specifications

1.3.1 Specifications for MU195020A

Table 1.3.1-1 Operating Bit Rate

Item	Specifications
Operating Bit Rate Setting Range	2.4 to 21.0 Gbit/s*1 2.4 to 32.1 Gbit/s*2 The range of the operating bit rate is determined by the interlocking module*2 and Table 1.3.1-13 "Clock Output".
MU181000A/B synchronized operation ON Setting Range Offset	This item can be specified when MU181000A or MU181000B are installed to the same unit. 2.400 000 to 21.000 000 Gbit/s, 0.000 002 Gbit/s step*1 2.400 000 to 25.000 000 Gbit/s, 0.000 002 Gbit/s step*2 25.000 004 to 32.100 000 Gbit/s, 0.000 004 Gbit/s step*2 –1000 to +1000 ppm, 1 ppm step*3
MU181500B synchronized operation ON Setting Range Offset	This item can be specified when MU181000A, MU181000B and MU181500B are installed to the same unit. 2.400 000 to 3.125 000 Gbit/s, 0.000 002 Gbit/s step 3.200 002 to 6.250 000 Gbit/s, 0.000 002 Gbit/s step 6.400 002 to 12.500 000 Gbit/s, 0.000 002 Gbit/s step 12.800 002 to 21.000 000 Gbit/s, 0.000 002 Gbit/s step*1 12.800 002 to 25.000 000 Gbit/s, 0.000 002 Gbit/s step*2 25.600 004 to 32.100 000 Gbit/s, 0.000 004 Gbit/s step*2 –1000 to +1000 ppm, 1 ppm step*4

*1: Not available Option x01

*2: Available Option x01

*3: Available when installed in the same mainframe as the MU195020A.

*4: Offset setting range depends on the bit rate. The range is –1000 to 0 ppm at the following bit rate.
Full Rate: 12.500000 Gbit/s, 25.000000 Gbit/s
Half Rate: 25.000000 Gbit/s

1

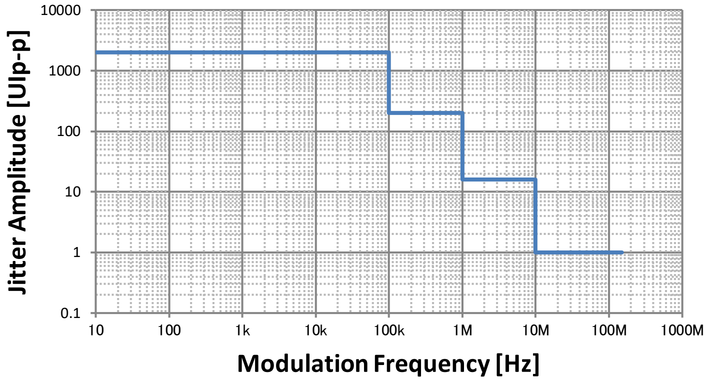
Overview

Table 1.3.1-1 Operating Bit Rate (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>External Clock
When the Output Clock Rate is set to Full Rate</td><td>
<table>
<tr><th>Operating bit rate range</th><th>Input Clock Frequency</th><th>Relationship Between Bitrate and Clock Frequency</th></tr>
<tr><td>2.4 to 16.0 Gbit/s</td><td>2.4 to 16.0 Gbit/s</td><td>Operate at 1/1 clock</td></tr>
<tr><td>16.0 to 20.0 Gbit/s*1</td><td>8.0 to 10.0 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 to 21.0 Gbit/s*1</td><td>10.0 to 10.5 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>16.0 to 20.0 Gbit/s*2</td><td>8.0 to 10.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 to 32.1 Gbit/s*2</td><td>10.0 to 16.05 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 32.1 Gbit/s*2</td><td>6.25 to 8.025 Gbit/s</td><td>Operate at 1/4 clock</td></tr>
</table>
</td></tr>
<tr><td>When the Output Clock Rate is set to Half Rate</td><td>
<table>
<tr><th>Operating bit rate range</th><th>Input Clock Frequency</th><th>Relationship Between Bitrate and Clock Frequency</th></tr>
<tr><td>2.4 to 28.1 Gbit/s*1</td><td>1.2 to 10.05 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>2.4 to 32.1 Gbit/s*2</td><td>1.2 to 16.05 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 32.1 Gbit/s*2</td><td>6.25 to 8.025 Gbit/s</td><td>Operate at 1/4 clock</td></tr>
</table>
</td></tr>
<tr><td>Tracking with external clock MU181500B
When the Output Clock Rate is set to Full Rate</td><td>
<table>
<tr><th>Operating bit rate range</th><th>Input Clock Frequency</th><th>Relationship Between Bitrate and Clock Frequency</th></tr>
<tr><td>2.4 to 15.0 Gbit/s</td><td>2.4 to 15.0 Gbit/s</td><td>Operate at 1/1 clock</td></tr>
<tr><td>15.0 to 20.0 Gbit/s*1</td><td>7.5 to 10.0 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 to 21.0 Gbit/s*1</td><td>10.0 to 10.5 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>15.0 to 20.0 Gbit/s*2</td><td>7.5 to 10.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 to 30.0 Gbit/s*2</td><td>10.0 to 15.0 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 32.1 Gbit/s*2</td><td>6.25 to 8.025 Gbit/s</td><td>Operate at 1/4 clock</td></tr>
</table>
</td></tr>
<tr><td>When the Output Clock Rate is set to Half Rate</td><td>
<table>
<tr><th>Operating bit rate range</th><th>Input Clock Frequency</th><th>Relationship Between Bitrate and Clock Frequency</th></tr>
<tr><td>2.4 to 21.0 Gbit/s*1</td><td>1.2 to 10.5 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>2.4 to 30.0 Gbit/s*2</td><td>1.2 to 15.0 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 32.1 Gbit/s*2</td><td>6.25 to 8.025 Gbit/s</td><td>Operate at 1/4 clock</td></tr>
</table>
</td></tr>
</table>

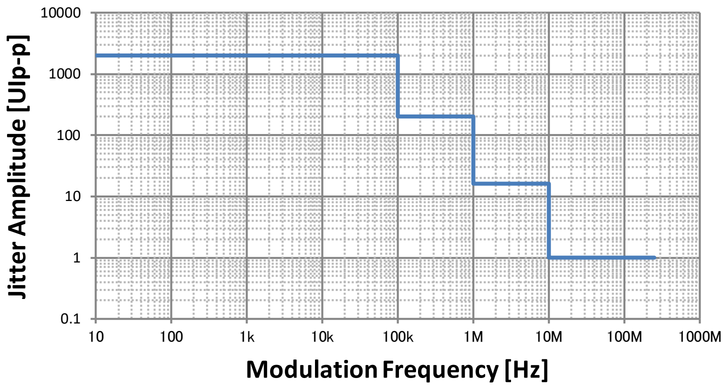
Table 1.3.1-2 Jitter Setting Range

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ1 Clock Output Rate</td><td>At MU181000A/B and MU181500B synchronized operation
When Built-in SJ2 is selected as SJ2, the Jitter Amplitude setting range is narrowed by half.</td></tr>
<tr><td>SJ1 Clock Output Rate
At Full Rate</td><td>30 < Bit rate ≤ 32.1 Gbit/s, 15 < Bit rate ≤ 17 Gbit/s



<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 2000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 200</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 16</td></tr>
<tr><td>10.01M to 150M</td><td>0 to 1</td></tr>
</table>

17 < Bit rate ≤ 30 Gbit/s

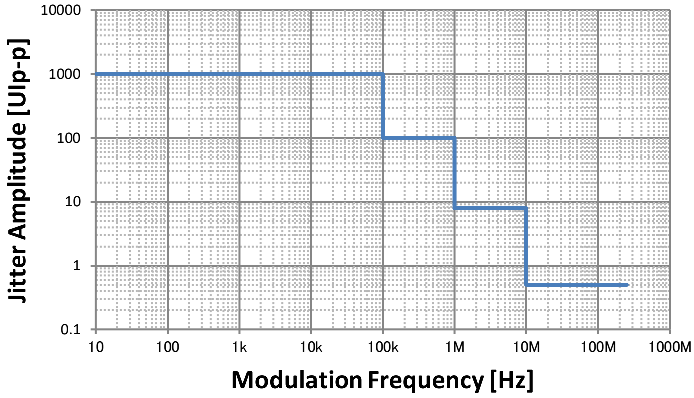


<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 2000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 200</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 16</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 1</td></tr>
</table>
</td></tr>
</table>

Table 1.3.1-2 Jitter Setting Range (Cont'd)

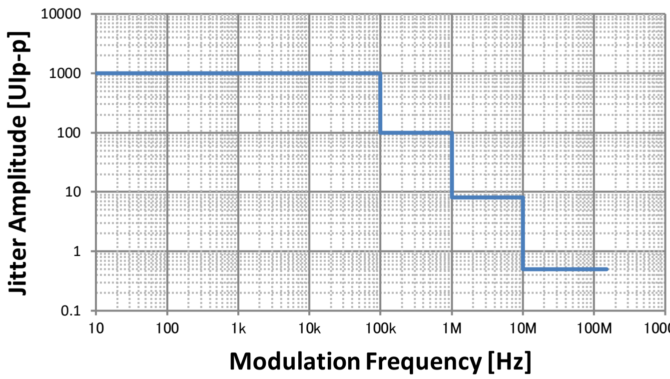
<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ1 Clock Output Rate At Full Rate (Cont'd)</td><td>

8.5 < Bit rate ≤ 15 Gbit/s



<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 1000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 100</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 8</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 0.5</td></tr>
</table>

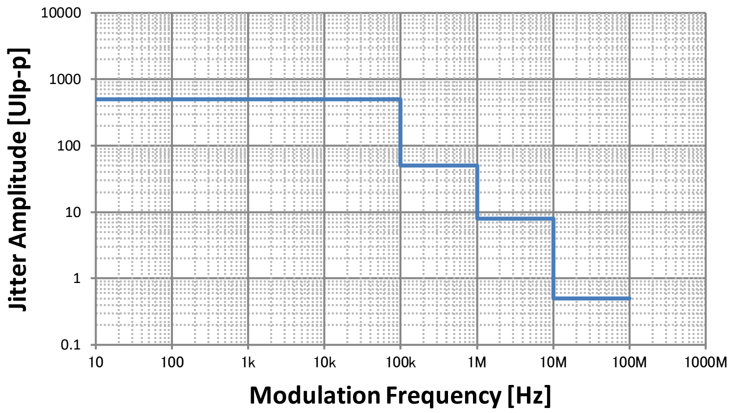
4 < Bit rate ≤ 8.5 Gbit/s



<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 1000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 100</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 8</td></tr>
<tr><td>10.01M to 150M</td><td>0 to 0.5</td></tr>
</table>

</td></tr>
</table>

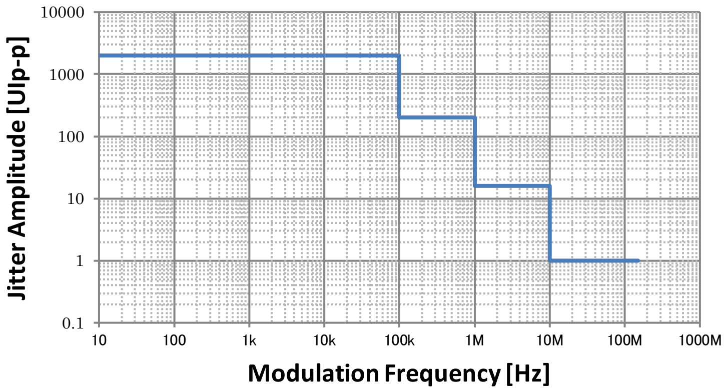
Table 1.3.1-2 Jitter Setting Range (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ1 Clock Output Rate
At Full Rate (Cont'd)</td><td>2.4 < Bit rate ≤ 4 Gbit/s


<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 500</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 50</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 8</td></tr>
<tr><td>10.01M to 100M</td><td>0 to 0.5</td></tr>
</table></td></tr>
</table>

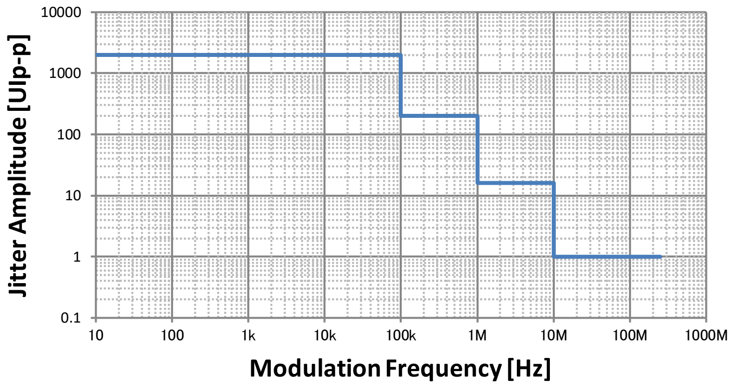
Table 1.3.1-2 Jitter Setting Range (Cont'd)

Item	Specifications
SJ1 Clock Output Rate At Half Rate	30 < Bit rate ≤ 32.1 Gbit/s, 8 < Bit rate ≤ 17 Gbit/s



Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 150M	0 to 1

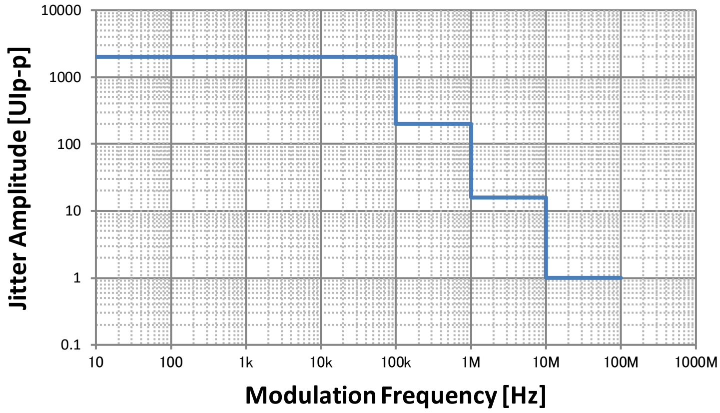
17 < Bit rate ≤ 30 Gbit/s



Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 250M	0 to 1

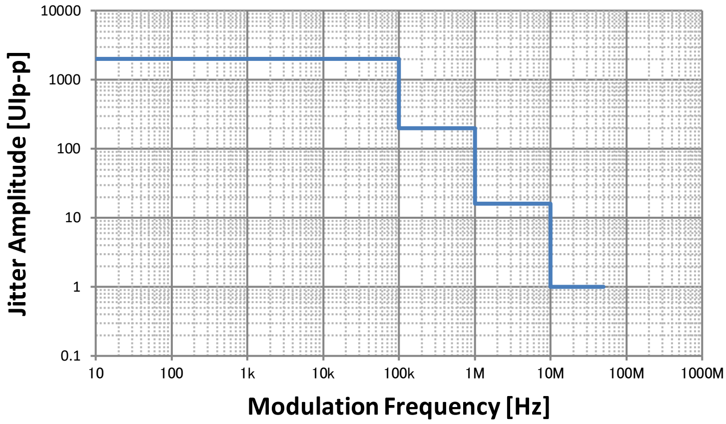
Table 1.3.1-2 Jitter Setting Range (Cont'd)

Item	Specifications
SJ1 Clock Output Rate At Half Rate (Cont'd)	2.4 < Bit rate ≤ 8 Gbit/s



Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 100M	0 to 1

Bit rate 2.4 Gbit/s

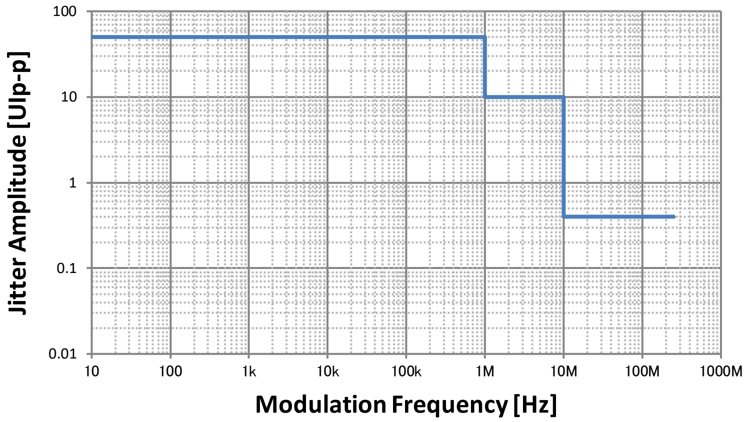


Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 50M	0 to 1

Table 1.3.1-2 Jitter Setting Range (Cont'd)

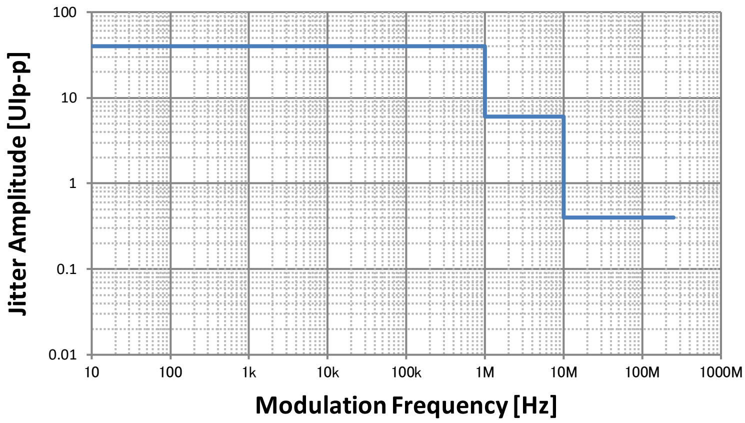
<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ2 Clock Output Rate
SJ2 via MU181000A Clock Output Rate
At Full Rate*1</td><td>

15.000 001 ≤ Bit rate ≤ 32.1 Gbit/s



<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 50</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 10</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 0.4</td></tr>
</table>

6.400 001 ≤ Bit rate ≤ 15 Gbit/s



<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 40</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 6</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 0.4</td></tr>
</table>

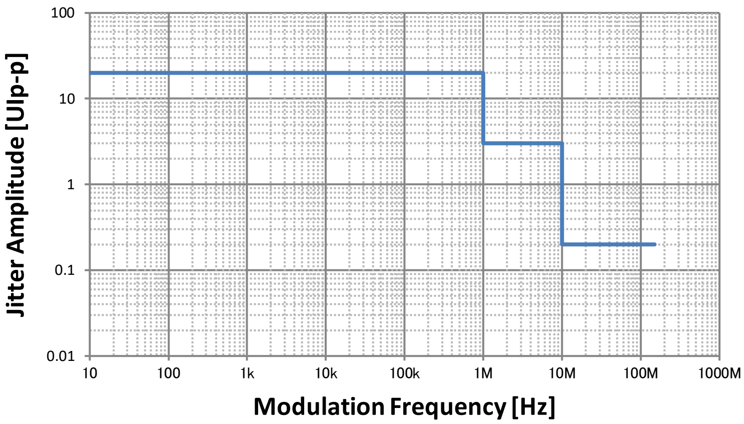
</td></tr>
</table>

*1: Mutually exclusive with Built-in SJ2.

Table 1.3.1-2 Jitter Setting Range (Cont'd)

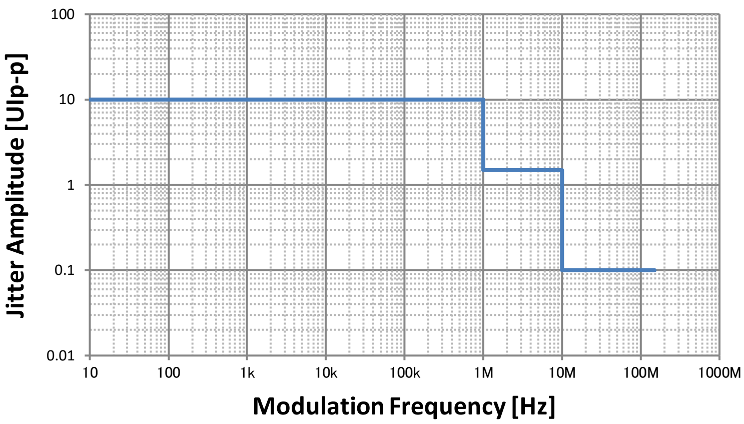
<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ2 via MU181000A Clock Output Rate
At Full Rate*1 (Cont'd)</td><td>

3.200 001 ≤ Bit rate ≤ 6.25 Gbit/s



<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 20</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 3</td></tr>
<tr><td>10.01M to 150M</td><td>0 to 0.2</td></tr>
</table>

2.4 ≤ Bit rate ≤ 3.125 Gbit/s



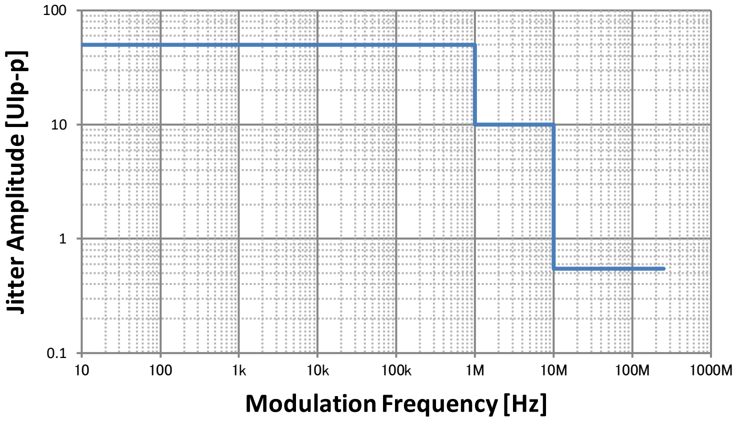
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 10</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 1.5</td></tr>
<tr><td>10.01M to 150M</td><td>0 to 0.1</td></tr>
</table>

</td></tr>
</table>

Table 1.3.1-2 Jitter Setting Range (Cont'd)

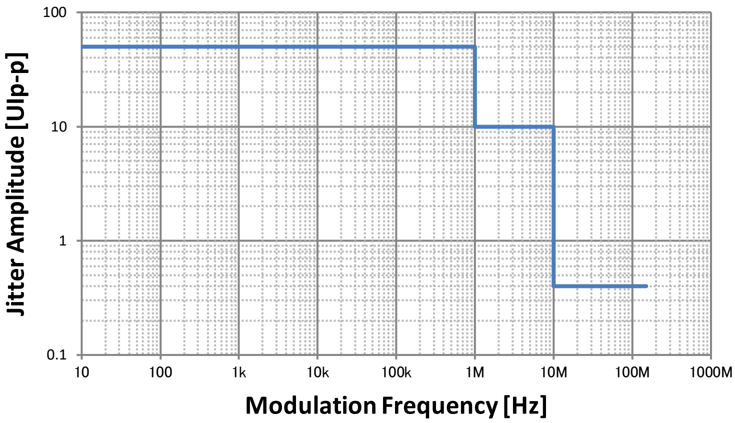
<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ2 via MU181000A Clock Output Rate
At Half Rate*1</td><td>

$12.800001 \leq$ Bit rate ≤ 32.1 Gbit/s



<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 50</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 10</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 0.548</td></tr>
</table>

$6.400001 \leq$ Bit rate ≤ 12.5 Gbit/s

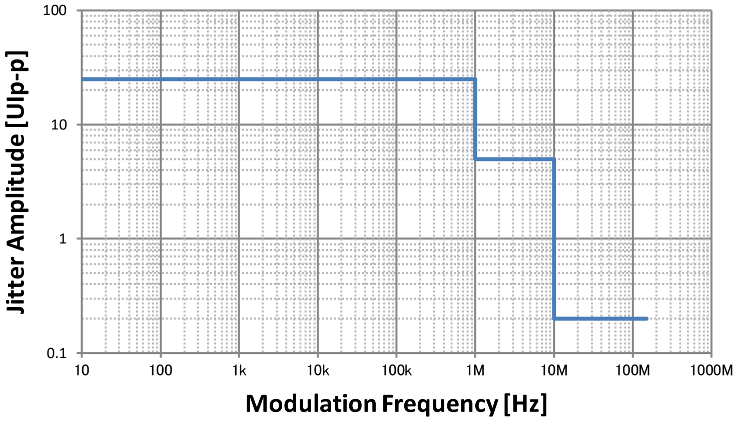


<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 50</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 10</td></tr>
<tr><td>10.01M to 150M</td><td>0 to 0.4</td></tr>
</table>

</td></tr>
</table>

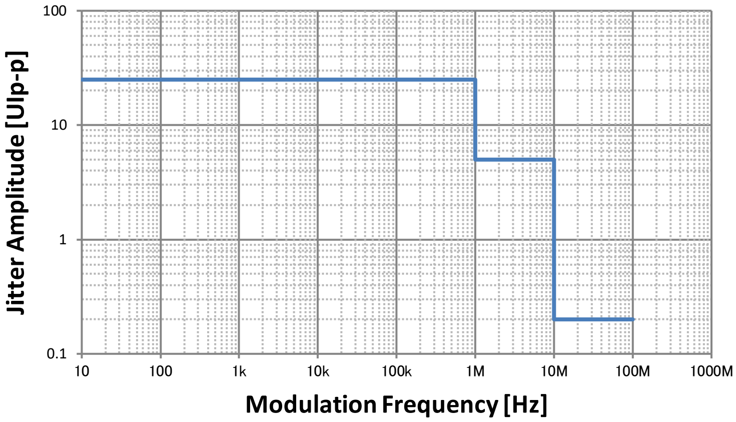
Table 1.3.1-2 Jitter Setting Range (Cont'd)

Item	Specifications
SJ2 via MU181000A Clock Output Rate At Half Rate*1 (Cont'd)	3.600001 ≤ Bit rate ≤ 6.25 Gbit/s



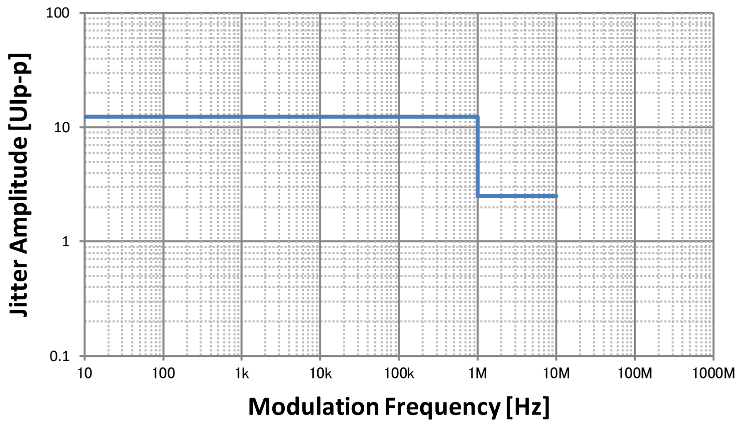
Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 1M	0 to 25
1.001M to 10M	0 to 5
10.01M to 150M	0 to 0.2

3.200001 < Bit rate ≤ 3.6 Gbit/s



Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 1M	0 to 25
1.001M to 10M	0 to 5
10.01M to 100M	0 to 0.2

Table 1.3.1-2 Jitter Setting Range (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ2 via MU181000A Clock Output Rate
At Half Rate*1 (Cont'd)</td><td>2.4 ≤ Bit rate ≤ 3.125 Gbit/s


<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 12.4</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 2.5</td></tr>
</table></td></tr>
<tr><td>Built-in SJ2 Clock Output Rate

Built-in SJ2 Clock Output Rate
At Full Rate*2</td><td>At MU181000A/B and MU181500B synchronized operation

15 < Bit rate ≤ 32.1 Gbit/s
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
<tr><td>100M</td><td>0 to 0.5</td></tr>
<tr><td>210M</td><td>0 to 0.2</td></tr>
</table>
4 < Bit rate ≤ 15 Gbit/s
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>33k</td><td>0 to 500</td></tr>
<tr><td>100M</td><td>0 to 0.25</td></tr>
<tr><td>210M</td><td>0 to 0.1</td></tr>
</table>
2.4 ≤ Bit rate ≤ 4 Gbit/s
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>33k</td><td>0 to 500</td></tr>
<tr><td>100M</td><td>0 to 0.25</td></tr>
</table></td></tr>
</table>

*2: Available when installed in the MP1900A, and mutually exclusive with the SJ2 via MU180000A

Table 1.3.1-2 Jitter Setting Range (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Built-in SJ2 Clock Output Rate
At Half Rate*2</td><td>8 < Bit rate ≤ 32.1 Gbit/s
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
<tr><td>100M</td><td>0 to 0.500</td></tr>
<tr><td>210M</td><td>0 to 0.200</td></tr>
</table>
2.4 < Bit rate ≤ 8 Gbit/s
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
<tr><td>100M</td><td>0 to 0.5</td></tr>
</table>
Bit rate 2.4 Gbit/s
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
</table>
</td></tr>
</table>

Table 1.3.1-3 External Clock Input

Item	Specifications
Number of Input	1 (Single-Ended)
Input frequency range	1.2 to 16.05 GHz
Input amplitude	0.3 to 1.0 Vp-p (–6.5 to +4.0 dBm)
Termination	AC, 50 Ω
Connector	SMA connector (f.)

Table 1.3.1-4 Aux Input and Output

Item	Specifications
Aux Input	
Number of Input	1 (Single-Ended)
Validation	Error Injection, Burst, Sequence Trigger*
Minimum Pulse Width	1/128 of data rate
Input level	0/–1 V (H: –0.25 to 0.05 V L: –1.1 to –0.8 V) 0/–0.5 V(H: –0.05 to 0.05 V L: –0.55 to –0.45 V) Vth 0 V (Input amplitude: 0.5 to 1.0 Vp-p) Select one of the above.
Termination	GND, 50 Ω
Connector	SMA connector (f.)
Aux Output	
Number of Output	2 (Differential output)
Output control	ON/OFF switching
Validation	1/n Clock (n = 4, 6, 8, 10...510, 512), Pattern Sync, Burst Out2, LTSSM Trigger*
Pattern Sync	
PRBS, PRGM	Position: 1 to {(Least common multiple of Pattern Length' and 128) –135}, in 8-bit steps When the pattern length' is 511 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 512 bits or more.
Pattern Change Trigger	Outputs a trigger when Data is selected in Test Pattern and Current Outputting Pattern is changed.
Mixed Data	Block No. setting: 1 to the Block No. specified for Mixed Data, in 1-steps Row No. setting: 1 to the Row No. specified for Mixed Data, in 1-steps
Burst Out2	
Burst Trigger Delay	0 to (Burst Cycle – 128) bits, in 8-bit steps
Pulse Width	0 to (Burst Cycle – 128) bits, in 8-bit steps
Output level	0/–0.6 V (H: –0.25 to 0.05 V, L: –0.80 to –0.45 V)
Terminator	GND, 50 Ω
Connector	SMA connector (f.)

*: Sequence Trigger and LTSSM Trigger can be selected only when Test Pattern is Sequence.

Table 1.3.1-5 Gating Output

Item	Specifications
Number of Output	2 (Differential output)
Output control	ON/OFF switching
Validation	Burst*1, Repeat*1, LFPS*2
Burst	Burst Output
Burst Trigger Delay	0 to (Burst Cycle – 128) bits, in 8-bit steps
Enable Pulse Width	128 to (Burst Cycle – 128) bits, in 8-bit steps
Output Level	0/–1 V (H: –0.25 to 0.05 V, L: –1.25 to –0.8 V)*3
Repeat	Timing Signal Output
Timing Signal Cycle	INT $(\frac{\text{PatternLength}}{128}) \times 128$ (other than Mixed)
Timing Signal Pulse Width	For PRBS, Zero-Substitution, Data: 128 to {(Least common multiple of Pattern Length' and 128) –128}, in 8-bit steps The maximum settable number is 34 359 738 240. When the pattern length is 511 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 512 bits or more. For Mixed: 128 to (Row length × Number of rows × Number of blocks –128), in 8-bit steps The maximum settable number is 2 415 918 976.
Timing Signal Delay	Same value as the timing signal pulse width.
Output Level	0/–1 V (H: –0.25 to 0.05 V, L: –1.25 to –0.8 V)*
Terminator	GND, 50 Ω
Connector	SMA connector (f.)

*1: Can be set when Test Pattern is other than Sequence.

*2: Can be set when Test Pattern is Sequence and Specification is USB3.0 or USB3.1 Gen2.

*3: L: Output Enable, H: Output Disable

Table 1.3.1-6 Pattern Generation

Item	Specifications
PRBS Pattern Length Mark ratio	 2^n–1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) 1/2 (1/2INV is supported by a logical inversion.)
Zero-Substitution Additional bit Pattern Length Start position Length of Consecutive Zero Bits	 0 bit, 1 bit 2^n (n = 7, 9, 10, 11, 15, 20, 23) 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23) Substitutes the bit coming after the maximum “0” successive bits. 1 to (Pattern Length–1) bits If the bit coming after Zero-substitution is “0”, then it is replaced with “1”.
Data Data Length Current Outputting Pattern Maximum List Num	 2 to 268 435 456 bits, in 1-bit steps 1 to 10, 1 step Outputs the pattern of the selected number. Patterns can be switched glitch-free. 1 to 10, 1 step
Mixed Pattern Pattern Mixed Block Mixed Row Length Data Length Number of rows Number of blocks PRBS Pattern Length, Mark ratio PRBS Sequence Scramble	 Data To the smaller of the following values: 1 to 511 Block, 1-Block steps $\mathrm{INT}\left(\frac{268435456}{\text{ROW count}} \times \text{Data length}\right)$ bits $\mathrm{INT}\left(\frac{268435456 + 2^{31}}{\text{ROW length}} \times \text{ROW count}\right)$ bits 2048 to 268435456 + 2^{31}, in 1024-bit steps (Data + PRBS Length) 1024 to 268435456 bits, in 1-bit steps 1 to 16, in 1-steps 1 to 511, in 1-steps Same as PRBS. Restart, Consecutive Can be set per PRBS and Data for each Block (except the Data area for Block 1)

Table 1.3.1-6 Pattern Generation (Cont'd)

Item	Specifications
PAM4*1	
Sequence	Square Wave, JP03A, JP03B, PRQS10, SSPR, QPRBS13, QPRBS13-CEI, SSPRQ, Transmitter Linearity, PRBS13Q, PRBS31Q, User Define
User Define in detail	
Raw Data	PRBS, Data
PRBS Pattern Length	Same as PRBS.
PRBS Inversion	Logic Inversion/Non-Inversion of PRBS part
Data Length	Same as Data
Gray Coding	Gray Coding ON/OFF
Raw Data	PRBS, Data
PRBS Pattern Length, Mark Ratio	Same as PRBS.
PRBS Inversion	Logic Inversion/Non-Inversion of PRBS part
Data Length	Same as Data
Gray Coding	Gray Coding ON/OFF
Sequence*2	
Specification	PCIe1, PCIe2, PCIe3, PCIe4, USB3.0, USB3.1 Gen2
Logic	POS, NEG
PRBS Inversion	ON, OFF
Transmit	Starts transmitting the sequence pattern. The LED lights up during transmission.
Manual	Enabled when Manual Trigger is set.
Trigger Block No.	Sets the block number of the sequence to output an LTSSM Trigger signal from AUX Output connector. 1 to 128 Block No., 1 step

*1: Configurable only when 2ch Combination or 64G x 2ch Combination is set.

*2: The MU195020A-z50 is required. This can be set only when Module Combination is set to **Independent**.
If either Ch1 or Ch2 is set to Sequence, the other is also set to Sequence.

Table 1.3.1-7 Sequence Editor

Item	Specifications
Preset	Emphasis Preset settings PCIe1, PCIe2, PCIe3, PCIe4 2.5G: P0 to P10 5.0G: P0 to P10 8.0G: P0 to P10 16.0G P0 to P10 USB3.0 5.0G: P0 to P10 USB3.1 Gen2 10.0G: P0 to P10
Break	External(LFPS)*1 External(Edge) Manual OFF
Loop	Time, Num Enabled when Break is set to OFF.
Loop Time	1 to 1,000,000 μsec, 1 μsec step
Loop Num	2 to 1,000,000 times, 2 time step
Insert OS	
SKP OS	SKP OS Insertion: ON, OFF SKP OS Reset: ON, OFF
EIEOS	EIEOS Insertion: ON, OFF EIEOS Reset: ON, OFF EIEOS Interval: 1 to 65536 pattern repeats, 1 step Enabled when Specification is PCIe1, PCIe2, PCIe3, and PCIe4
SYNC OS	SYNC OS Insertion: ON, OFF SYNC OS Reset: ON, OFF SYNC OS Interval: 1 to 65536 pattern repeats, 1 step Enabled when Specification is USB3.1 Gen2.
Scrambler Seed	8b10b: FFFF 128b130b: Lane0, Lane1, Lane2, Lane3, Lane4, Lane5, Lane6, Lane7 128b132b: 1DBFBC

*1: Enabled when the Specification is USB3.0 or USB3.1.

Table 1.3.1-7 Sequence Editor (Cont'd)

Item	Specifications	
PCIe1		
Bitrate	2.5 Gbit/s	
Coding	8b10b	
Block number	1 to 128 blocks	
Pattern Length	32 to 1024 bit, 8 bit step (8b10b) 2 to 268,435,450 bit, 1 bit step (General) 2^n-1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) (General)	
Pattern type	Electrical Idle, 8b10b, General*2	
SKP Ordered Set Insertion	Length:	COM+1, COM+2, COM+3, COM+4, COM+5
	Interval:	76 to 3076 symbols, 2 step
	Symbol Length x2:	ON, OFF
PCIe2		
Bitrate	2.5 Gbit/s, 5.0 Gbit/s	
Coding	8b10b	
Block number	1 to 128 blocks	
Pattern Length	32 to 1024 bit, 8 bit step (8b10b) 2 to 268,435,450 bit, 1 bit step (General) 2^n-1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) (General)	
Pattern type	Electrical Idle, 8b10b, General*2	
SKP Ordered Set Insertion	Length:	COM+1, COM+2, COM+3, COM+4, COM+5
	Interval:	76 to 3076 symbols, 2 step
	Symbol Length x2:	ON, OFF

*2: General can be set to only the last line of Sequence.

Table 1.3.1-7 Sequence Editor (Cont'd)

Item	Specifications
PCIe3	
Bitrate	2.5 Gbit/s, 5.0 Gbit/s, 8.0 Gbit/s
Coding	8b10b, 128b130b 128b130b can be set only when Bitrate is 8.0 Gbit/s.
Block number	1 to 128 blocks
Pattern Length	32 to 1024 bit, 8 bit step (8b10b) 128 to 1024 bit, 128 bit step (128b130b) 2 to 268,435,450 bit, 1 bit step (General) 2^n-1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) (General)
Pattern type	Electrical Idle, 8b10b, 128b130b, General*2
SKP Ordered Set Insertion	Length: 8, 12, 16, 20, 24 Interval: 20 to 750 blocks, 1 step Symbol Length x2: ON, OFF
PCIe4	
Bitrate	2.5 Gbit/s, 5.0 Gbit/s, 8.0 Gbit/s, 16.0 Gbit/s
Coding	8b10b, 128b130b 128b130b can be set only when Bitrate is 8.0 Gbit/s and 16.0 Gbit/s.
Block number	1 to 128 blocks
Pattern Length	32 to 1024 bit, 8bit step (8b10b) 128 to 1024 bit, 128bit step (128b130b) 2 to 268,435,450 bit, 1bit step (General) 2^n-1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) (General)
Pattern type	Electrical Idle, 8b10b, 128b130b, General*2
SKP Ordered Set Insertion	Length: 8, 12, 16, 20, 24 Interval: 20 to 750 blocks, 1 step Symbol Length x2: ON, OFF

Table 1.3.1-7 Sequence Editor (Cont'd)

Item	Specifications
USB3.0	
Bitrate	5.0 Gbit/s
Coding	8b10b
Block number	1 to 128 blocks
Pattern Length	32 to 1024 bit, 8 bit step 2 to 268,435,450 bit, 1 bit step (General) 2^n-1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) (General)
Pattern type	LFPS*3,*4 Warm Reset, Polling LFPS, Ping LFPS, Loopback Exit Preset Pattern TS1, TS2, TSEQ, Idle Data, CP0, CP1, CP2, CP3, CP4, CP5, CP7, CP8 User Defined User Defined Pattern User Defined pattern is only for 5GT/s signal.
SKP Ordered Set Insertion	Length: 2, 4, 6 Interval: 76 to 708 symbols, 1 step
USB3.1 Gen2	
Bitrate	10.0 Gbit/s
Coding	128b132b
Block number	1 to 128 blocks
Pattern Length	128 to 1024 bit, 128 bit step
Pattern type	LFPS*3,*4 Warm Reset, Polling LFPS, Ping LFPS, Loopback Exit Preset Pattern TS1, TS2, TSEQ, Idle Data, CP0, CP1, CP2, CP3, CP4, CP5, CP7, CP8 User Defined User Defined Pattern User Defined pattern is only for 5GT/s signal.
SKP Ordered Set Insertion	Length: 8, 12, 16, 20, 24, 28, 32, 36, 40 Interval: 20 to 80 Blocks, 1 Step Symbol Length x2: ON, OFF

*3: LFPS can be transmitted on CH1 only

*4: LFPS is a fixed pattern and cannot be edited by the user.

Table 1.3.1-7 Sequence Editor (Cont'd)

Item	Specifications
8b10b Pattern Editor	
Notation	Symbol, Bin, Hex
Scrambler Enable	Scrambles the selected symbols. ON, OFF
Scrambler Reset	Resets the seed value of scrambler on the selected symbols. ON, OFF
Code	K-code, D-code
K code	K28.0, K28.1, K28.2, K28.3, K28.4, K28.5, K28.6, K28.7 K23.7, K27.7, K29.7, K30.7
D code	D0.0 to D31.7
MSB First / LSB First	MSB First, LSB First
128b130b Pattern Editor	
Notation	Bin, Hex
Scrambler Enable	Scrambles the selected symbols. ON, OFF
Scrambler Reset	Resets the seed value of scrambler on the selected symbols. ON, OFF
DC Balance	Adds DC balance to the symbol 14 and 15. ON, OFF
Sync Header	Defines 2-bits Sync Header.
MSB First / LSB First	MSB First, LSB First
128b132b Pattern Editor	
Notation	Symbol Bin, Symbol Hex
Scrambler Enable	Scrambles the selected symbols. ON, OFF
Scrambler Reset	Resets the seed value of scrambler on the selected symbols. ON, OFF
DC Balance	Adds DC balance to the symbol 14 and 15. ON, OFF
Sync Header	Defines 4-bits Sync Header.
MSB First / LSB First	MSB First, LSB First

Table 1.3.1-8 Pattern Sequence

Item	Specifications
Sequence	Repeat/Burst
Repeat	Continuous Pattern
Burst	
Source	Internal, External-Trigger (Aux Input), External-Enable (Aux Input)
Data Sequence	Restart, Consecutive, Continuous
Burst Cycle	25600 to 2147483648 bits, in 1024-bit steps
Enable period	Internal: 12800 to 2147483392 bits, in 256-bit steps Ext Trigger: 12800 to 2147483648 bits, in 256-bit steps

Table 1.3.1-9 Pre-Code

Item	Specifications
ON/OFF	Sets Pre-Code function ON and OFF*
Modulation type	2ch Combination: DQPSK
Initial Data	Choose 0 or 1.

*: The function is available only when Pattern Sequence is Repeat.

Table 1.3.1-10 Error addition

Item	Specifications
Area	ALL, Specific Block (Can be selected only for Mixed.)
Internal trigger	
Error Variation	Repeat, Single
Error Ratio	*E– n (*=1 to 9, n=3 to 12), Upper limit is 5.0E–3
Insertion CH	1 to 32, or channel scan (Only when Internal is set.)
External trigger*	
Control Method	External-Trigger (Rise edge trigger), External-Disable (L: Disable)
Bit/Burst	Selects Bit Error or Burst Error
Burst Length	1 to 127, 1 step

*: Can be set when Test Pattern is other than Sequence.

Table 1.3.1-11 Data Output

Item	Specifications*1
Number of outputs	Option x10: 2 (Data, XData) Option x20: 4 (Data1, XData1, Data2, XData2)
Eye amplitude	
Setting range	0.1 to 1.3 Vp-p, 2 mV step
Accuracy	±50 mV± 17%
Offset	
Setting range	$-2.0-\frac{\text{Amp.}}{2}$ to $+3.3-\frac{\text{Amp.}}{2}$ Vth, 1mV step
Accuracy	±65 mV ±10% of offset (Vth) ± (Eye Amp. Accuracy / 2)*2
Defined Interface	NECL, SCFL, NCML, PCML, LVPECL
Cross Point	50% Fixed
Rising/falling time	12 ps (20 to 80%)*2,*3,*4, ≤15 ps (20 to 80%)*2,*3
Half Period Jitter	
Setting range	–20 to 20, in 1-steps
Accuracy	±0.02 UI*4,*5

*1: Unless otherwise specified, these are defined with the conditions of PRBS2^{31}–1, Mark ratio 1/2, and Cross Point 50%.

These values are monitored using an applicable part (J1439A coaxial cable, 0.8 m, K connector) at a sampling oscilloscope bandwidth of 70 GHz.

*2: Option x11 or Option x21 is installed and that Emphasis is not set.

*3: If Option x01 is not available, then this is at 21 Gbit/s.

If Option x01 is available, then this is at 32.1 Gbit/s.
Amplitude: 1.0 Vp-p

*4: Typical value

*5: When the value is set to 0.

Table 1.3.1-11 Data Output (Cont'd)

Item	Specifications*1
Intrinsic Jitter	
Peak-to-Peak Jitter (p-p)	6 ps p-p (Measurement count 30)*3,*4,*6
Random Jitter (RMS)	300 fs rms (1,0 repeat pattern)*3,*4,*6 115 fs rms (28 Gbit/s 1,0 repeat pattern)*3,*4,*7
Total Jitter (Total)	6 ps (Measurement count 30)*3,*4,*6,*8
Waveform Distortion (0-peak)	±25 mV ±15%*3,*4,
Output control	ON/OFF switching
Data/XData skew	±1 ps*4,*9
Skew between channels*10	±0.25 UI
Termination	AC, DC switching, 50 Ω For DC: GND, –2 V, +1.3 V, +3.3 V, Open (LVDS)
Connector	K (f.)
Offset Reference level	Vth
Level Guard	Amplitude, Voh, and Vol can be specified.
External ATT factor	0 to 40 dB, in 1 dB steps

*6: Using oscilloscope with residual jitter of less than 200 fs (RMS).

*7: Using oscilloscope with residual jitter of less than 70 fs (RMS).

*8: Defined by PRBS2^{15}-1 and BER 10^{-12}.

*9: Cable error is not included.

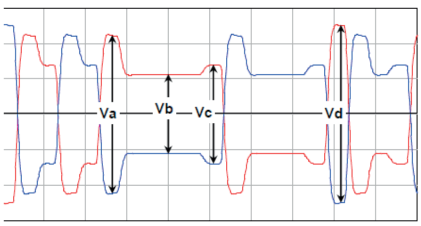
*10: When Option x20 is available.

Table 1.3.1-12 10 Tap Emphasis*1

Item	Specifications
Emphasis Tap	10 (6 post-cursor, 3 pre-cursor)
Cursor Setting Range	–20 to 20 dB, in 0.1 dB steps*2
Accuracy	±1 dB*3,*4
Emphasis Peak Voltage Setting Range	0.1 to 1.5 Vp-p (Single-Ended)
Output control	ON/OFF switching
Transition Time from Idle State	≤ 8 ns*5
Channel Emulator*6,*7	Normal: Outputs the PPG Data signal whose waveform emulates the connected transmission line with the loaded S parameter. Inverse: Outputs the PPG data signal whose waveform emulates the De-Emphasis compensating the loss of the transmission line with the loaded S parameter.
Response	Normal, Inverse
S-Parameter file	S2P file (Extension: "*.s2p"), S4P file (Extension: "*.s4p") Supports output files from Vector Network Analyzer MS4640B Series.
Variable ISI*6	Sets the loss of the channel which generates ISI and outputs the PPG data signal whose waveform emulates the setting. (The output waveform amplitude is standardized by the amplitude settings.) This is available when combining with the optional accessory J1758A ISI Board (select "J1758A") or the external channel board (select "Not Specified").
Frequency Setting	Insertion Loss configurable at Nyquist Frequency or 1/2 Nyquist Frequency
Insertion Loss Setting	1.5 to 25 dB in 0.01 dB steps @Nyquist Frequency 0 to 25 dB in 0.01 dB steps @1/2Nyquist Frequency
Insertion Loss Accuracy*8	±1dB Nominal @Nyquist Frequency 10 dB, Repeating pattern of "1,0", ±1dB Nominal @1/2Nyquist Frequency 5 dB, Repeating pattern of "1,1,0,0", Bit rate 16 Gbit/s, 25 Gbit/s (when Option 01 installed), Eye Amplitude 1.0 Vp-p, at each spectrum

*1: When Option x11 or Option x21 is added.

*2: Post-cursor: $20\log_{10}(\frac{V_a}{V_b})$, Pre-cursor: $20\log_{10}(\frac{V_c}{V_b})$



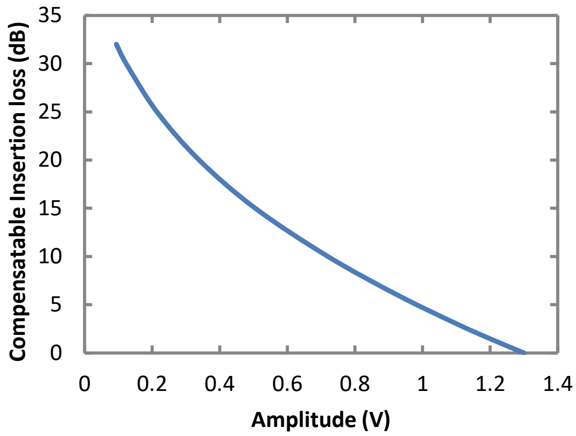
*3: Typical value

*4: Defined for the preset of 8 Gbit/s, 16 Gbit/s, and 25 Gbit/s for PCIe 3 and PCIe 4 respectively.

*5: Maximum time to transition to valid diff signaling after leaving Electrical Idle

*6: When Option x40 or Option x41 is installed.

*7: The compensable maximum transmission line loss without decreasing the amplitude by the Channel Emulator function is shown in the following graph.



*8: The frequency characteristics of Insertion Loss Accuracy when setting 25 dB@Nyquist Frequency and 12.5 dB@1/2 Nyquist Frequency are shown below. (Nominal)

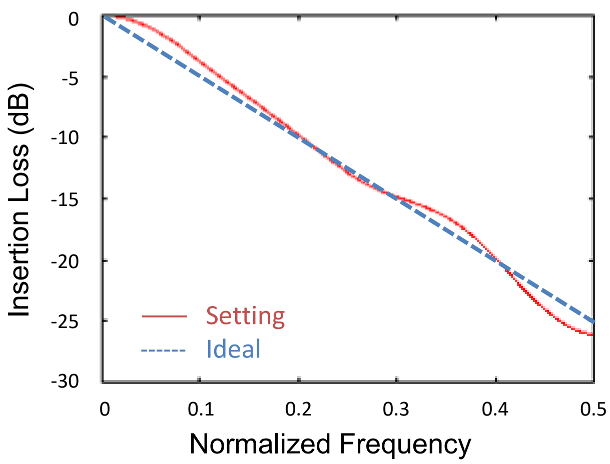


Table 1.3.1-13 Clock Output

Item	Specifications*1
Frequency	
Full Rate	2.4 to 21.0 GHz*2 2.4 to 32.1 GHz*3 Operation bit rate is same as clock output frequency.
Half Rate	1.2 to 10.5 GHz*2 1.2 to 16.05 GHz*3 Operation bit rate is double of output clock frequency.
Number of Output	1
Amplitude	0.3 to 1.0 Vp-p
Output control	ON, OFF switching
Termination	AC, 50 Ω
Connector	K (f.)

*1: These values are monitored using an applicable part (J1439A coaxial cable, 0.8 m, K connector) at a sampling oscilloscope bandwidth of 70 GHz.

*2: Option x01 not available.

*3: Option x01 available.

Table 1.3.1-14 Data Delay*1

Item	Specifications
Phase setting range	–1000 to +1000 mUI, in 2 mUI steps
Accuracy	±50 mUIp-p*2,*3
mUI – ps switching	Available
Calibration	Available
Calibration indicator	This indicator is on when Calibration is required due to: • 1/1 Clock frequency change by ±250 kHz. • Ambient temperature change by ±5 degree.

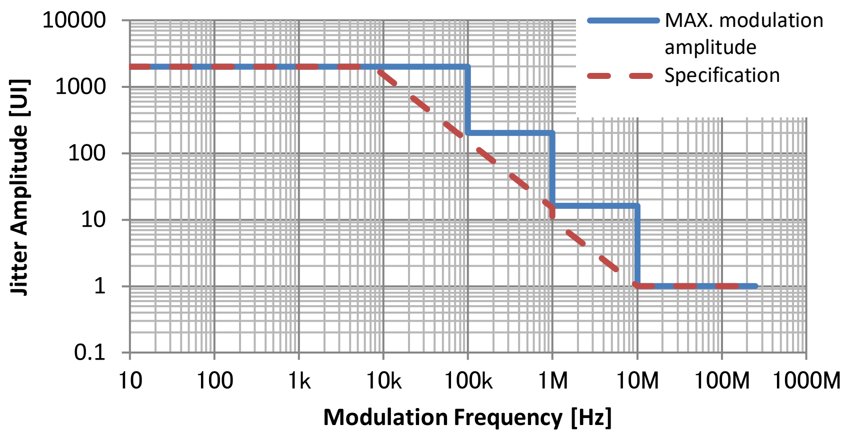
*1: When Option x30 or Option x31 is available.

*2: When using an item with an oscilloscope residual jitter of less than 200 fs (RMS).

*3: Typical value

Table 1.3.1-15 Jitter tolerance

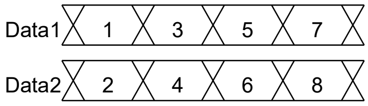
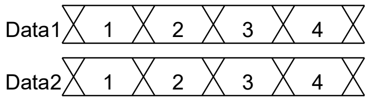
<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Jitter tolerance mask</td><td>
Bit rate: 16 Gbit/s, 28.1 Gbit/s*, 32.1 Gbit/s*
Pattern: PRBS2^{31}–1
SSC with a 5300 ppm amplitude and RJ of 0.3 UI can be simultaneously applied by using MU181500B.
These specifications are defined assuming the following conditions: Loopback connection to the MU195040A, defined by one specific temperature in the range of 20 to 30°C.
When RJ + BUJ is bigger than 0.5 UIp-p or SJ1 + Built-in SJ2 + RJ + BUJ is bigger than the standard value + 0.3 UIp-p, “Overload” is displayed on the MU181500B screen.



<table>
<tr><th>Modulation frequency [Hz]</th><th>MAX. modulation amplitude [UIp-p]</th><th>Specification [UIp-p]</th></tr>
<tr><td>10</td><td>2,000</td><td>2,000</td></tr>
<tr><td>7,500</td><td>2,000</td><td>2,000</td></tr>
<tr><td>100,000</td><td>2,000</td><td>150</td></tr>
<tr><td>1,000000</td><td>200</td><td>15</td></tr>
<tr><td>10,000,000</td><td>16</td><td>1</td></tr>
<tr><td>250,000,000</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
</table>

*: Option x01 available.

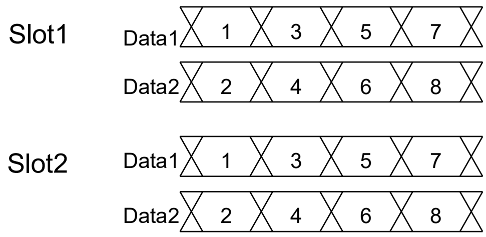
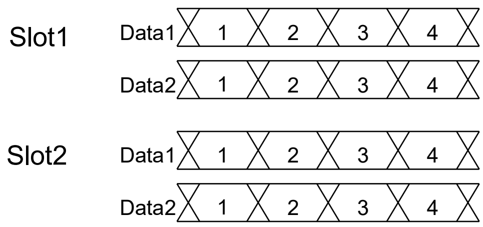
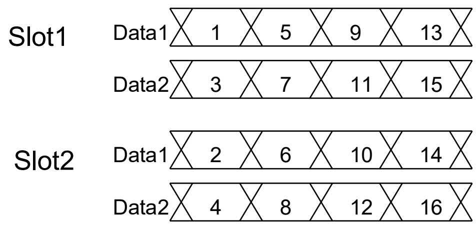
Table 1.3.1-16 Multichannel operation*1

Item	Specifications
Combination Setting *2 2ch Combination	Generates signals with bit phase shift as 42/64 Gbit/s band signal source. Supports 2ch Combination.  Image of 2ch Combination Combination condition: • Combination using multiple modules is not supported. .
Channel Synchronization	Generate patterns that start position has been synchronized as a parallel signal generator. Each channel has an independent Test Pattern and is controlledso that the timing of generation in the same.  Image of Channel Synchronization

*1: Multichannel operation cannot be set when Test Pattern is set to Sequence.

*2: Option x31 is required.

Table 1.3.1-16 Multichannel operation (Cont'd)

Item	Specifications
Inter-modules combination*3	Combination Setting condition: • Options of each module must be same. • Slot 1 to 4: 2ch CH Sync, CH Sync, 64G × 2ch Combination • When modules to be combined are installed sequentially from slot 1.
2ch CH Sync*4	Inter-modules synchronization of 2ch Combination: DataXs of each module synchronize.  Image of 2ch CH Sync
CH Sync	Inter-modules synchronization: Pattern bits of each Data channel synchronize.  Image of CH Sync
64G × 2ch Combination*4	Inter-modules synchronization of 2ch Combination: Pattern bits of DataX channel of each module shift in 1/4 period.  Image of 64G × 2ch Combination

*3: Option x30 or option x31 is required.

*4: Only for option x31.

Table 1.3.1-16 Multichannel operation (Cont'd)

Item	Specifications
Output	
Phase variable range	–64 000 to +64 000 mUI*5
Phase variable step	2 mUI*5
Pattern	
Data	
Data Length	$2 \times n$ to $268435456 \times n$ bits, in n-bit steps*6
Mixed	
Row Length	$(2048 \times n)$ to $\{(268435456 + 2^{31}) \times n\}$, in $(1024 \times n)$-bit steps*6
Data Length	$(1024 \times n)$ to $268435456 \times n$ bits, in n-bit steps*6
Burst	
Burst Cycle	$(25600 \times n)$ to $(2147483648 \times n)$ bits, in $(1024 \times n)$-bit steps*6
Enable period	Internal: $(12800 \times n)$ to $2147483392 \times n$ bits, in $(256 \times n)$-bit steps*6 Ext Trigger: $(12800 \times n)$ to $2147483648 \times n$ bits, in $(256 \times n)$-bit steps*6
Pulse Width	0 to $\{(\text{Burst Cycle} - 128) \times n\}$ bits, in $(8 \times n)$-bit steps*6
Delay	0 to $\{(\text{Burst Cycle} - 128) \times n\}$ bits, in $(8 \times n)$-bit steps*6
Gating Output Repeat (Data)	
Pulse Width	$0 \times n$ to $(268435328 \times n)$, in $(8 \times n)$-bit steps*6
Delay	$0 \times n$ to $(268435328 \times n)$, in $(8 \times n)$-bit steps*6
Repeat (Mixed)	
Pulse Width	$0 \times n$ to $(2^{31} + 268435456 - 128) \times n$, in $(8 \times n)$-bit steps*6
Delay	$0 \times n$ to $(2^{31} + 268435456 - 128) \times n$, in $(8 \times n)$-bit steps*6

*5: A separate value can be set for each channel. This value is common to both Channel Combination and Channel Synchronization.

*6: Common to every channel specified by Combination Setting.

Table 1.3.1-17 General

Item	Specifications
Dimensions	21 mm (H), 234 mm (W), 175 mm (D) Excluding protrusions
Mass	2.5 kg max.
Operating Temperature	15 to 35°C
Storage Temperature	–20 to 60°C

Table 1.3.1-18 Extension Function

Item	Specifications
PCIe	Supports the following PCIe tests when controlled by MX183000A.
Supported standards	PCI Express Base Specification Revision 4.0 Version 0.5, 0.7, 1.0 PCI Express Base Specification Revision 5.0 Version 1.0 Bitrate: PCIe Gen1, Gen2, Gen3, Gen4, Gen5 Lane number: × 1 Test target: Root Complex, End Point
Required option	Option x10/x11 or x20/x21
Required software	MX183000A-PL011: This software enables setting DUT to Loopback state by following PCIe LTSSM and generating a training sequence required for transition to Loopback state. MX183000A-PL021: This software enables setting DUT to Loopback state by following PCIe LTSSM and supporting negotiation with DUT. LTSSM state transition can be analyzed as log. (With this software, one MU195020A and one MU195040A are required.) MX183000A-PL025: This software enables extending the functionality of PL021 to PCIe 5.0. Adding MX183000A-PL001 to each option of the above software enables controlling MU195020A, MU181500B, and MU195040A and supporting Jitter Tolerance Test.
Loopback Through	Configuration, Recovery
Test pattern	Modified Compliance Pattern Insert Delay Symbol: Enable, Disable (Available for Gen1 and Gen2) Insert SRIS: Enable, Disable (Available for Gen3, Gen4, and Gen5) Compliance Pattern Insert Delay Symbol: Enable, Disable (Available for Gen1 and Gen2) User PRBS, Data (8. The pattern defined in Table 1.3.1-6 “Pattern Generation”)
SKP Ordered Set Insertion	Enable, Disable
SKP Length/Insertion	For Gen1, Gen2 Length: COM+1, COM+2, COM+3, COM+4, COM+5 Interval: 768 to 3076, 1-steps For Gen3, Gen4, Gen5 Length: 8, 12, 16, 20, 24 Interval: 187 to 750, 1-steps
Dynamic Link Training	Available when using MX183000A-PL021.
Ling training repeat	1 to 15 (when using MX183000A-PL021)

Table 1.3.1-18 Extension Function (Cont'd)

Item	Specifications
Counter	Tx SKP Count, Rx SKP Count (when using MX183000A-PL021) Error Rate, Error Count (when using MX183000A-PL021)
Error Addition	Defined for Modified Compliance Pattern, Compliance Pattern
Error Variation	Repeat, Single
Error Ratio	*E– n (*=1 to 9, n=3 to 12), upper limit is 5.0E–3.
PAM4	Supports the following by combining MU195020A with MZ1834A/B and G0375A. PAM4 signal generation • Amplitude (Single-ended) 0.048 to 0.310 Vp-p (MZ1834A) • Amplitude (Single-ended) 0.048 to 0.489 Vp-p (MZ1834B) • Amplitude (Single-ended) 0.3 to 1.95 Vp-p (G0375A) PAM4 Emphasis signal generation (when Option x11 or Option x21 is installed) • Emphasis Peak Voltage (Single-ended) 0.048 to 0.357 Vp-p (MZ1834A) • Emphasis Peak Voltage (Single-ended) 0.048 to 0.564 Vp-p (MZ1834B) • Emphasis Peak Voltage (Single-ended) 0.3 to 2.25 Vp-p (G0375A)
USB	Supports the following USB tests when controlled by MX183000A.
Supported standards	USB3.0/3.1
Required option	Option x10/x11 or x20/x21
Required software	MX183000A-PL022: This software enables setting DUT to Loopback state by following USB LTSSM and supporting negotiation with DUT. LTSSM state transition can be analyzed as log. (With this software, one MU195020A and one MU195040A are required.) Adding MX183000A-PL001 to each option of the above software enables controlling MU195020A, MU181500B, and MU195040A and supporting Jitter Tolerance Test.

1.3.2 Specifications for MU195040A

Table 1.3.2-1 Operating bit rate

Item	Specifications
Operating bit rate	2.4 to 21.0 Gbit/s*[1] 2.4 to 32.1 Gbit/s*[2]

*1: When option x01 is not installed.

*2: When option x01 is installed.

Table 1.3.2-2 System Clock

Item	Specifications
System Clock	External, Clock Recovery, Clock and Data Recovery are optional.*

*: Available when Option x22 is installed. If it is not installed, only External is available. Clock is recovered from the data input to the Data1 Input connector.

Table 1.3.2-3 Data Input

Item	Specifications
Number of inputs	2 (Data, XData) (Differential)*[1] 4 (Data1, XData1, Data2, XData2) (Differential)*[2]
Amplifier	Single-Ended 50 Ω, Differential 50 Ω, Differential 100 Ω can be set. At single-ended 50 Ω: Data and XData can be set. At differential 50/100 Ω: Tracking, Independent, Alternate can be set. When Alternate is selected: Data-XData and XData-Data can be set.*[3] CTLE: On/Off Switching*[4]
Input signal format	NRZ, PAM4
Input amplitude*[5]	0.05 to 1.0 Vp-p (NRZ) 0.3 to 1.0 Vp-p (PAM4, ≤ 28.1 Gbaud) 0.4 to 1.0 Vp-p (PAM4, > 28.1 Gbaud)
Threshold voltage	–3.5 to +3.3 V (1mV step) (Can be set separately.) (Absolute value of difference between Data and XData Threshold values shall be 3 V or less.)

*1: Option x10

*2: Option x20

*3: Absolute value of difference between Data and XData Threshold values shall be 1.5 V or less.

*4: Option x11 or Option x21

*5: The NRZ input amplitude is the range where the Auto Adjust function operates. The PAM4 input amplitude is the range where the PAM4 Auto Search function operates. Input sensitivity is the minimum input amplitude which becomes error-free.

Table 1.3.2-3 Data Input (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Input sensitivity</td><td>
NRZ*5,*6,*7
<table>
<tr><th></th><th colspan="2">Bitrate</th></tr>
<tr><th></th><th>21.0 Gbit/s</th><th>28.1Gbit/s*8</th></tr>
<tr><td>Amplitude</td><td>19 mVp-p*9, ≤27 mVp-p</td><td>22 mVp-p*9, ≤31 mVp-p</td></tr>
<tr><td>Eye height*10</td><td>13 mV*9</td><td>15 mV*9</td></tr>
</table>
PAM4*5,*7,*11
<table>
<tr><th></th><th colspan="2">Baud rate</th></tr>
<tr><th></th><th>21.0 Gbaud</th><th>28.1 Gbaud*8</th></tr>
<tr><td>Amplitude</td><td>120 mVp-p*9, 40 mV/Eye</td><td>150 mVp-p*9, 50 mV/Eye</td></tr>
<tr><td>Eye height</td><td>24 mV*9</td><td>26 mV*9</td></tr>
</table>
</td></tr>
</table>

*6: PRBS31, Single-Ended, Mark ratio 1/2, CTLE OFF

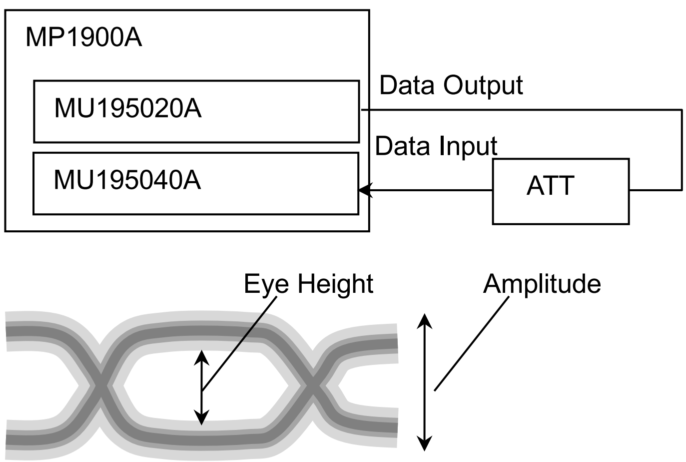
*7: Defined by one specific temperature in the range of 20 to 30°C.

*8: Option x01

*9: Typical value

*10: Sensitivity of eye height.

Eye height is the minimum value that induces no bit error when MU195040A receives the output signal from MU195020A + ATT in the measurement system shown in the following figure (using a sampling oscilloscope of 70 GHz band or higher for measuring output amplitude).



*11: PRBS15, Single-Ended, marking rate equivalent to 1/2, CTLE OFF, MU195020A + G375A and back-to-back connection

Table 1.3.2-3 Data Input (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Phase margin</td><td>NRZ*6,*12
<table>
<tr><th></th><th colspan="4">Bitrate</th></tr>
<tr><th></th><th>21.0 Gbit/s</th><th>25.0 Gbit/s*8</th><th>28.1 Gbit/s*8</th><th>32.1 Gbit/s*8</th></tr>
<tr><td>Phase margin</td><td>33 ps*9</td><td>27 ps*9</td><td>20 ps*9</td><td>18 ps*9</td></tr>
</table>
PAM4 Middle*11,*13
<table>
<tr><th></th><th colspan="4">Baud rate</th></tr>
<tr><th></th><th>21.0 Gbaud</th><th>25.0 Gbaud*8</th><th>28.1 Gbaud*8</th><th>32.1 Gbaud*8</th></tr>
<tr><td>Phase margin</td><td>13 ps*9</td><td>8 ps*9</td><td>5 ps*9</td><td>2 ps*9</td></tr>
<tr><td>Eye width</td><td>26.5 ps*9</td><td>20 ps*9</td><td>15 ps*9</td><td>13 ps*9</td></tr>
</table>
PAM4 Upper/Lower*11,*13
<table>
<tr><th></th><th colspan="3">Baud rate</th></tr>
<tr><th></th><th>21.0 Gbaud</th><th>25.0 Gbaud*8</th><th>28.1 Gbaud*8</th></tr>
<tr><td>Phase margin</td><td>8 ps*9</td><td>5 ps*9</td><td>3 ps*9</td></tr>
<tr><td>Eye width</td><td>26.5 ps*9</td><td>20 ps*9</td><td>15 ps*9</td></tr>
</table>
</td></tr>
<tr><td>Termination</td><td>GND,50 Ω,
Variable,50 Ω</td></tr>
<tr><td>Termination voltage
Connector
CTLE*4
Band
CTLE Gain
Setting range
Accuracy
Input amplitude</td><td>When Variable is selected for Termination: –2.5 to +3.5 V, 10 mV step
K (f.)

OFF, 8-10 Gbit/s, 16-20 Gbit/s, 25-28 Gbit/s, PCIe3, PCIe4, PCIe5

0 to –12 dB, 0.1 dB step
±0.5 dB*9
0.05 to 0.4 Vp-p*14</td></tr>
</table>

*12: When using 0.5 Vp-p Input and External Clock.

*13: Emphasis ON (Best value in the range of 1Pre ≤ 3 dB/1 Post ≤ 1 dB), Based on the IEEE802.3bs measurement methods

*14: Input range that the signal is not saturated when CTLE is On.

Table 1.3.2-4 Clock Input

Item	Specifications
Number of inputs	1 (Single-Ended)
Frequency range	1.2 to 16.05 GHz
Input level	0.3 to 1.0 Vp-p (–6.5 to +4.0 dBm)
Termination	AC, 50 Ω
Connector	SMA (f.)

Table 1.3.2-5 Aux Input, Aux Output

Item	Specifications
Aux Input	
Number of inputs	1 (Single-Ended)
Variation	External Mask, Burst, Capture External Trigger
Minimum pulse width	1/128 of Data rate
Input level	• 0/–1 V (H: –0.25 to 0.05 V / L: –1.1 to –0.8 V) • 0/–0.5 V (H: –0.05 to 0.05 V / L: –0.55 to –0.45 V) • Vth 0 V (Input amplitude 0.5 to 1.0 Vp-p) Select one of the above.
Termination	GND, 50 Ω
Connector	SMA (f.)
Aux Output	
Number of outputs	2 (Differential)
Variation	1/n Clock (n = 4, 6, 8, 10…510, 512), Pattern Sync*, Sync. Gain, Error Output
Pattern Sync	
PRBS, PRGM	Position: 1 to {(Least common multiple of Pattern Length’ and 128) – 135}, in 8-bit steps Pattern Length’ shall be the value obtained by multiplying Pattern Length setting until it becomes 512 or more if it is 511 or less.
Mixed Data	Block No. setting: 1 to the Block No. specified for Mixed Data, in 1-steps Row No. setting: 1 to the Row No. specified for Mixed Data, in 1-steps
Output level	0/–0.6 V (H: –0.25 to 0.05V / L: –0.80 to –0.45 V)
Termination	GND, 50 Ω
Connector	SMA (f.)

*: Cannot be selected when Test Pattern is HSSB Data.

Table 1.3.2-6 Pattern Detection

Item	Specifications
PRBS	
Pattern length	2^n-1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31)
Mark ratio	1/2 (1/2INV is supported by a logical inversion.)
Zero-Substitution	
Additional Bit	0 bit, 1 bit
Pattern length	2^n or 2^n-1 (n = 7, 9, 10, 11, 15, 20, 23)
Start position	Substitutes the bit coming after the maximum "0" successive bits.
Successive-zeros bit length	1 to (Pattern Length–1) bits If the bit coming after Zero-substitution is "0," then it is replaced with "1."
Data	
Data length	2 to 268435456 bits, in 1-bit steps
Mixed Pattern	
Pattern	Data
Mixed Block	To the smaller of the following values: 1 to 511 Block, in 1-Block steps $\mathrm{INT}\left(\frac{268435456}{\mathrm{ROW\ count}}\times \mathrm{Data\ length}\right)$ bits $\mathrm{INT}\left(\frac{268435456+2^{31}}{\mathrm{ROW\ length}}\times \mathrm{ROW\ count}\right)$ bits
Mixed Row Length	2048 to 268435456+2^{31} bits, in 1024-bit steps (Data + PRBS Length)
Data length	1024 to 268435456 bits, in 1-bit steps
Number of rows	1 to 16, in 1-steps
Number of blocks	1 to 511, in 1-steps
PRBS steps/Mark ratio	Same as PRBS.
PRBS Sequence	Restart, Consecutive
Descramble	Can be set per PRBS and Data for each Block (except the Data area for Block 1).
PAM4 *1	
Pattern Type	Square Wave, JP03A, JP03B, PRQS10, SSPR, QPRBS13, QPRBS13-CEI, SSPRQ, Transmitter Linearity, PRBS13Q, PRBS31Q, User Define
User Define in detail	
Raw Data	PRBS, Data
PRBS Pattern Length	Same as PRBS.
PRBS Inversion	Logic Inversion/Non-Inversion of PRBS part
Data Length	Same as Data
Gray Coding	Gray Coding ON/OFF

*1: Configurable when 2ch Combination is set

Table 1.3.2-6 Pattern Detection (Cont'd)

Item	Specifications
HSSB Data*2	
Specification	PCIe1, PCIe2, PCIe3, PCIe4, USB3.0, USB3.1 Gen2
EIEOS	EIEOS Insertion: ON,OFF EIEOS Interval: 1 to 65536 pattern repeats, 1 step Enabled when Specification is PCIe1, PCIe2, PCIe3, and PCIe4 When Specification is PCIe3 or PCIe4, only ON is available for EIEOS Insertion.
SYNCOS	SYNC OS Insertion: ON, OFF SYNC OS Interval: 1 to 65536 pattern repeats, 1 step When Specification is USB3.0, only OFF is available. Enabled when Specification is USB3.1 Gen2.
Scrambler Seed	When Specification is set to PCIe1, PCIe 2, or USB3.0: FFFF When Specification is set to PCIe3, or PCIe4: Lane0, Lane1, Lane2, Lane3, Lane4, Lane5, Lane6, Lane7 When Specification is set to USB3.1 Gen2: 1DBFBC
PCIe1	
Length	32 to 1024 bit, 8bit step
Coding	8b10b
PCIe2	
Length	32 to 1024 bit, 8bit step
Coding	8b10b
PCIe3	
Length	128 to 1024 bit, 128bit step
Coding	128b130b
PCIe4	
Length	128 to 1024 bit, 128bit step
Coding	128b130b
USB3.0	
Length	32 to 1024 bit, 8bit step
Coding	8b10b
USB3.1 Gen2	
Length	128 to 1024 bit, 128bit step
Coding	128b132b

*2: This can be set only when Module Combination is set to Independent and the channel is Data1.

Table 1.3.2-6 Pattern Detection (Cont'd)

Item	Specifications
HSSB Data*2 (Cont'd)	
8b10b Pattern Editor	
Notation	Symbol, Bin, Hex
Scrambler Enable	Scrambles the selected symbols. ON, OFF
Scrambler Reset	Resets the seed value of scrambler on the selected symbols. ON, OFF
Code	K-code, D-code
K code	K28.0, K28.1, K28.2, K28.3, K28.4, K28.5, K28.6, K28.7 K23.7, K27.7, K29.7, K30.7
D code	D0.0 to D31.7
MSB First / LSB First	MSB First, LSB First
128b130b Pattern Editor	
Notation	Bin, Hex
Scrambler Enable	Scrambles the selected symbols. ON, OFF
Scrambler Reset	Resets the seed value of scrambler on the selected symbols. ON, OFF
DC Balance	Adds DC balance to the symbol 14 and 15. ON, OFF
Sync Header	Defines 2-bits Sync Header.
MSB First / LSB First	MSB First, LSB First
128b132b Pattern Editor	
Notation	Symbol Bin, Symbol Hex
Scrambler Enable	Scrambles the selected symbols. ON, OFF
Scrambler Reset	Resets the seed value of scrambler on the selected symbols. ON, OFF
DC Balance	Adds DC balance to the symbol 14 and 15. ON, OFF
Sync Header	Defines 4-bits Sync Header.
MSB First / LSB First	MSB First, LSB First

Table 1.3.2-7 Pattern Sequence

Item	Specifications	
Sequence	Repeat, Burst	
Repeat	Continuous Pattern	
Burst		
Source	Internal, External-Trigger (Aux Input), External-Enable (Aux Input)	
Delay	Internal:	0 to 2147483640 bits, in 8-bit steps
	Ext Trigger, Enable:	0 to 2147483520 bits, in 8-bit steps
	Adjust Method:	Auto, Manual
Enable Period	Internal:	12800 to 2147482624 bits, in 256-bit steps
	Ext Trigger:	12800 to 2147483392 bits, in 256-bit steps
Burst Cycle	25600 to 2147483648 bits, in 1024-bit steps	

Table 1.3.2-8 Measurement

Item	Specifications	
Measurement types	Error Rate:	0.0001E–18 to 1.0000E00
	Error Count:	0 to 9999999, 1.0000E07 to 9.9999E17
	Error Interval:	0 to 9999999, 1.0000E07 to 9.9999E17
	%Error Free Interval:	0.0000 to 100.0000
	Frequency:	2400.000 to 32100.000 MHz
	Frequency measurement accuracy:	±1 ppm ±1 kHz*
	Clock Count:	0 to 9999999, 1.0000E07 to 9.9999E17
	Sync Loss Interval:	0 to 9999999, 1.0000E07 to 9.9999E17
	Clock Loss Interval:	0 to 9999999, 1.0000E07 to 9.9999E17
Gating	Time, Clock Count, Error Count, Block Count	
Unit, Cycle setting	Time:	1 second to 99 days 23 hours 59 minute 59 seconds
	Clock Count:	> E+4 to > E+16
	Error Count:	> E+4 to > E+16
	Block Count:	> E+2 to > E+14
Gating Cycle	Single, Repeat, Untimed	
Current	On, Off can be set.	
	Calculation:	Progressive, Immediate
	Interval:	100 ms, 200 ms, 500 ms
Auto Sync	On, Off can be set.	
	Synchronization threshold:	INT, E–2 to E–8
Sync Control	PRBS:	Automatic Synchronization
	Data:	Frame On, Quick
	Mixed-Data:	Frame On
	HSSB Data:	Automatic Synchronization
Frame length	4 to 64 bits, in 4-bit steps	
Frame mask	Available	
Frame Position	1 to (Pattern Length – Frame Length +1) bits, in 1-bit steps	
Error/Alarm conditions		
Error detection mode	• Total, Insertion, Omission • Transition, Non Transition	
EI/EFI interval	1 ms, 10 ms, 100 ms, 1 s	
SKP OS Filtering	Filters the SKP OS that are compliant with the following standards: • PCIe: Gen1, Gen2, Gen3, Gen4, Gen5 This function is available only at the bit rate of each standard. When Test pattern is HSSB Data, only ON is enabled.	

*: When Gating is selected and the MP1900A reference clock 10 MHz is calibrated.

Table 1.3.2-9 Error Analysis

Item	Specifications
Block Window	Excludes the specified data pattern bit from the measurement target according to the settings. Invalid when "Mixed" pattern or "HSSB Data" is selected for Test Pattern.
Setting resolution	Pattern length (bits) / Step [bits] 2 to 2097152 / 1 2097153 to 4194304 / 2 4194305 to 8388608 / 4 8388609 to 16777216 / 8 16777217 to 33554432 / 16 33554433 to 67108864 / 32 67108865 to 134217728 / 64 134217729 to 268435456 / 128
Bit window*1	Excludes any channels among internal 32 channels from the measurement target.
External mask*1	H: Measurement L: Mask
Capture function*1	
Number of blocks	1, 2, 4, 8, 16, 32, 64, 128
Length of block	$\frac{8\text{Mbits}}{n}$ (n is Number of blocks.)
Trigger	Error Detect, Match Pattern, Manual Trigger, External Trigger (Rising Edge)
Trigger position	Top, Middle, Bottom
Matching pattern	4 to 64, in 4-bit steps
Automatic measurement function	Eye margin*1,*2, Bathtub*1,*2, Eye Contour*1,*2, PAM4 BER measurement Auto Adjust*3,*4,*5, Auto Search*3, Auto Search PAM4 mode*6

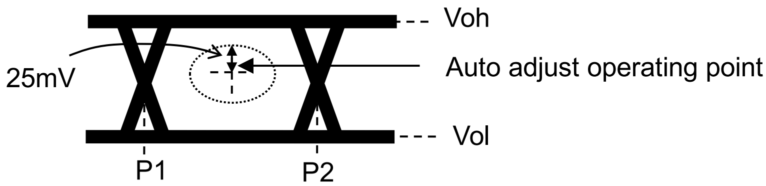
*1: Not available when "HSSB Data" is selected for Test Pattern.

*2: Unavailable when the system clock is set to Clock and Data Recovery.

*3: The input pattern must be an NRZ PRBS pattern with a mark ratio of 1/2.

*4: The Auto Adjust function obtains a point in the vicinity of the following as an optimum point:
- (Voh + Vol) / 2 in voltage direction
- (P1 + P2) / 2 in phase direction

The Auto Adjust function works properly when there are no mask-hits which are observed by the oscilloscope vertically within ±25 mV area from the Auto Adjust operating point.



*5: If eye diagram of input signal is not symmetry, the Auto Adjust may not adjust input signals to the optimum value. The Auto Search Fine is recommended to measure asymmetric input signals.

*6: Each of PAM4 waveform levels is equal. PRBS pattern with a mark ratio of 1/2.

Table 1.3.2-10 PAM4 BER Measurement

Item	Specifications
PAM4 BER Measurement	Available patterns ・ GrayPRBS7, 9, 10, 11, 13Q-IEEE200G_400G[Draft2], 15,20 ・ GrayPrePRBS20 ・ GrayPreQPRBS13-CEI ・ GrayPreQPRBS13-IEEE100GBASE-KP4_Lane0, 1, 2, 3 ・ GrayPRQS10 ・ GrayQPRBS13-CEI ・ GrayQPRBS13-IEEE100GBASE-KP4_Lane0, 1, 2, 3 ・ GraySSPR ・ PRBS7, 9, 10, 11, 13Q-IEEE200G_400G[Draft2], 15, 20 ・ PrePRBS20 ・ PreQPRBS13-CEI ・ PRQS10 ・ QPRBS13-CEI ・ QPRBS13-IEEE100GBASE-KP4_Lane0, 1, 2, 3 ・ Squarewave ・ SSPR ・ SSPRQ ・ Transmitter_Linearity

Table 1.3.2-11 Variable Clock Delay

Item	Specifications
Phase variable range	–1000 to +1000 mUI, 2 mUI step
Accuracy	±50 mUIp-p*1,*2
mUI – ps switching	Available
Calibration	Available
Calibration indicator	This indicator is on when Calibration is required due to: • Change in 1/1Clock frequency by ±250 kHz. • Change in the ambient temperature by ±5°C.

*1: Using oscilloscope with residual jitter of less than 200 fs (RMS).

*2: Typical value

Table 1.3.2-12 Clock Recovery

<table>
<tr><th>Item</th><th colspan="2">Specifications</th></tr>
<tr><td>Clock source options</td><td colspan="2">Clock Recovery, Clock and Data Recovery Clock*1</td></tr>
<tr><td rowspan="2">Operating bit rate</td><th>NRZ</th><th>PAM4</th></tr>
<tr><td>2.4 to 21.0 Gbit/s*2
2.4 to 32.1 Gbit/s*3</td><td>2.4 to 21.0 Gbaud*2
2.4 to 28.1 Gbaud*3
28.100 001 to 32.1 Gbaud*3,*4</td></tr>
<tr><td>Setting range</td><td colspan="2">2.400000 to 21.000000 Gbit/s, 0.000001 Gbit/s step*2
2.400000 to 32.100000 Gbit/s, 0.000001 Gbit/s step*3</td></tr>
</table>

*1: The system clock can be selected only when option x22 is installed.
Clock is recovered from the data input to the Data1 Input connector.
The input pattern must be an NRZ PRBS pattern with a mark ratio of 1/2.
When PAM4 is set, clock recovery is performed with PRBS15, Data1 and Middle. Upper, Middle, Lower are measured with Data2.
At the back-to-back connection with MU195020A + J1741A + G0375A + J1728A, the target loop band is defined at the maximum bit rate of each Bit rate range.

*2: When option x22 is installed.

*3: When option x01 is installed.

*4: Typical value, BER 1.0E–7

Table 1.3.2-12 Clock Recovery (Cont'd)

Item	Specifications	
Supported standard and bit rate	Standard	Bit rate [Gbit/s]
	100G ULH	32.100000*3
	PCI Express Gen5	32.000000*3
	32GFC	28.050000*3
	100G OTU4	27.952496*3
	100GbE(25.78x4)	25.781250*3
	InfiniBand EDR	25.781250*3
	SAS	24.000000*3
	SAS4	22.500000*3
	Thunderbolt2	20.625000
	DisplayPort UHBR 20	20.000000
	USB4 Gen3	20.000000
	PCI Express Gen4	16.000000
	InfiniBand FDR	14.062500
	16G FC	14.025000
	DisplayPort UHBR 13.5	13.500000
	10G FC Over FEC	11.316800
	10GbE Over FEC	11.095700
	OTU2	10.709225
	G975 FEC	10.664228
	10G FC	10.518750
	10GbE	10.312500
	Thunderbolt1	10.312500
	DisplayPort UHBR 10	10.000000
	USB4 Gen2	10.000000
	InfiniBand QDR	10.000000
	USB3.1	10.000000
	OC-192/STM-64	9.953280
	8G FC	8.500000
	DisplayPort HBR3	8.100000
	PCI Express Gen3	8.000000
	HSBI	6.250000
	SATA 6Gb/s	6.000000
	DisplayPort HBR2	5.400000
	PCI Express Gen2	5.000000
	USB3.0	5.000000
	InfiniBand DDR	5.000000
	4G FC	4.250000

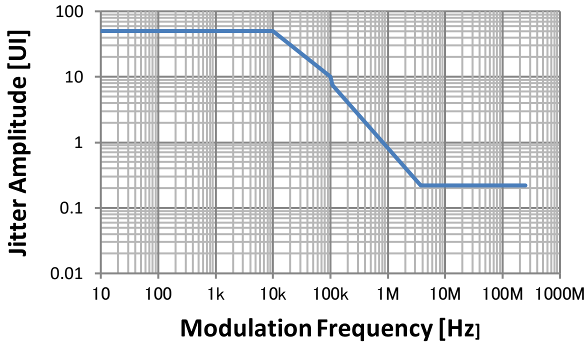
Table 1.3.2-12 Clock Recovery (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Supported standard and bit rate (Cont'd)</td><td>
<table>
<tr><th>Standard</th><th>Bit rate [Gbit/s]</th></tr>
<tr><td>XAUI</td><td>3.125000</td></tr>
<tr><td>SATA 3Gb/s</td><td>3.000000</td></tr>
<tr><td>DisplayPort HBR</td><td>2.700000</td></tr>
<tr><td>OTU1</td><td>2.666060</td></tr>
<tr><td>InfiniBand SDR</td><td>2.500000</td></tr>
<tr><td>PCI Express Gen1</td><td>2.500000</td></tr>
<tr><td>OC-48/STM-16</td><td>2.488320</td></tr>
</table>
</td></tr>
<tr><td>Operating bit rate tracking</td><td>Supported.
Tracking target: The operating bit rate of the PPG mounted to the same mainframe</td></tr>
<tr><td>Maximum number of consecutive zeros*5</td><td>72 bit (Zero Substitution 2^{15})</td></tr>
<tr><td>Lock range*5</td><td>±200 ppm</td></tr>
<tr><td>Target loop band</td><td>Available options are $\frac{\text{Bit rate}}{1667}$ MHz, $\frac{\text{Bit rate}}{2578}$ MHz, Jitter Tolerance*6 and Variable.
If the Variable option is selected, the following settings are available:
<table>
<tr><th>Bit rate [Gbit/s]</th><th>Setting Range [MHz]</th><th>Step [MHz]</th></tr>
<tr><td>2.400000 to 5.500000</td><td>3</td><td>-</td></tr>
<tr><td>5.500001 to 7.500000</td><td>3 to 4</td><td>1</td></tr>
<tr><td>7.500001 to 9.500000</td><td>3 to 5</td><td>1</td></tr>
<tr><td>9.500001 to 10.500000</td><td>3 to 6</td><td>1</td></tr>
<tr><td>10.500001 to 12.500000</td><td>3 to 7</td><td>1</td></tr>
<tr><td>12.500001 to 14.500000</td><td>3 to 8</td><td>1</td></tr>
<tr><td>14.500001 to 15.500000</td><td>3 to 9</td><td>1</td></tr>
<tr><td>15.500001 to 17.500000</td><td>3 to 10</td><td>1</td></tr>
<tr><td>17.500001 to 19.500000</td><td>3 to 11</td><td>1</td></tr>
<tr><td>19.500001 to 20.500000</td><td>3 to 12</td><td>1</td></tr>
<tr><td>20.500001 to 22.500000</td><td>3 to 13</td><td>1</td></tr>
<tr><td>22.500001 to 24.500000</td><td>3 to 14</td><td>1</td></tr>
<tr><td>24.500001 to 25.500000</td><td>3 to 15</td><td>1</td></tr>
<tr><td>25.500001 to 27.500000</td><td>3 to 16</td><td>1</td></tr>
<tr><td>27.500001 to 29.500000</td><td>3 to 17</td><td>1</td></tr>
<tr><td>29.500001 to 30.500000</td><td>11 to 18</td><td>1</td></tr>
<tr><td>30.500001 to 32.100000</td><td>11 to 19</td><td>1</td></tr>
</table>
</td></tr>
</table>

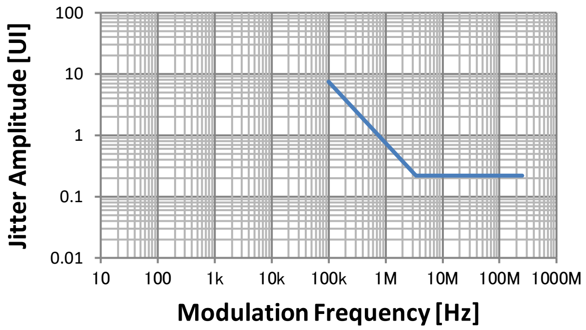
*5: When the option x22 is installed:
The target loop band is specified by the maximum setting value of each bit rate.

*6: The Jitter Tolerance option makes the loop band wider than the other options and enables the Jitter Tolerance measurement.

Table 1.3.2-12 Clock Recovery (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Jitter Tolerance
Clock Recovery*7,*8</td><td>At the bit rate of 28.05 Gbit/s, conforming to Jitter Tolerance Mask defined by the "32G FC standard"


<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Tolerance Mask (UIp-p)</th></tr>
<tr><td>10</td><td>50</td></tr>
<tr><td>10,000</td><td>50</td></tr>
<tr><td>100,000</td><td>10</td></tr>
<tr><td>108,805</td><td>7.5</td></tr>
<tr><td>3,709,271</td><td>0.22</td></tr>
<tr><td>250,000,000</td><td>0.22</td></tr>
</table>

At the bit rate of 25.78125 Gbit/s, conforming to Jitter Tolerance Mask defined by the "100GbE (25.78 × 4) standard"


<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Tolerance Mask (UIp-p)</th></tr>
<tr><td>100,000</td><td>7.5</td></tr>
<tr><td>3,409,256</td><td>0.22</td></tr>
<tr><td>250,000,000</td><td>0.22</td></tr>
</table>
</td></tr>
</table>

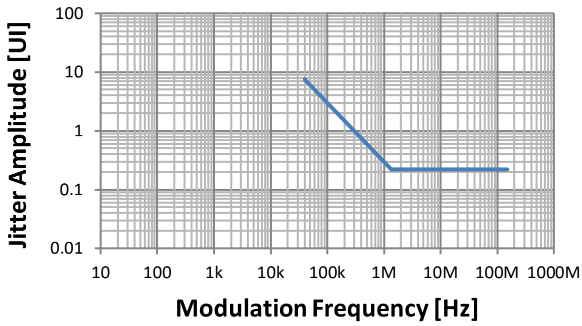
*7: Defined assuming the following conditions:
- Loop-back connection to MU195020A
- Test Pattern (Length): PRBS (2^31–1)
- Data input amplitude: 0.05 Vp-p

*8: Typical value, specified at 20 to 30°C

Table 1.3.2-12 Clock Recovery (Cont'd)

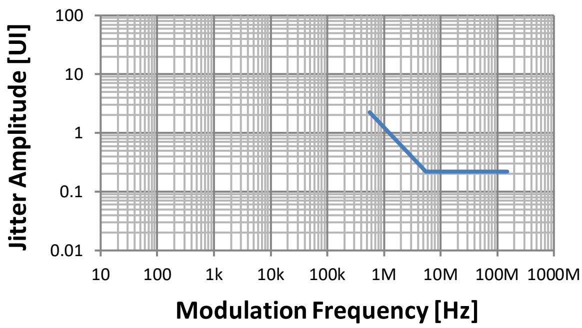
<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Jitter Tolerance
Clock Recovery (Cont'd)</td><td>

At the bit rate of 14.0625 Gbit/s, conforming to Jitter Tolerance Mask defined by the "Infiniband FDR standard"



Modulation Frequency (Hz)	Jitter Tolerance Mask (UIp-p)
40,000	7.5
1,363,636	0.22
150,000,000	0.22

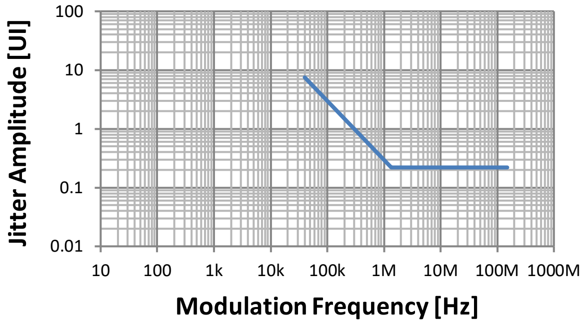
At the bit rate of 14.025 Gbit/s, conforming to Jitter Tolerance Mask defined by the "16G FC standard"



Modulation Frequency (Hz)	Jitter Tolerance Mask (UIp-p)
561,000	2.25
5,535,929	0.22
150,000,000	0.22

</td></tr>
</table>

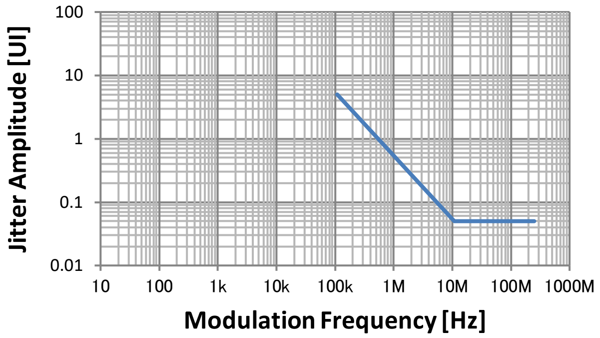
Table 1.3.2-12 Clock Recovery (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Jitter Tolerance
Clock Recovery (Cont'd)</td><td>At the bit rate of 10.3125 Gbit/s, conforming to Jitter Tolerance Mask defined by the "10GbE standard"


<table><tr><th>Modulation Frequency (Hz)</th><th>Jitter Tolerance Mask (UIp-p)</th></tr><tr><td>40,000</td><td>7.5</td></tr><tr><td>1,363,636</td><td>0.22</td></tr><tr><td>150,000,000</td><td>0.22</td></tr></table></td></tr>
</table>

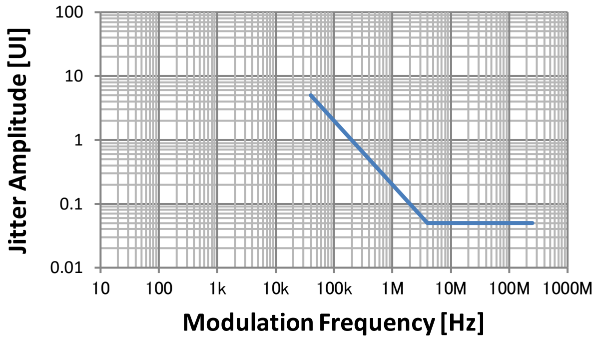
Table 1.3.2-12 Clock Recovery (Cont'd)

Item	Specifications
Jitter Tolerance Data Clock Recovery	SSC with 5300 ppm amplitude can be simultaneously applied by using MU181500B. At the bit rate of 28.05 Gbit/s



Modulation Frequency (Hz)	Jitter Tolerance Mask (UIp-p)
108,805	5
10,880,528	0.05
250,000,000	0.05

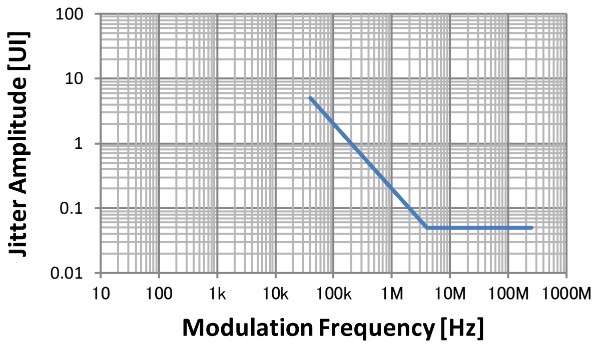
At the bit rate of 25.78125 Gbit/s



Modulation Frequency (Hz)	Jitter Tolerance Mask (UIp-p)
40,000	5
4,000,000	0.05
250,000,000	0.05

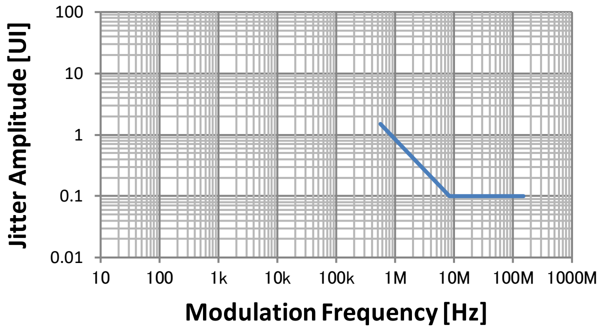
Table 1.3.2-12 Clock Recovery (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Jitter Tolerance
Data Clock Recovery
(Cont'd)</td><td>
At the bit rate of 14.0625 Gbit/s



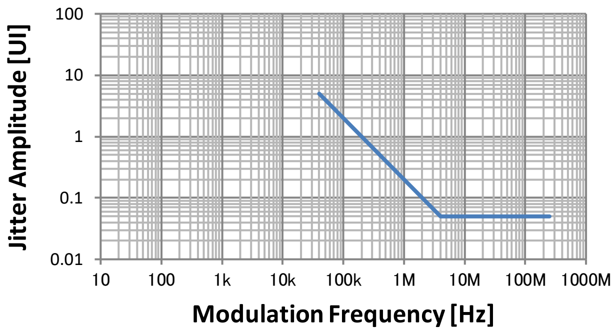
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Tolerance Mask (UIp-p)</th></tr>
<tr><td>40,000</td><td>5</td></tr>
<tr><td>4,000,000</td><td>0.05</td></tr>
<tr><td>150,000,000</td><td>0.05</td></tr>
</table>

At the bit rate of 14.025 Gbit/s



<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Tolerance Mask (UIp-p)</th></tr>
<tr><td>561,000</td><td>1.5</td></tr>
<tr><td>8,413,317</td><td>0.1</td></tr>
<tr><td>150,000,000</td><td>0.1</td></tr>
</table>
</td></tr>
</table>

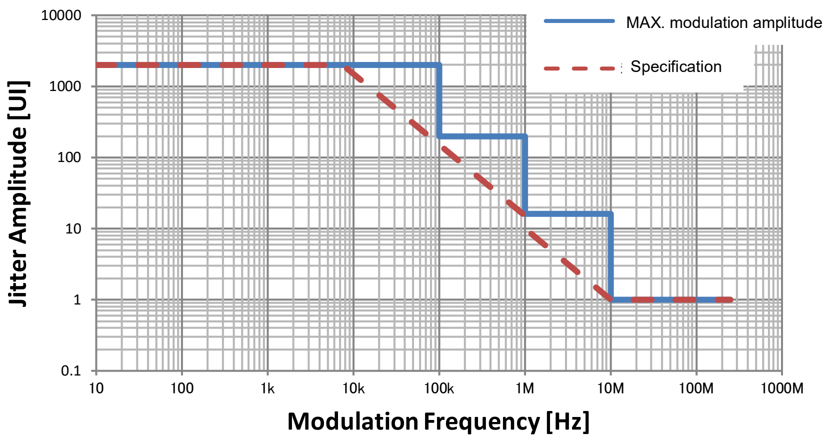
Table 1.3.2-12 Clock Recovery (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Jitter Tolerance
Clock Recovery (Cont'd)</td><td>At the bit rate of 10.3125 Gbit/s


<table><tr><th>Modulation Frequency (Hz)</th><th>Jitter Tolerance Mask (UIp-p)</th></tr><tr><td>40,000</td><td>5</td></tr><tr><td>4,000,000</td><td>0.05</td></tr><tr><td>250,000,000</td><td>0.05</td></tr></table></td></tr>
</table>

Table 1.3.2-13 Jitter Tolerance

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Jitter tolerance
When using external clock</td><td>Bit rate: 16 Gbit/s, 28.1 Gbit/s*, 32.1 Gbit/s*
Pattern: PRBS2^{31}–1
SSC with a 5300 ppm amplitude and RJ of 0.3 UI can be simultaneously applied by using MU181500B.
These specifications are defined assuming the following conditions:
Loopback connection to the MU195020A, defined by one specific temperature in the range of 20 to 30°C.
When RJ+BUJ is bigger than 0.5 UIp-p or SJ + RJ + BUJ is bigger than the standard value + 0.3 UIp-p, “Overload” is displayed on the MU181500B screen.



<table>
<tr><th>Modulation frequency [Hz]</th><th>MAX. modulation amplitude [UIp-p]</th><th>Specification [UIp-p]</th></tr>
<tr><td>10</td><td>2,000</td><td>2,000</td></tr>
<tr><td>7,500</td><td>2,000</td><td>2,000</td></tr>
<tr><td>100,000</td><td>2,000</td><td>150</td></tr>
<tr><td>1,000000</td><td>200</td><td>15</td></tr>
<tr><td>10,000,000</td><td>16</td><td>1</td></tr>
<tr><td>250,000,000</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
</table>

*: When option x01 is installed.

Table 1.3.2-14 Multichannel operation*1

Item	Specifications		
Combination*2			
Number of channels	2		
Pattern	At Combination n = 2 below (2ch combination)		
Data			
Data Length	2 × n to 268435456 × n bits, in n-bit steps*3		
Mixed			
Row Length	2048 × n to (268435456+2^{31}) × n bits, in 1024 × n bit steps*3		
Data Length	1024 × n to 268435456 × n bits, in n-bit steps*3		
HSSB Data	Not available for combination.		
Block Window	Excludes the specified data pattern bit from the measurement target according to the settings. (Mask measurement function) Invalid when “Mixed” is selected for Test Pattern. Invalid when Zero-substitution is set to “2^n–1”. n = 2 (2ch Combination) is considered in the following:		
Setting resolution		Pattern length (bits)	Step [bits]
		2 to 2 097 152 × n	1 × n
		2 097 153 to 4 194 304 × n	2 × n
		4 194 305 to 8 388 608 × n	4 × n
		8 388 609 to 16 777 216 × n	8 × n
		16 777 217 to 33 554 432 × n	16 × n
		33 554 433 to 67 108 864 × n	32 × n
		67 108 865 to 134 217 728 × n	64 × n
		134 217 729 to 268 435 456 × n	128 × n
Burst			
Burst Cycle	25600 × n to 2147483648 × n bits, in 1024 × n bit steps*3		
Enable Period	Internal:	12800 × n to 2147482624 × n bits, in 256 × n bit steps*3	
	Ext Trigger:	12800 × n to 2147483392× n bits, in 256 × n bit steps*3	
Delay	Internal:	0 to 2147483640 × n bits, in 8 × n bit steps*3	
	Ext Trigger, Enable:	0 to 2147483520 × n bits, in 8 × n bit steps*3	
Measurement			
Sync Control			
Frame length	4 × n to 64 × n bits, in 4 × n bit steps*3		
Frame Position	1 to (Pattern Length' – Frame Length + n) bits, in n-bit steps		

*1: Cannot be set when Test Pattern is HSSB Data.

*2: Combination extending over multiple slots cannot be set.

*3: Common to every channel specified by Combination Setting.

Table 1.3.2-15 Multichannel operation (Cont'd)

Item	Specifications
Error detection mode	Total, Insertion, and Omission
Eye Contour	
Measurement target	Data 1 to Data n*4
Eye Margin	
Measurement target	Data 1 to Data n*4
Bathtub	
Measurement target	Data 1 to Data n*4
Capture	2 Ch Combination is available*3

*4: Separately specified for each channel.

Table 1.3.2-16 General

Item	Specifications
Dimensions	21 mm (H), 234 mm (W), 175 mm (D), Excluding protrusions
Mass	2.5 kg max.
Operating temperature	15 to 35°C
Storage temperature	–20 to 60°C

Table 1.3.2-17 Extension Function

Item	Specifications
PCIe	
Supported standards	PCI Express Base Specification Revision 4.0 Version 0.5, 0.7, 1.0 PCI Express Base Specification Revision 5.0 Version 1.0 Bitrate: PCIe Gen1, Gen2, Gen3, Gen4, Gen5 Lane number: ×1 Test target: Root Complex, End Point
Required option	Option x10/x11/x22 or x20/x21/x22
Required software	MX183000A-PL011: This software enables setting DUT to Loopback state by following PCIe LTSSM and generating a training sequence required for transition to Loopback state. MX183000A-PL021: This software enables setting DUT to Loopback state by following PCIe LTSSM and supporting negotiation with DUT. LTSSM state transition can be analyzed as log. (One MU195020A and one MU195040A are required for this software.) MX183000A-PL025: This software enables extending the functionality of PL021 to PCIe 5.0. Adding MX183000A-PL001 to each option of the above software enables controlling MU195020A, MU181500B, MU195040A and supporting Jitter Tolerance Test.

Table 1.3.2-17 Extension Function (Cont'd)

Item	Specifications
Loopback Through	Configuration, Recovery
Test Pattern	Modified Compliance Pattern Insert Delay Symbol: Enable, Disable (Available for Gen1 and Gen2) Insert SRIS: Enable, Disable (Available for Gen3 and Gen4) Compliance Pattern Insert Delay Symbol: Enable, Disable (Available for Gen1 and Gen2) User PRBS, Data
SKP Ordered Set Insertion	Enable, Disable
SKP Length/Insertion	For Gen1, Gen2 Length: COM+1, COM+2, COM+3, COM+4, COM+5 Interval: 768 to 3076, in 1-steps For Gen3, Gen4, Gen5 Length: 8, 12, 16, 20, 24 Interval: 187 to 750, in 1-steps
Dynamic Link Training	Available when using MX183000A-PL021.
Counter	Tx SKP Count, Rx SKP Count (when using MX183000A-PL021) Error Rate, Error Count (when using MX183000A-PL021)
LTSSM Log	
Log Item	LTSSM State, Link Speed, Time[ns]
Log Size	16384 times
Termination condition	Memory full

1.3.3 Specifications for MU195050A

Table 1.3.3-1 Operating bit rate

Item	Specifications
Operating bit rate	2.4 to 32.1 Gbit/s

Table 1.3.3-2 Data Input

Item	Specifications
Number of channels	2
Number of inputs per channel	2 (Data, XData) (Differential)
Input amplitude	1.5 Vp-p max. (Single-ended) 3.0 Vp-p max. (Differential)
Offset	–2.0 to 3.3 V
Impedance	50 Ω
Connector	K (f.)

Table 1.3.3-3 Data Output*1

Item	Specifications
Number of channels	2
Number of outputs per channel	2 (Data, XData) (Differential)
Insertion loss	–3 dB +1/–2.5 dB*2
Impedance	50 Ω
Connector	K (f.)

*1: The signal that is output from the noise source is AC-coupled.

*2: Defined for 12.890625 GHz and sine wave.

Table 1.3.3-4 External Input*1

Item	Specifications
Number of channels	1*2
Number of inputs per channel	2 (Differential)
Input amplitude	1.5 Vp-p max. (Single-ended) 3.0 Vp-p max. (Differential)
Output control	Only Data Input 1 Channel can be turned On and Off. (Either DMI/CMI or White Noise is selectable.)
Termination	50 Ω, AC coupling
Connector	SMA Connector (f.)

*1: For connecting to G0373A USB3.1 Receiver Test Adapter or the Gating Output signal of MU195020A.

*2: Data Input 1 Channel only

Table 1.3.3-5 Differential Mode Interface (DMI)*1

Item	Specifications
Amplitude	4 to 200 mVp-p (Differential)*2
Amplitude setting step	1 mV
Amplitude accuracy	±20%±10mV*3
Frequency	2 to 10 GHz
Frequency setting step	10 MHz
Waveform	Sine wave
Presets	PCIe 3, PCIe 4, PCIe 5
Output control	Capability of switching ON/OFF of Data Input 1 Channel and Data Input 2 Channel simultaneously. (Either White Noise or External Input can be selected for Data Input 1 Channel) (Either Data Input 2 Channel or White Noise can be selected)

*1: The setting is common for Data Input 1 and Data Input 2.

*2: The setting is available from 0 mVp-p. (Accuracy is guaranteed from 4 mVp-p.)

*3: Defined at certain temperature between 20 to 30°C for 2.1 GHz, 4.2 GHz, 10 GHz.

Table 1.3.3-6 Common Mode Interface (CMI)*1

Item	Specifications
Amplitude	10 to 250 mVp-p (Single-ended)*2
Amplitude setting step	2 mV
Amplitude accuracy	±20%±25mV*3
Frequency	Low Band: 100 MHz to 1 GHz High Band: 1 to 6 GHz
Frequency setting step	Low Band: 1 MHz High Band: 10 MHz
Waveform	Sine wave
Presets	TBT3, PCIe 4, PCIe 5
Output control	Capability of switching ON/OFF of Data Input 1 Channel and Data Input 2 Channel simultaneously. (Either White Noise or External Input can be selected for Data Input 1 Channel) (Either Data Input 2 Channel or White Noise can be selected)

*1: The setting is common for Data Input 1 and Data Input 2.

*2: The setting is available from 0 mVp-p. (Accuracy is guaranteed from 10 mVp-p.)

*3: Defined at certain temperature between 20 to 30°C for 120 MHz, 400 MHz, 1 GHz, 6 GHz.

Table 1.3.3-7 White Noise*1

Item	Specifications
Flatness	±5 dB (10 MHz to 10 GHz)
Crest Factor	> 5 (p-p/rms)
Amplitude	0.2 to 25 mV rms
Amplitude setting step	0.2 mV rms
Amplitude accuracy	±20%±2.5 mV rms*2
ON/ OFF	Capability of switching ON/OFF of Data Input 1 Channel and Data Input 2 Channel simultaneously. (Either DMI/CMI or External Input can be selected for Channel 1) (Either Channel 2 or DMI/CMI can be selected)

*1: The setting is common for Data Input 1 and Data Input 2.

*2: Defined at one specific temperature between 20 to 30°C, subtracting the residual noise value from the data by sampling oscilloscope with 50 GHz bandwidth.

Table 1.3.3-8 General

Item	Specifications
Dimensions	21 mm (H), 234 mm (W), 175 mm (D), Excluding protrusions
Mass	1.2 kg max.
Operating temperature	15 to 35°C
Storage temperature	–20 to 60°C

Chapter 2 Before Use

This chapter describes preparations required before using the MP1900A modules.

2.1 Installation to MP1900A

For information on how to install the MP1900A modules to the MP1900A and how to turn on the power, refer to Chapter 3 "Preparation before Use" in the *MP1900A Signal Quality Analyzer-R Operation Manual*.

2.2 How to Operate Application

The modules connected to the MP1900A are controlled by operating the MX190000A Signal Quality Analyzer-R Control Software (hereinafter, referred to as "MX190000A").

For information on how to start up, shut down, and operate the MX190000A, refer to the *MX190000A Signal Quality Analyzer-R Control Software Operation Manual.*

2.3 Preventing Damage

Always observe the ratings when connecting to the input and output connectors of the MP1900A modules.
If an out-of-range signal is input, the MP1900A modules may be damaged.

⚠ CAUTION

- When signals are input to the MP1900A modules, avoid excessive voltage beyond the rating. Otherwise, the circuit may be damaged.
- When output is used at the 50 Ω GND terminator, never feed any current or input signals to the output.
- As a countermeasure against static electricity, ground other devices to be connected (including experimental circuits) with ground wires before connecting the I/O connector.
- The outer conductor and core of the coaxial cable may become charged as a capacitor. Use any metal to discharge the outer conductor and core before use.
- Never open the MP1900A modules. If you open it and MP1900A modules have failed or sufficient performance cannot be obtained, we may decline to repair the MP1900A modules.
- The MP1900A modules have many important circuits and parts including hybrid ICs. These parts are extremely sensitive to static electric charges, so never open the case of the MP1900A modules.
- The hybrid ICs used in the MP1900A modules are sealed in airtight containers; never open them. If you open it and the MP1900A modules have failed or sufficient performance cannot be obtained, we may decline to repair the MP1900A modules.
- To protect the MP1900A modules from electrostatic discharge failure, a conductive sheet should be placed onto the workbench, and the operator should wear an electrostatic discharge wrist strap. Always ground the wrist strap to the workbench antistatic mat or the frame ground of the MP1900A modules.

⚠ CAUTION

There is a risk of damaging connected devices and DUTs due to a voltage surge that can occur at module output terminals when powering on / off the MP1900A. Always follow the precaution below when preparing for measurement.

- **Do not power on / off the MP1900A when the installed MP1900A modules are connected to other devices or DUTs.**

<Power-on procedure>

1. **Make sure the MP1900A modules are not connected to other devices or DUTs.**
2. **Power on the MP1900A.**
3. **Connect the MP1900A modules to other devices and DUTs.**

<Power-off procedure>

1. **Make sure the MP1900A modules are not connected to other devices or DUTs.**
2. **Power off the MP1900A.**

CAUTION

When connecting an external device such as a Bias-T to the output connectors of MP1900A modules, if the output signal includes any DC voltage, variations in the output of the DC power supply or load may change the level of the output signal, risking damage to the internal circuits.

- **Do not connect or disconnect any external devices while DC voltage is impressed.**
- **Only switch DC power sources ON and OFF when all equipment connections have been completed.**

<Recommended procedure>

Measurement Preparation 1:

1. **Connect all equipment.**
2. **Set the DC power supply output to ON.**
3. **Set the MP1900A modules output to ON and complete measurement.**

Measurement Preparation 2

1. **Set the equipment output to OFF.**
2. **Set the DC power supply output to OFF.**
3. **Disconnect the MP1900A modules, or change the DUT connections.**

Since even unforeseen fluctuations in DC voltage and load (open or short circuits at the MP1900A modules output side and changes caused by using a high-frequency probe, etc.,) can damage the DUT and equipment, we recommend connecting a 50–ohm resistance in series with the DC terminal of the Bias-T to prevent risk of damage.

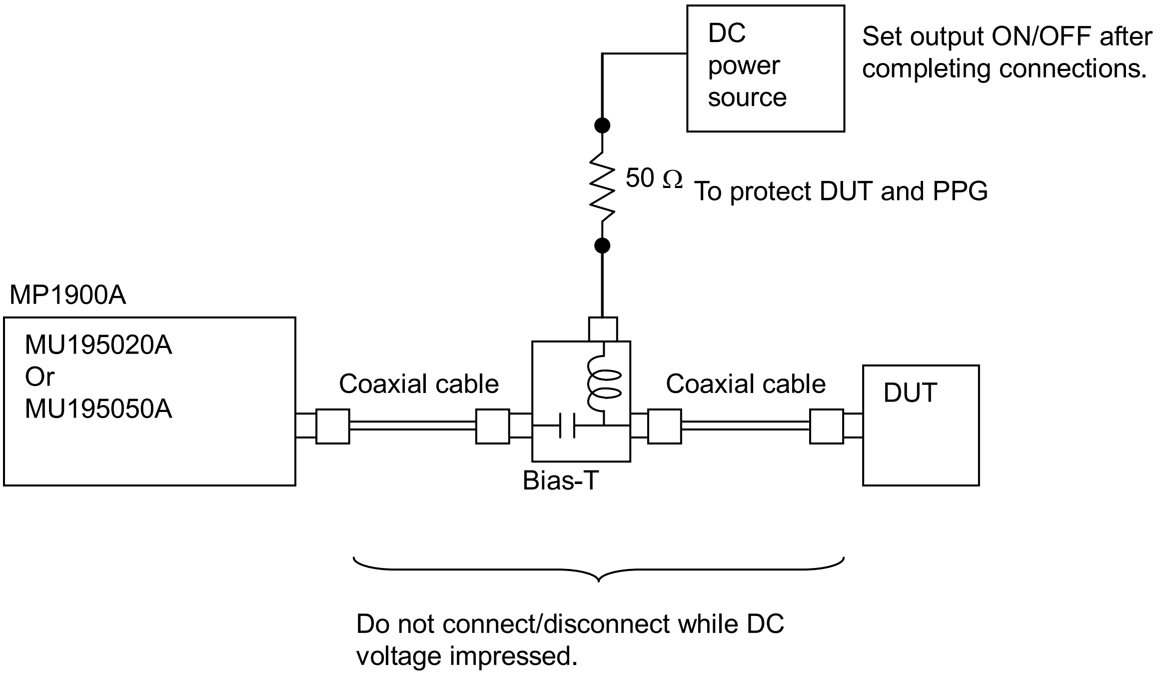


Figure 2.3-1 Bias-T Connection Example

Chapter 3 Panel Layout and Connectors

This chapter describes the panel and connectors of the MP1900A modules.

3.1 Panel Layout

3.1.1 MU195020A

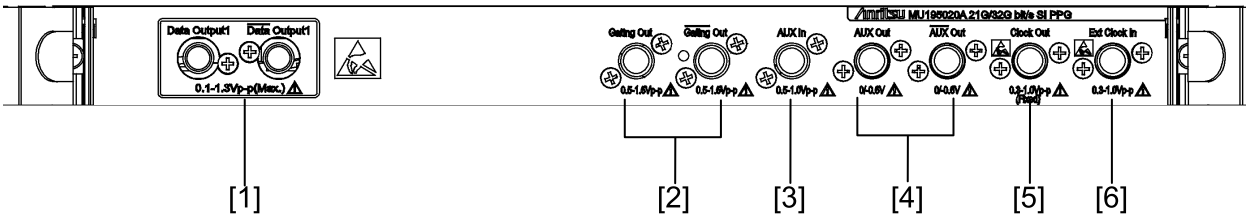


Figure 3.1.1-1 Panel layout (MU195020A-x10)

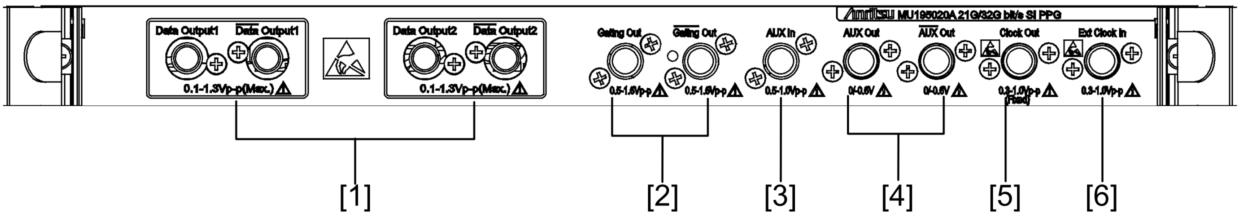


Figure 3.1.1-2 Panel layout (MU195020A-x20)

Table 3.1.1-1 Connectors on panel

No.	Name	Description
[1]	Data Output, $\overline{\text{Data}}$ Output	Outputs the differential data signals. Various interface signals can be output, depending on the installed option (s).
[2]	Gating Out, $\overline{\text{Gating}}$ Out	In case of Repeat: Outputs the timing signals. In case of Burst: Outputs the timing signals for Burst.
[3]	AUX In	Inputs auxiliary signals. Error Injection, and Burst can be selected.
[4]	AUX Out, $\overline{\text{AUX}}$ Out	Outputs auxiliary signals. 1/N clock, Pattern Sync, and Burst2 signals can be output according to the setting. Because of differential output, be sure to terminate the unused connector with the coaxial terminator (J1632A).
[5]	Clock Out	Outputs clock signals.
[6]	Ext Clock In	Inputs clock signals from these units: MU181000A 12.5GHz Synthesizer MU181000B 12.5GHz 4 Port Synthesizer MU181500B Jitter Modulation Source External Synthesizer*

*: We recommend using the MG3690C series as an external synthesizer.

For details about the MG3690C series, contact Anritsu or our sales representative.

3.1.2 MU195040A

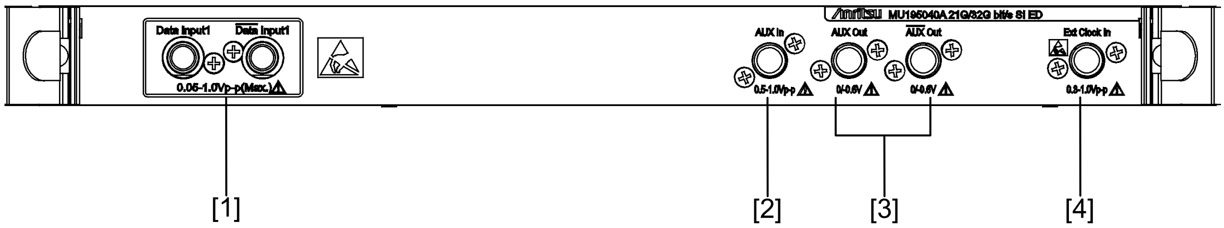


Figure 3.1.2-1 Panel layout (MU195040A-x10)

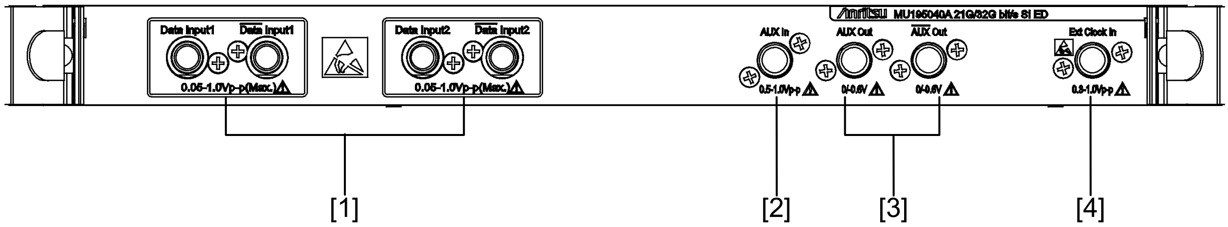


Figure 3.1.2-2 Panel layout (MU195040A-x20)

Table 3.1.2-1 Connectors on panel

No.	Name	Description
[1]	Data Input, $\overline{\text{Data}}$ Input	Input Data, $\overline{\text{Data}}$ data signals. Support both differential and single-ended input signals. When the MU195040A-x22 Clock Recovery is installed, the clock is recovered from the signal input to the Data Input1 connector.
[2]	AUX In	Inputs auxiliary signals. External Mask, Burst, or Capture External Trigger can be selected.
[3]	AUX Out, $\overline{\text{AUX}}$ Out	Outputs auxiliary signals. 1/N Clock, Pattern Sync, Error, and Sync Gain output signals can be selected. Because of differential output, be sure to connect the coaxial terminator (J1632A) to unused side connector.
[4]	Ext Clock In	Inputs clock signals.

3.1.3 MU195050A

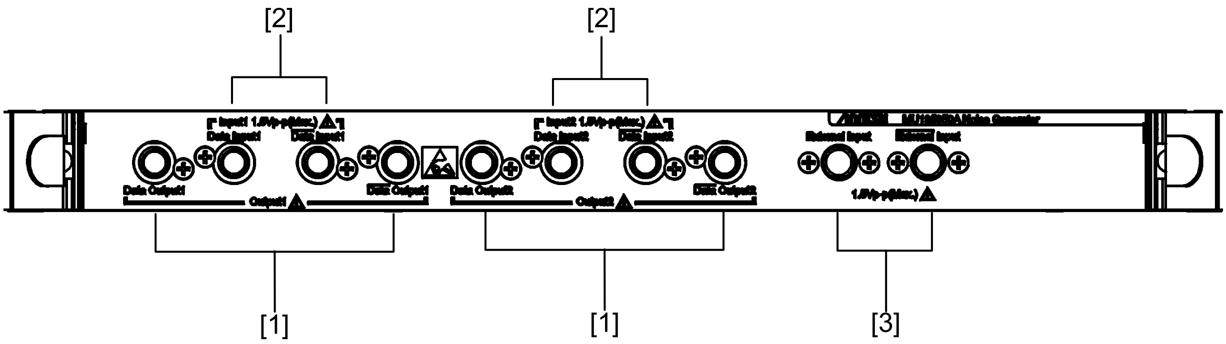


Figure 3.1.3-1 Panel layout (MU195050A)

Table 3.1.3-1 Connectors on panel

No.	Name	Description
[1]	Data Output, $\overline{\text{Data}}$ Output	Connectors to output differential Data and $\overline{\text{Data}}$ signals to which noise is added.
[2]	Data Input, $\overline{\text{Data}}$ Input	Connectors to input Data and $\overline{\text{Data}}$ signals to add noise. Support both differential and single-ended input signals.
[3]	External Input, $\overline{\text{External}}$ Input	Inputs auxiliary signals. They are used in connection with BSG4G USB Test Adapter or MU195020A Gating Output signal.

3.2 Inter-Module Connection

Avoid static electricity when handling the devices.

⚠ WARNING

- **When signals are input to this MP1900A modules, avoid excessive voltage beyond the rating. Otherwise, the circuit may be damaged.**
- **As a countermeasure against static electricity, ground other devices to be connected (including experimental circuits) with ground wires before connecting the I/O connector.**
- **The outer conductor and core of the coaxial cable may become charged as a capacitor. Use any metal to discharge the outer conductor and core before use.**
- **The power supply voltage rating for the MP1900A is shown on the rear panel. Be sure to operate the MP1900A within the rated voltage range. The MP1900A may be damaged if a voltage out of the rating range is applied.**
- **To protect the MP1900A modules from electrostatic discharge failure, a conductive sheet should be placed onto the workbench, and the operator should wear an electrostatic discharge wrist strap. Always ground the wrist strap to the workbench antistatic mat or the frame ground of the MP1900A.**
- **When removing a cable from a connector on the front panel of the MP1900A modules, be careful not to add excessive stress to the connector.**
  Addition of excessive stress to a connector may result in characteristic degradation or a failure. Use a torque wrench (recommended torque: 0.9 N-M) when attaching or removing a cable.

⚠ CAUTION

Note that the maximum output level of the Data Output connector of MU195020A-x10/x20 is “1.30 Vp-p” (1.50 Vp-p when Option x11/x21 is installed). Also, the data output level of MU195050A is decided by the data input level, and it is at maximum 1.50 Vp-p. The maximum data input level of MU195040A is 1.00 V.

When connecting the Data Output connector of MU195020A/MU195050A directly to the Data Input connector of MU195040A to verify operation, make sure that the data output level of MU195020A/MU195050A is 1 V or under.

Avoid inputting the signal exceeding the maximum input level to the Data Input connector of MU195040A. Failure to do so can cause damage.

3.2.1 Measuring Errors

This section describes a connection example of MU195020A, MU181000A 12.5GHz synthesizer (hereafter MU181000A), and MU195040A that are installed to an MP1900A.

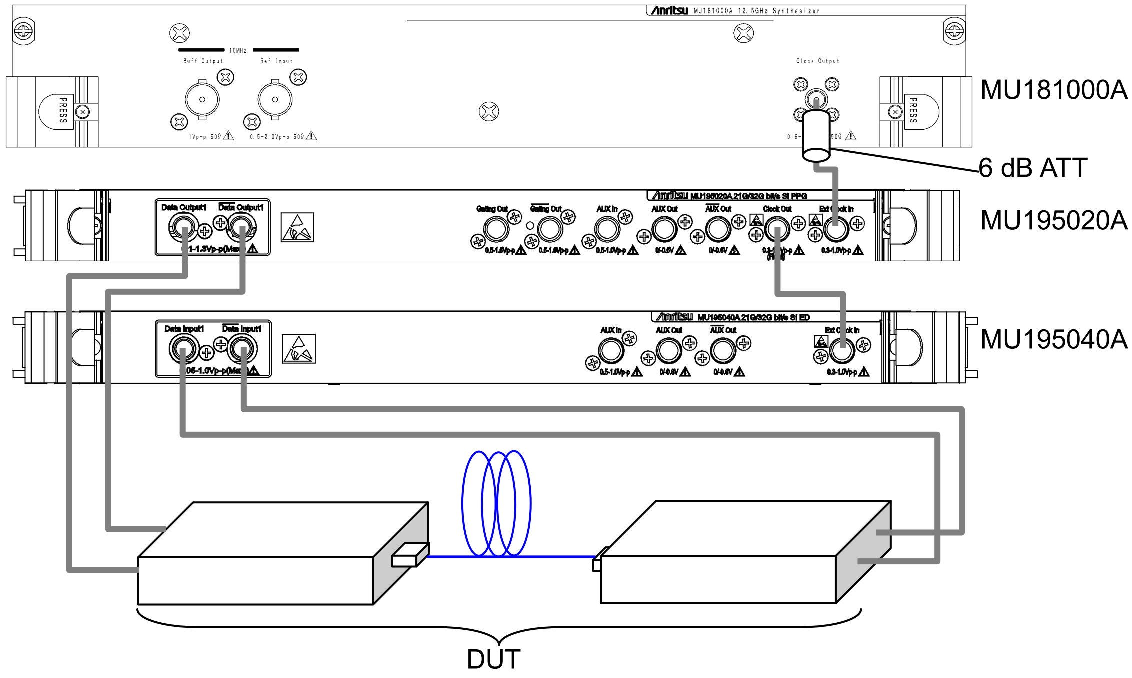


Figure 3.2.1-1 Inter-module connection example

1. For the case of the MU181000A, attach the 6 dB fixed attenuator (ATT) to the Clock Output connector.
   The following module and options do not require the 6 dB fixed attenuator.
   MU181000A-x01, MU181000B, MU181000B-x01
2. Connect the Clock Output connector of the MU181000A and the Ext. Clock Input connector of the MU195020A, using a coaxial cable.
3. Connect the Clock Output connector of the MU195020A and the Ext. Clock Input connector of the MU195040A, using a coaxial cable.
4. Connect the Data Output connector of the MU195020A and the Data Input connector of the device under test (DUT) using a coaxial cable. Also connect the $\overline{\text{Data}}$ Output connector of the MU195020A and the $\overline{\text{Data}}$ Input connector of the DUT, using a coaxial cable.
5. Connect the Data Output connector of the DUT and the Data Input connector of the MU195040A, using a coaxial cable. Also connect the $\overline{\text{Data}}$ Output connector of the DUT and the $\overline{\text{Data}}$ Input connector of the MU195040A, using a coaxial cable.

6. Start MX190000A and select **Initialize** from the **Menu** to initialize the entire system.
   Note that all the settings are initialized to the factory default settings by initialization. If necessary, select **Save** from the **Menu** to save the settings before initialization.

3.2.2 Measuring Errors with Noise Added

This section describes a connection example of MU195020A, MU181000A, MU195050A, and MU195040A that are installed to an MP1900A.

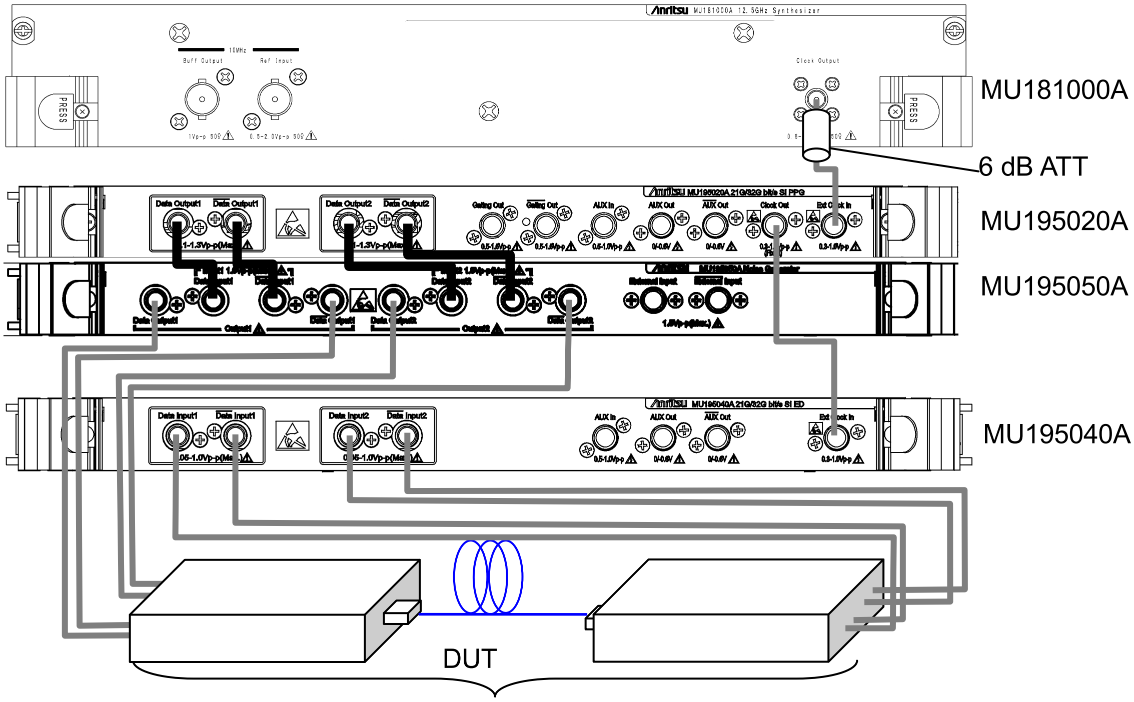


Figure 3.2.2-1 Inter-module connection example

1. For the case of the MU181000A, attach the 6 dB fixed attenuator (ATT) to the Clock Output connector.
   The following module and options do not require the 6 dB fixed attenuator.

   MU181000A-x01, MU181000B, MU181000B-x01
2. Connect the Clock Output connector of the MU181000A and the Ext. Clock Input connector of the MU195020A, using a coaxial cable.
3. Connect the Data Output connector of the MU195020A and the Data Input connector of the MU195050A using a coaxial cable coming with MU195050A. Also connect the $\overline{\text{Data}}$ Output connector of the MU195020A and the $\overline{\text{Data}}$ Input connector of the MU195050A, using a coaxial cable (J1746A, J1747A) coming with MU195050A.
4. Connect the Data Output connector of the MU195050A and the Data Input connector of the device under test (DUT) using a coaxial cable. Also connect the $\overline{\text{Data}}$ Output connector of the MU195050A and the $\overline{\text{Data}}$ Input connector of the DUT, using a coaxial cable.
5. Connect the Data Output connector of the DUT and the Data Input connector of the MU195040A, using a coaxial cable. Also connect the

$\overline{\text{Data}}$ Output connector of the DUT and the $\overline{\text{Data}}$ Input connector of the MU195040A, using a coaxial cable.

6. Start MX190000A and select **Initialize** from the **Menu** to initialize the entire system.
   Note that all the settings are initialized to the factory default settings by initialization. If necessary, select **Save** from the **Menu** to save the settings before initialization.

3.2.3 Adding Jitter to Output Signal

MU181000A or MU181000B (hereafter MU181000A/B) and MU181500B jitter modulation source (hereafter MU181500B) are used to add jitter to signal that is outputted from PPG.

Figure 3.2.3-1 shows a connection example of MU181000A, MU181500B, MU195020A, and MU195040A.

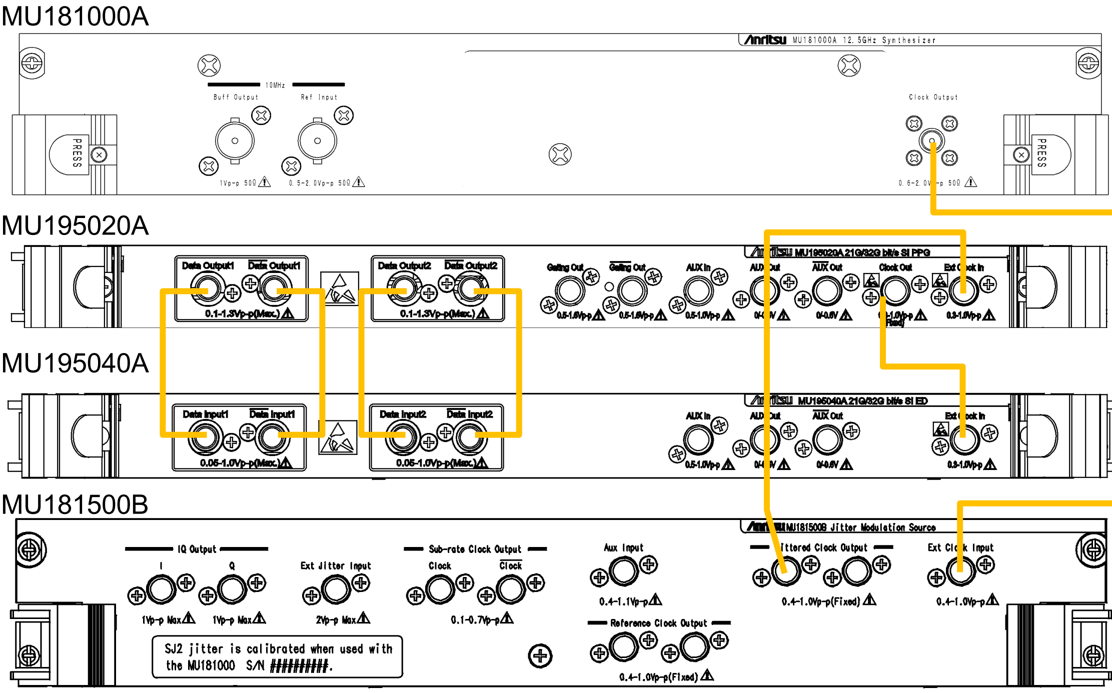


Figure 3.2.3-1 Connection example when adding jitter to output signal

1. Use a coaxial connector to connect the Clock Output connector of the MU181000A and the Ext Clock Input connector of the MU181500B.
2. Use a coaxial connector to connect the Jittered Clock Output connector of the MU181500B and the Ext Clock Input connector of the MU195020A.
3. Use a coaxial connector to connect the Clock Output connector of the MU195020A and the Ext Clock Input connector of the MU195040A.
4. Use coaxial cables to connect Data Output and $\overline{\text{Data}}$ Output connectors of the MU195020A with Data Input and $\overline{\text{Data}}$ Input connectors of the MU195040A (2 connections).
5. Start MX190000A and select **Initialize** from the **Menu** to initialize the entire system.
   Note that all the settings are initialized to the factory default settings by initialization. If necessary, select **Save** from the **Menu** to save the settings before initialization.

3.2.4 Synchronizing Multiple Channels of PPG

To synchronize multiple MU195020As installed to MP1900A, use MU181000A/B or external clock.

Below is a connection example when synchronizing two units of MU195020A using MU181000B.

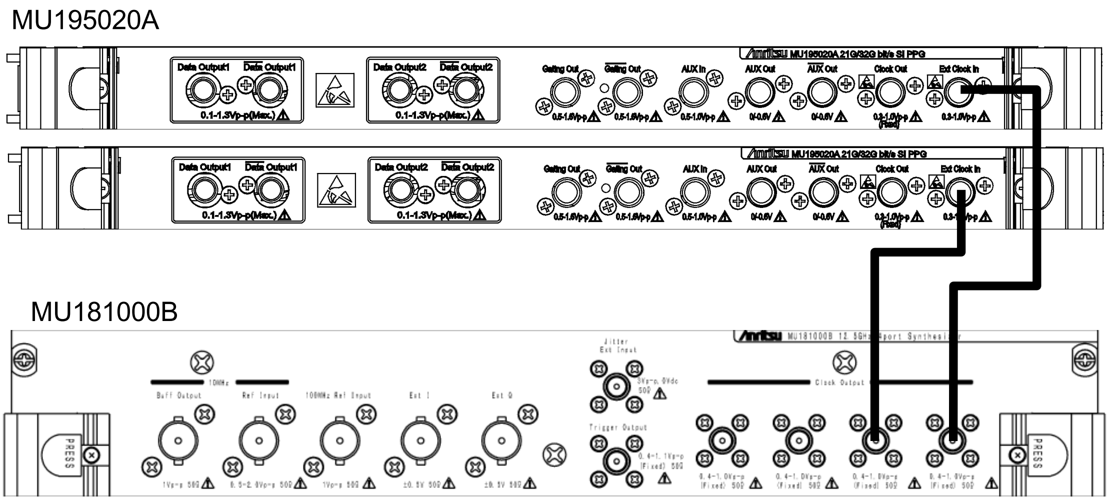


Figure 3.2.4-1 Connection Example for PPG Multi-Channel Synchronization

1. Connect the Clock Output connector of MU181000B and the Ext Clock Input connector of MU195020A with a coaxial cable.
2. Start MX190000A and select **Menu** → **Combination Setting** on the menu bar. Set **Sync ON/OFF** of **Inter module Combination** to **Channel Synchronization**.

Notes:

- Insert units of MU195020A into slots in order from Slot 1.
- Make sure that the cable phase difference is 10 ps or under.

Chapter 4 Configuration of Setup Dialog Box

This chapter describes the configuration of the MP1900A modules setup dialog box.

4.1 Configuration of Entire Setup Dialog Box

Following figure shows the configuration of the setup dialog box when MP1900A modules are mounted in an MP1900A.

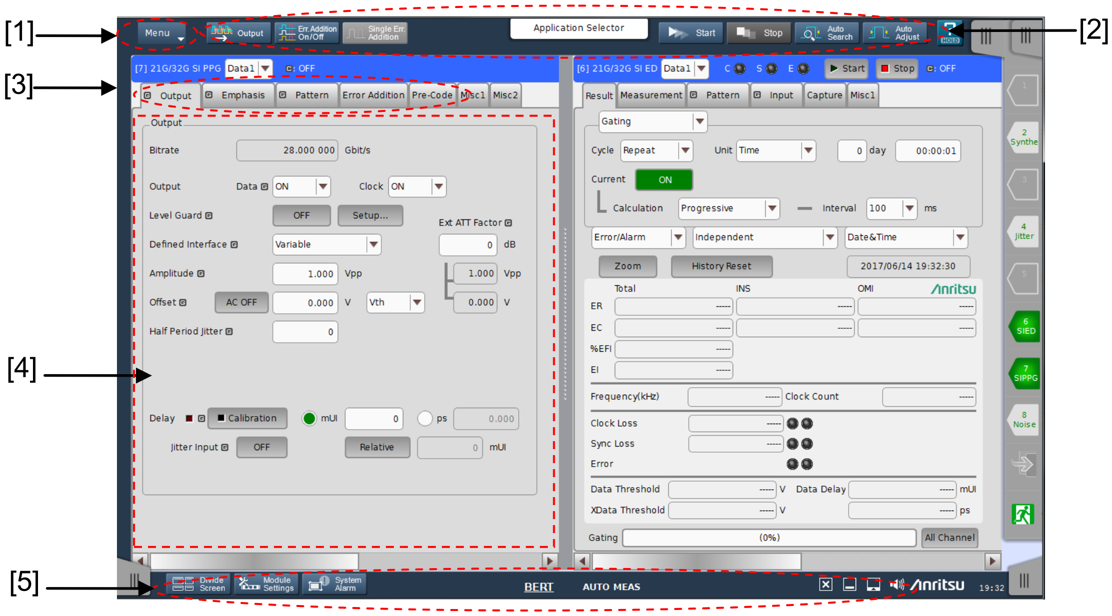


Figure 4.1-1 Configuration of entire setup dialog box for MP1900A modules

The screens consist of four blocks ([1] to [4] in Figure 4.1-1). Table 4.1-1 describes the function of each block.

Table 4.1-1 Functions of blocks

No.	Block	Function
[1]	Menu ber	Selects the setting functions related to the entire device.
[2]	Module functions	Shortcut buttons for the function items common to the displayed modules.
[3]	Function setting selection tabs	Tabs to switch the module setup window according to the function items. Refer to Chapter 5 “Operation Method” for details.
[4]	Operation area	Configures settings specific to each module. Refer to Chapter 5 “Operation Method” for details.
[5]	System control	Controls the basic functions of the system. Refer to Chapter 5 “Operation Method” for details.

4.2 Equipment Composition

Tabs to operate the MP1900A modules have the following functions.
Refer to Chapter 5 “Operation Method” for details on each tab.

4.2.1 MU195020A

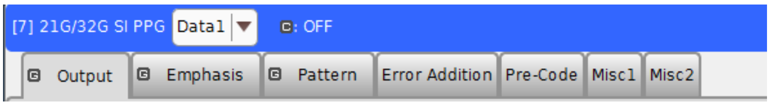
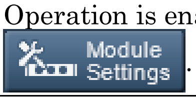


Figure 4.2.1-1 MU195020A function setting selection tabs

Table 4.2.1-1 List of MU195020A function setting selection tabs

Tab Name	Function
Output	Selection and setting of Data/XData and Clock outputs Various output interface settings can be configured in this tab window.
Emphasis	This is displayed when MU195020A-x11/x21 is installed. It sets Emphasis of Data and XData. ISI can be set when MU195020A-x40/x41 is installed.
Pattern	Selection and setting of test pattern A test pattern can be selected and edited in this tab window.
Error Addition	Selection and setting of error addition The error addition function can be set in this tab window.
Pre-Code	This is displayed when MU195020A-x20 is installed. Operation is enabled when Combination is set by  .
Misc1	Other settings can be configured. Pattern generation method setting, auxiliary input/output selection, and other settings can be configured in this tab window.
Misc2	Setting of frequency ratio of Clock Input and Data Output.

4.2.2 MU195040A

Figure 4.2.2-1 MU195040A function setting selection tabs

Table 4.2.2-1 List of MU195040A function setting selection tabs

Tab Name	Function
Result	Measurement results are displayed.
Measurement	Various measurement conditions can be set.
Pattern	Test pattern types can be set. A test pattern can be selected and edited in this tab window.
Input	Test signal input interface can be set.
Capture	Test patterns can be captured into the internal memory.
Misc1	Other settings can be configured. Pattern generation method setting, auxiliary input/output selection, and other settings can be configured in this tab window.

4.2.3 MU195050A

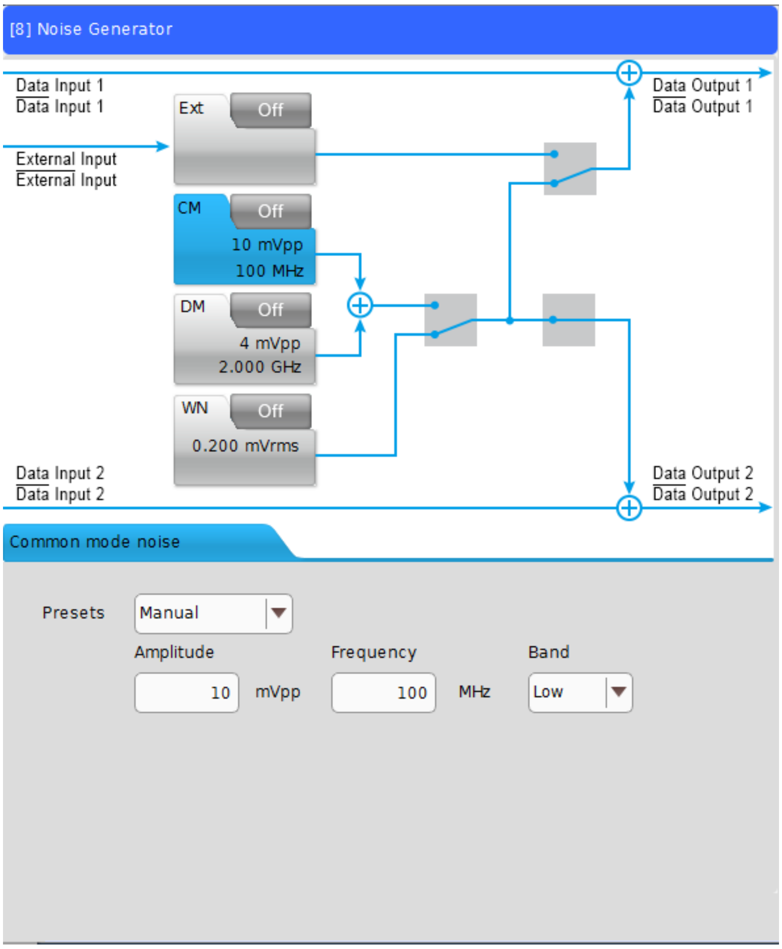


Figure 4.2.3-1 MU195050A function setting

MU195050A has one window without function tabs.

Chapter 5 Operation Method

This chapter explains the functions on the operation screen of MX190000A.
For description of MU195020A, refer to 5.1 through 5.10.
For description of MU195040A, refer to 5.11 through 5.19.
For description of MU195050A, refer to 5.20.

5

Operation Method

5.1 Setting Output Interface

To set the output interface, touch the **Output** tab of the MU195020A operation window.

On the **Output** tab, the settings for the Data and Clock can be configured. The Data signal is output from the Data connector of the MU195020A, and the XData signal is output from the $\overline{\text{Data}}$ connector. Also, the Clock signal is output from the Clock connector.

5.1.1 Setting the data

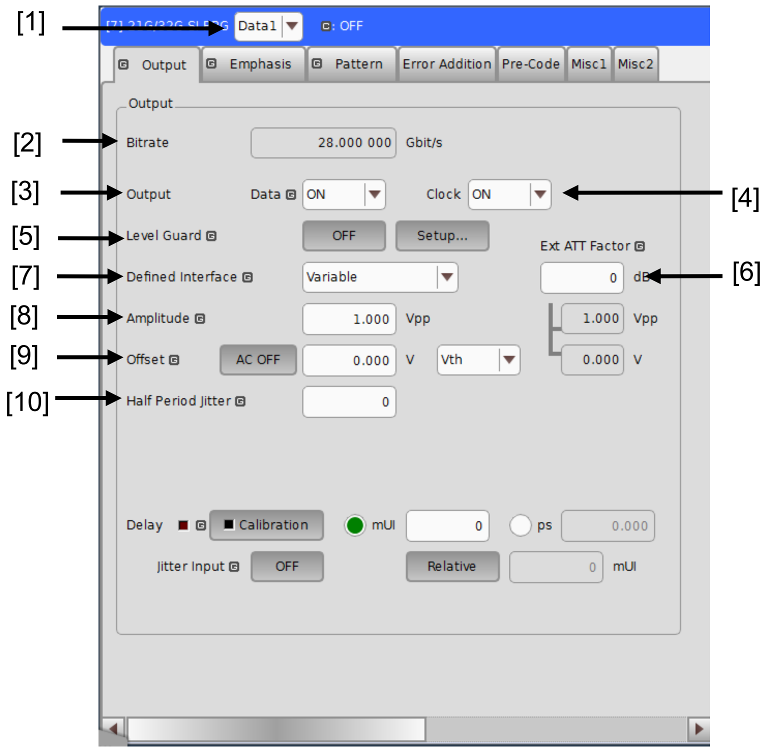


Figure 5.1.1-1 Output tab

Delay appears when the MU195020A-x30 or x31 is added.

[1] Selects a channel for which you set up data.

[2] When clock supply source is **External**, the data bit rate is displayed. When the clock source is MU181000A/B, the data bit rate can be set. For details, refer to 5.1.4 “Setting bit rate” and 5.7.1 “Setting Clock”.

[3] Sets data output.
This is data output setting concerning the selected MU195020A. To turn the output signal to On, turn On the output of the entire equipment (

) on the menu bar in addition to this setting.

Notes:

- The DUT may be damaged if the output setting is configured incorrectly. To prevent damage to the DUT, confirming the interface condition with the DUT, or configuring the level guard setting before making the output setting is recommended.

- When PCML, LVPECL, or NECL is selected for Defined Interface, the voltage corresponding to the DUT's termination voltage is applied to the output side of the MU195020A. In this event, the DUT may be damaged if the interface conditions do not match. Be sure to confirm the interface conditions.

- Waveforms may be distorted (what is known as a ringing phenomenon) when a commercially-available ECL terminator is used to observe output waveforms. This is, however, caused by the characteristics of the ECL terminator; the waveform output from the mainframe is not distorted.

- Be sure to confirm that a fixed attenuator is connected between the MU195020A and the DUT before setting the external ATT factor. If the external ATT factor is set when no fixed attenuator is connected or when the fixed attenuator has an attenuation value less than that set in the External ATT Factor area, the DUT may be damaged.

[4] Set the clock output.

Note:

Depending on the operating bit rate, some clock signals of several tens of mV may be output even if the clock output is set to Off.

[5] Configure the level guard settings.
Touch **Setup** to open the setup dialog box, and set the maximum amplitude (Amplitude), maximum offset (Offset Max (Voh); maximum value of the offset high level), and minimum offset (Offset Min (Vol); minimum value of the offset low level) for level guard, so that an excessively high voltage is not applied to the DUT.

When the external ATT factor is set (see [6] below), the level guard settings limit the output level of Amplitude, Offset Max (Voh), and Offset Min (Vol) after passing through the fixed attenuator connected between the MU195020A and the DUT. Thus, if use the equipment without a fixed attenuator, the signals above the set values are output.

[6] Set the external ATT Factor.
When a fixed attenuator is connected to the Data/XData output connector of the MU195020A, the attenuation of the attenuator is added to the value for the DUT and displayed. A value from 0 to 40 dB can be set in 1-dB steps. When Defined Interface is not set to other than **Variable**, the setting is reset to 0 and becomes invalid. Values displayed in the External ATT Factor-Amplitude and Offset display areas indicates the amplitude and offset value after passing through the attenuator, respectively.

[7] Set the Defined interface.
Note that it may not be possible to select some items, depending on the level guard setting.

Table 5.1.1-1 Amplitude setting values

Item	Amplitude	Offset Vth
Variable	–	–
PCML	0.5 V	+3.05 V
NCML	0.5 V	–0.25 V
SCFL	0.9 V	–0.45 V
NECL	0.8 V	–1.3 V
LVPECL	0.8 V	+2.0 V

[8] Set the common amplitude for Data and XData.
The setting range varies depending on the level guard setting, and offset setting.

[9] Set the common offset for Data and XData.
Range is $-2.000-\frac{\text{Amp.}}{2}$ to $+3.300-\frac{\text{Amp.}}{2}$ V, 0.001 V step.
Touching to change **AC OFF** to **AC ON** enables AC-coupled output.

5

Operation Method

[10] Set the Half Period Jitter for the data output signal. The Cross Point time axis can be adjusted as shown in Figure 5.1.1-2 using this setting while observing the Eye pattern. Adjacent Eye patterns become equal at default 0.

Table 5.1.1-2 Half Period Jitter setting range

Setting values	Resolution
–20 to 20	1

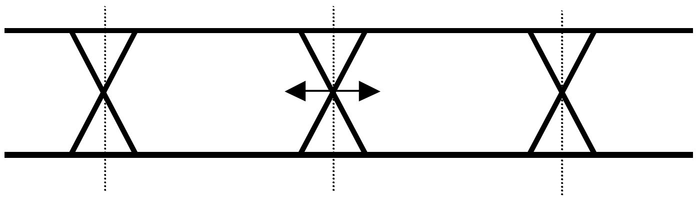


Figure 5.1.1-2 Setting Half Period Jitter

Note:

The data amplitude of MU195020A output with the following patterns may be attenuated by around 50% or the offset voltage (Vth) may be fluctuated.

- The pattern in the period of approximately 5 μs which follows continuous “0” or “1” with 5 μs or more.

  This kind of pattern may be generated by inserting continuous “0” or “1” or by a burst pattern.

- The pattern other than its mark ratio of 1/2.

5.1.2 Setting the delay

The Data output phase can vary relative to the Clock output when any of the following is installed:

- MU195020A-x30
- MU195020A-x31

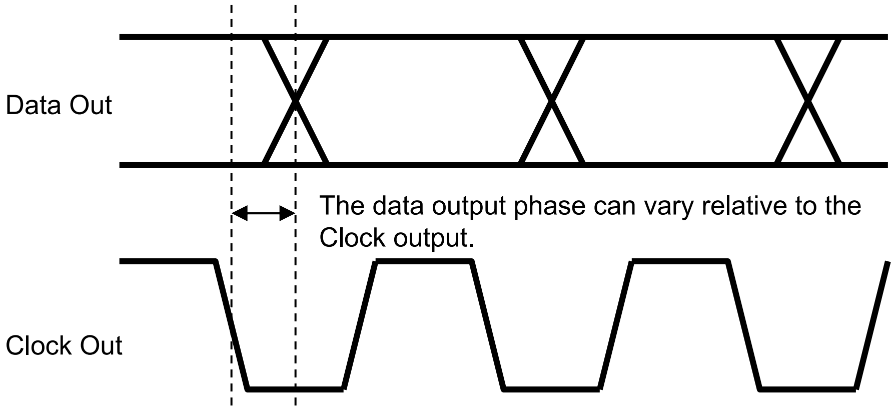


Figure 5.1.2-1 Delay setting

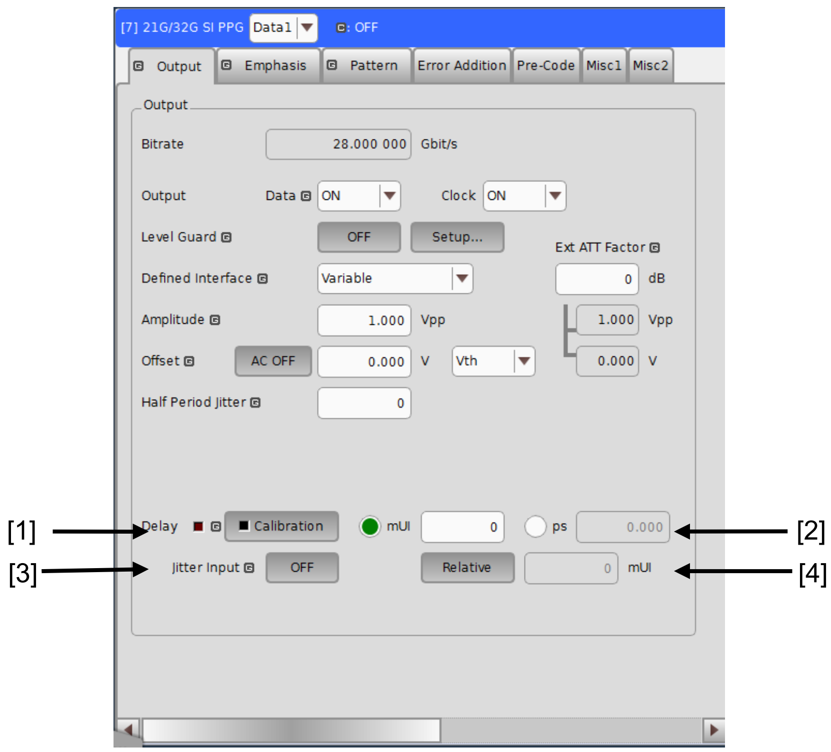


Figure 5.1.2-2 Output Tab When Setting the Delay

[1] Touch **Calibration** to perform calibration of a phase variable function.
When the power is supplied, the frequency is changed, or the ambient temperature fluctuates, the calibration prompting alarm LED lights up. In such a case, touch this button to perform calibration. Calibration will finish within 1 second.

[2] Set the delay in mUI or ps units.

<In the case of mUI units>

The delay can be set from –1000 to 1000 mUI, in 2-mUI steps.
When the 2ch Combination or Channel Synchronization Option is installed, setting is supported from –64,000 to 64,000 mUI in 2-mUI steps.

<In the case of ps units>

The delay can be set in steps of ps units, equivalent to 2 mUI. The setting range is the range converting –1000 to 1000 mUI in ps units. During 2ch Combination or Channel Synchronization, the setting range is equivalent to the range when the unit is mUI (–64,000 to 64,000 mUI), converted into ps units.

Table 5.1.2-1 Delay setting range

Bit rate	Setting range	
	Normal	2ch Combination Channel Synchronization
32.1 Gbit/s	–31.14 to 31.14 ps	–1 993.74 to 1 993.74 ps
25 Gbit/s	–40 to 40 ps	–2 560 to 2 560 ps
2.4 Gbit/s	–416 to 416 ps	–26 665.6 to 26 665.6 ps

[3] Set the Jitter Input.

When inputting jitter-modulated clocks, set Jitter Input of Delay to **ON**.

[4] Touch **Relative** to use the current set phase value as the reference of relative 0 for delay setting.

Notes:

- When the frequency or the temperature condition is changed, the LED on the **Calibration** lights, prompting performance of calibration. If calibration is not performed at this time, the error in the phase setting may be greater than at a normal phase setting.

- Values displayed in ps units vary as the frequency changes, because the MU195020A sets phases in mUI units as an internal standard.

Delay setting in the case of Combination or CH Synchronization

In the case of Combination or Channel Synchronization when multiple MU195020A modules are mounted, the delay between two or more channels can be changed relatively, as shown in Figure 5.1.2-3.

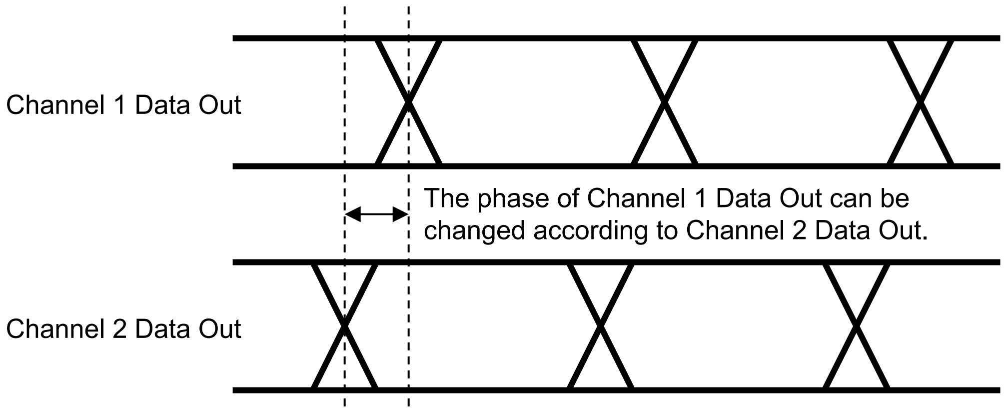


Figure 5.1.2-3 Delay setting in the case of Combination

5.1.3 When setting jitter-modulated signals

- When inputting jitter-modulated clocks, use MU181000A/B and MU181500B. For inter-module connection, refer to 3.2.2 “Adding Jitter to Output Signal”.
- Set Jitter Input of Delay to **ON**.
- Set the jitter modulation for input signals to non-modulation when executing calibration of Delay.
- When configuring Combination Setting, set the jitter modulation to non- modulation before setting Combination or Channel Synchronization.
- When changing the input frequency while Combination or Channel Synchronization is set, be sure to set Jitter Input of Delay for the MU195020A to **ON** and then set the jitter modulation to **ON**, in this order, after changing the frequency for measurement.

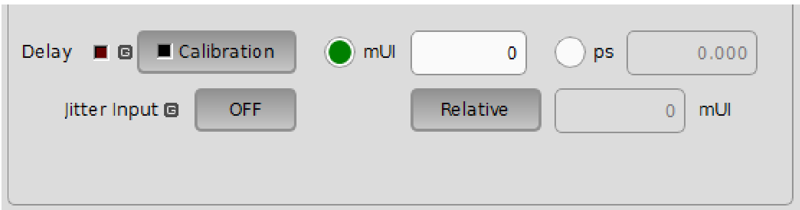


Figure 5.1.3-1 Delay Setting Items in the Output Tab (Close up)

Notes:

- When jitter-modulated clock is input while Jitter Input of Delay is set to **OFF**, the phase may become unstable.

- The Delay lamp may light up when a jitter-modulated clock signal is input. In addition, phase setting error may increase.

5.1.4 Setting bit rate

When the clock source is MU181000A/B or MU181500B, the bit rate of data output can be set. For how to set the clock source, refer to 5.7.1 “Setting Clock”.

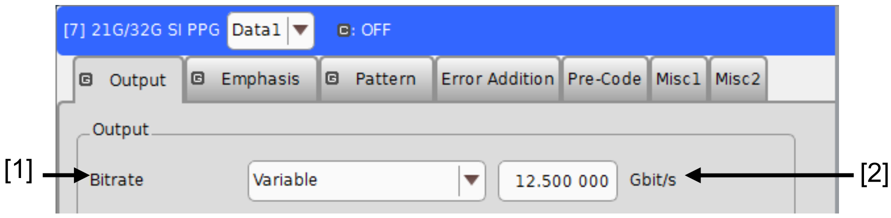


Figure 5.1.4-1 [Output] Tab Bit Rate Setting Area

[1] When the clock source is MU181000A, MU181000B or MU181500B, select a bit rate from the preset standard list (Table 5.1.4-1 Preset Standard of Bit Rate) or set to **Variable** to specify an arbitrary value.

[2] A corresponding bit rate is displayed when a preset standard is selected. When set to **Variable**, an arbitrary bit rate can be specified.

Note:

A bit rate can be set only when the MU181500B clock source is MU181000A/B. When using an external clock source for MU181500B, the PPG bit rate cannot be set.

Table 5.1.4-1 Preset Standard of Bit Rate

Preset Standard	Bit rate [Gbit/s]
OC-48/STM-16	2.488320
PCIe 1	2.500000
InfiniBand SDR	2.500000
OTU1	2.666060
DisplayPort HBR	2.700000
SATA 3Gb/s	3.000000
XAUI	3.125000
4G FC	4.250000
USB3.0	5.000000
InfiniBand DDR	5.000000
PCIe 2	5.000000
DisplayPort HBR2	5.400000
SATA 6Gb/s	6.000000
HSBI	6.250000
PCIe 3	8.000000
DisplayPort HBR3	8.100000
8G FC	8.500000
OC-192/STM-64	9.953280
InfiniBand QDR	10.000000

Table 5.1.4-1 Preset Standard of Bit Rate (Cont'd)

Preset Standard	Bit rate [Gbit/s]
USB3.1 Gen2	10.000000
USB4 Gen2	10.000000
DisplayPort UHBR 10	10.000000
Thunderbolt1	10.312500
10GbE	10.312500
10G FC	10.518750
G975 FEC	10.664228*2
OTU2	10.709225*2
10GbE over FEC	11.095700
10GFC over FEC	11.316800
SAS3	12.000000
DisplayPort UHBR 13.5	13.500000
16G FC	14.025000
InfiniBand FDR	14.062500
PCIe 4	16.000000
USB4 Gen3	20.000000
DisplayPort UHBR 20	20.000000
Thunderbolt2	20.625000
SAS4	22.500000*1
SAS	24.000000*1
InfiniBand EDR	25.781250*1, *2
100GbE(25.78x4)	25.781250*1, *2
100G OTU4	27.952496*1, *2
32G FC	28.050000*1
PCIe 5	32.000000*1
100G ULH	32.100000*1

*1: Only when the MU195020A-x01 is installed.

*2: The bit rate resolution is automatically set to 0.000002 Gbit/s or 0.000004 Gbit/s interlinking with the output clock rate of the 32G PPG Misc2 and the current bit rate. Thus, the bit rate may not be set to the exact standard value.

Table 5.1.4-2 Bit Rate Setting Range for [Variable]

Preset Standard	Bit rate [Gbit/s]
Variable	2.400000 to 21.000000 Gbit/s (32.100 000 Gbit/s with MU195020A-x01 installed) Can be set in increments of 0.000002 Gbit/s.*

*: When it cannot be set by the Output Clock Rate set for the interlinked 32G PPG Misc2 and the current bit rate, the bit rate resolution is set to 0.000004 Gbit/s.

5.2 Setting Emphasis and ISI

When MU195020A-x11 or MU195020A-x21 is installed, Emphasis can be added to the output data. To set Emphasis, touch the **Emphasis** tab on the MU195020A operation screen and select and set up Preset. ISI can be added to the output data when the MX190000A version is 2.0.0 or later and the MU195020A-x40 or MU195020A-x41 is installed.
ISI can be configured on **Emphasis** tab. It's same as Emphasis configuration.

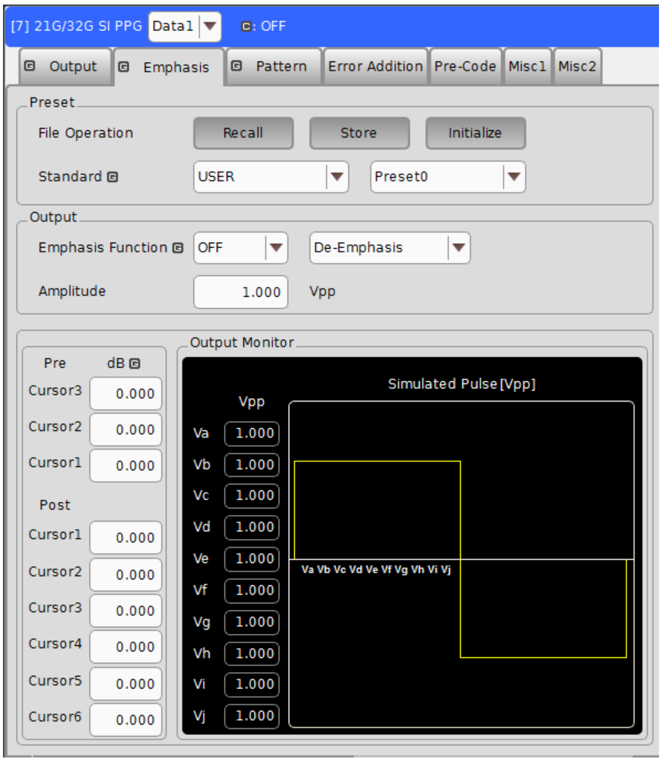


Figure 5.2-1 Emphasis Tab (MX190000A earlier than version 2.0.0)

5

Operation Method

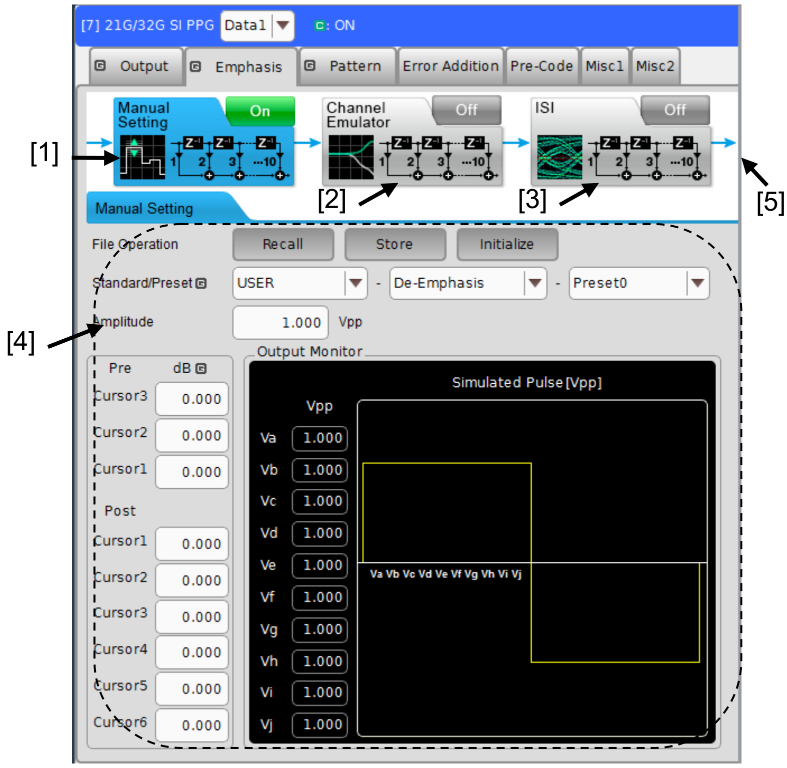


Figure 5.2-2 Emphasis tab When Manual Setting is selected (MX190000A version 2.0.0 or later)

[1] Touching this icon configures the manual setting of Emphasis.

[2] Touching this icon emulates the transmission channel.

[3] Touching this icon configures ISI.

[4] Advanced setting is configurable by selecting an item from [1] to [3].

[5] The Emphasis and the Emulated Responses set on the tabs with ON of [1] to [3] are combined and output.

5.2.1 Setting Emphasis Preset

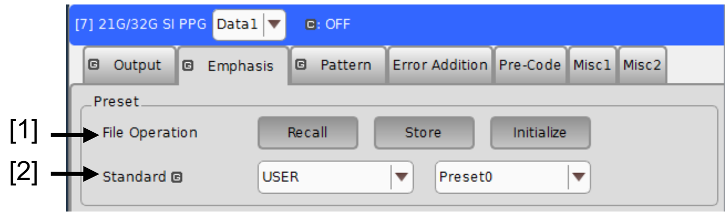


Figure 5.2.1-1 Preset Setting on Emphasis Tab

[1] **File Operation** to store, recall, and initialize preset setting.

Table 5.2.1-1 File Operation Buttons

Button	Function
Recall	Recalls the saved setting and set Preset.
Store	Stores Preset setting.
Initialize	Restores defaults.

[2] **Standard** can be selected from the preset standard list (table below) or set to an arbitrary preset value. Usable preset types are limited by standard.

Table 5.2.1-2 Emphasis Preset Standard

Preset Standard	Preset
PCIe 3	Preset0 to 10
PCIe 4	Preset0 to 10
PCIe 5	Preset0 to 10
USB3.0	Preset0
USB3.1 Gen2	Preset0 to 1
TBT3	Preset0 to 15
USER	Preset0 to 15

5.2.2 Setting Emphasis Function

Figure 5.2.2-1 Function Setting on Emphasis Tab

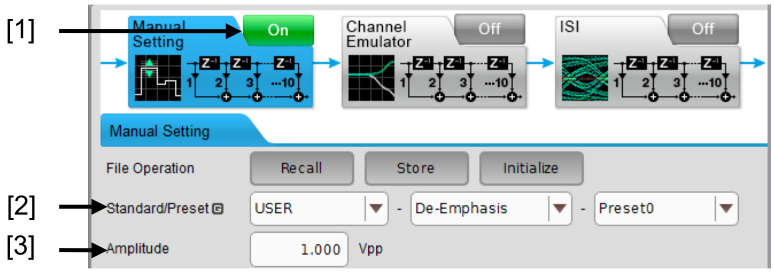


Figure 5.2.2-2 Emphasis Tab Function Selector (MX190000A version 2.0.0 or later)

[1] Sets Emphasis ON/OFF.

OFF: Although the emphasis waveform can be edited, the signal output from the front panel has no emphasis applied

ON: The signal output from the front panel has emphasis applied.

When using version 2.0.0 or later, set this by Manual Setting ON/OFF.

[2] Selects the type of Emphasis Function.
There are three selections: Coefficient, Pre-Emphasis, and De-Emphasis.
However, available functions are limited by preset standard.

Table 5.2.2-1 Emphasis Function According to Standard

Preset Standard	Emphasis Function
PCIe 3	De-Emphasis
PCIe 4	De-Emphasis
PCIe 5	De-Emphasis
USB3.0	De-Emphasis
USB3.1 Gen2	De-Emphasis
TBT3	Coefficient
USER	Coefficient, Pre-Emphasis, De-Emphasis

[3] Specifies Amplitude.
The setting is linked with the amplitude setting on the Output tab (see Figure 5.1.1-1 Output tab). Either tab allows you to set amplitude.

5.2.3 Setting Cursor Voltage

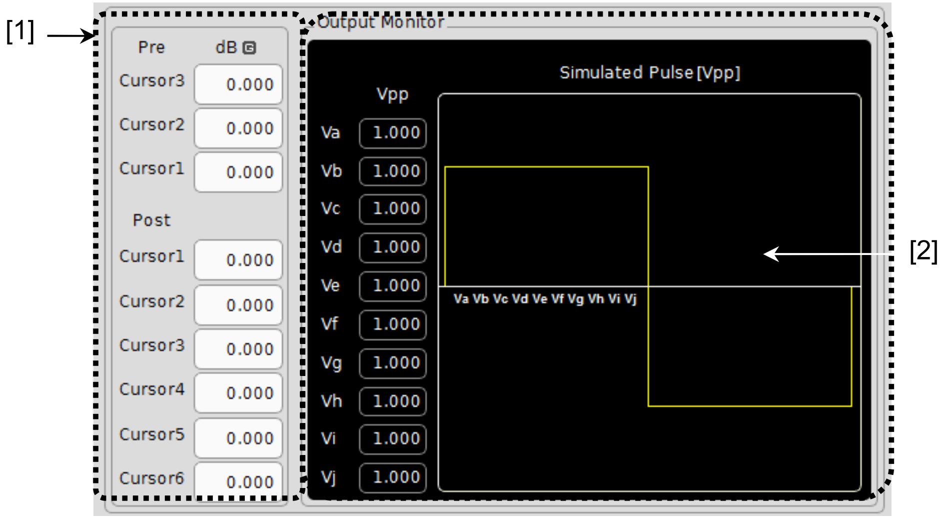


Figure 5.2.3-1 Cursor Setting on Emphasis Tab

[1] Sets the cursors.
3 Pre cursors and 6 Post cursors are available for Pre-Emphasis or De-Emphasis.
C3 to C6 cursors are available for Coefficient.

[2] Displays voltage of each cursor.
If **Channel Emulator** tab and **ISI** tab are ON, the Emulated Responses on each tab are combined and displayed on the monitor.

Note:

The setting range of cursor coefficients is limited so that the cursor voltage stays in the range of 0.1 to 1.5 V by the following settings.

- Amplitude
- Other cursor coefficients.

5 Operation Method

5.2.4 Channel Emulator Setting

MU195020A can load the S parameter file of the DUT and calculate optimum Emphasis setting for the DUT from the inverse characteristics of the loaded S parameter. Moreover, it can emulate the characteristics of transmission channel from its S parameter characteristics. The S parameters (s2p, s4p files) saved on the next models can be loaded.

- MICROWAVE NETWORK ANALYZER MS4640 Series
- BERTWave MP2100A/B Series

Notes:

- Channel Emulator is enabled only when MU195020A-x40 or MU195020A-x41 is installed.
- The FIR filter by 10Tap Emphasis cannot realize sharp attenuation and amplitude characteristics. Thus, this function cannot simulate the Normal and Inverse characteristics of S parameter that have steep filter characteristics.

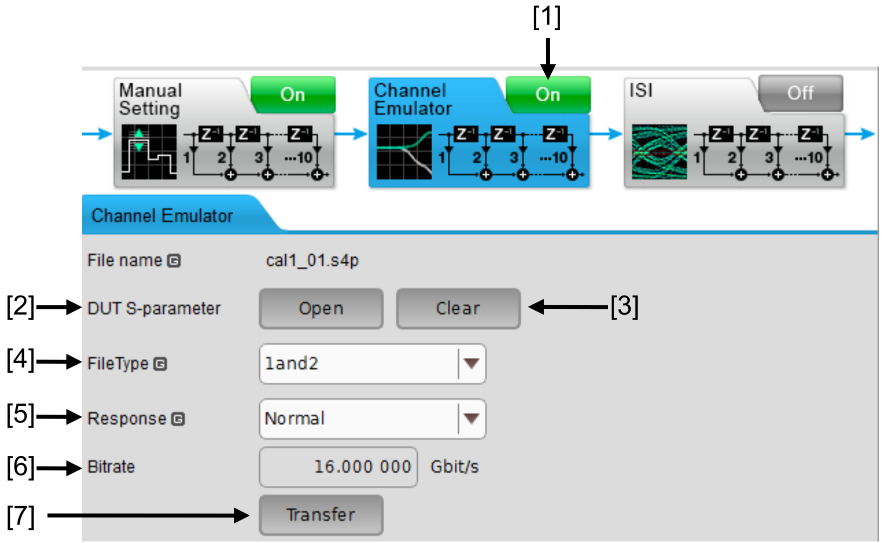


Figure 5.2.4-1 Emphasis tab Channel Emulator Configuration

[1] Set Channel Emulator on or off.
When this function is On, the Output Monitor in **Manual Setting** tab graphs the emulated results of S parameter characteristics and outputs the waveforms.

Off:	Turns Off Emulator.
On:	Turns On Emulator.

[2] Load the S parameter file of the DUT. Touch **Open** to display the file loading dialog box, "**Open S-Parameter File**". By selecting the S parameter file on this dialog box, Emphasis according to **Response** setting is set.

[3] Touch **Clear** to clear the currently loaded S parameter file.

[4] Selects a file type for s4p files.
This item is displayed when the loaded file in [2] is an s4p file.

1and3: Select this when the loaded s4p file has been assigned input port and output port as below.
Input Port: Port 1, Port 3
Output Port: Port 2, Port 4

Note:

Select this to open an s4p file of MICROWAVE NETWORK ANALYZER, MS4640.

1and2: Select this when the loaded s4p file has been assigned input port and output port as below.
Input Port: Port 1, Port 2
Output Port: Port 3, Port 4

[5] Select how to emulate impulse response from S parameter file.

Normal: Emulate Non-Inverse impulse response.
Select this to emulate channel characteristics.

Inverse: Emulate inverse impulse response.
Select this to compensate channel loss.

Note:

If **Inverse** is selected, inverse characteristics of channel are emulated.
Inverse characteristics of the channel can be computed by inverse Fourier transform of an inverse number of channel frequency characteristics (inverse number of channel transfer function).
Thus, channel inverse response exceeding the hardware limit can be emulated depending on S parameter file.
Not to exceed the hardware limit, Channel Emulator normalizes the maximum value of the output (Va-Vj) to 1.000 Vpp when the amplitude setting is 1.000 Vpp.
Therefore, it is not guaranteed to compensate channel response of any S parameter file without lowering the output level by normalization, when Channel Emulator is used for compensating Channel.

[6] The Bitrate of the MU195020A is displayed.

[7] By touching **Transfer**, the emulated results of Channel Emulator are transferred to the **Manual Setting** tab.
The transferred emulated results are overwritten as coefficient parameters. Also, when the transfer is completed, Channel Emulator is turned Off.

5.2.5 ISI Setting

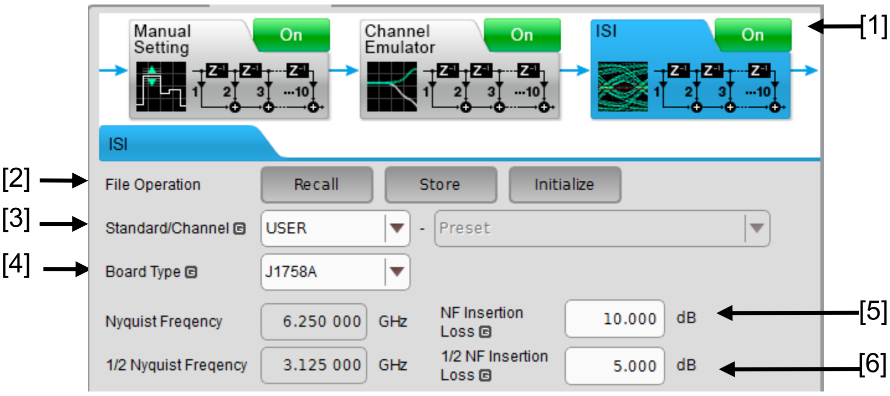


Figure 5.2.5-1 Emphasis Tab ISI Setting

Note:

ISI is enabled only when MU195020A-x40 or MU195020A-x41 is installed.

[1] Set ISI on or off.

Off: ISI can be set, but the value cannot re reflected to the waveform.

On: ISI is added to the waveform output from the front panel.

[2] File Operation to store, recall, and initialize preset setting.

Table 5.2.5-1 File Operation Buttons

Button	Function
Recall	Recalls the saved setting and set Preset.
Store	Stores Preset setting.
Initialize	Restores defaults.

[3] Set the standard to be referenced and the Calibration channel. When they are set, the Insertion Loss is automatically configured.

Table 5.2.5-2 Available Standards and Calibration Channel

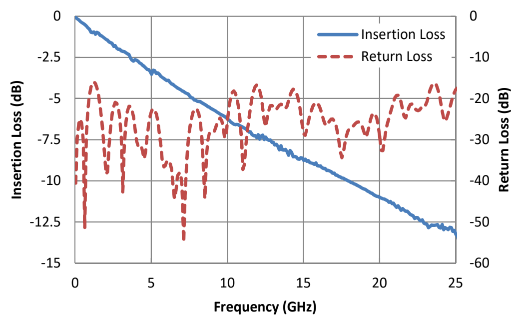
Preset Standard	Calibration Channel
CEI-28G	Short Reach 300 mm
	Medium Reach
	Very Short Reach
CEI-25G	Long Reach 686 mm
USER	The user can set arbitrary insertion loss.

[4] Select the ISI Board to use. To use the ISI Board not on this list and add loss to it, select **Not Specified**.

When **J1758A** is selected, the settings in [5] and [6] are treated as absolute values. It means that the output after passing J1758A is equivalent to the Insertion Loss that are set in [5] and [6] and the output in Nyquist frequency is in the range of the Insertion Loss (1.5 to 25.0 dB).

When **Not Specified** is selected, the settings in [5] and [6] are treated as relative values. It means that the loss of the used ISI board itself and the Insertion Loss set in [5] and [6] are added to the output through the board. And the output in Nyquist frequency is in the range of the Insertion Loss (1.5 to 25.0 dB) + xxdB (loss of board itself).

Table 5.2.5-3 Board Type List

Board Type	Frequency Characteristics (Typical)
J1758A	

[5] Set the Insertion Loss at Nyquist frequency. When setting Standard to **USER**, Nyquist frequency is automatically set from the Bit Rate. When other than **USER** is selected, the frequency corresponding to various standards are displayed.

[6] Set the Insertion Loss at half the frequency of the Nyquist frequency. The Insertion loss here should be equal to or below the Insertion Loss at Nyquist frequency.

5 Operation Method

5.3 Setting Test Patterns (MU195020A)

To set the PPG pattern, touch the **Pattern** tab on the MU195020A operation screen. Select a test pattern and set other items.

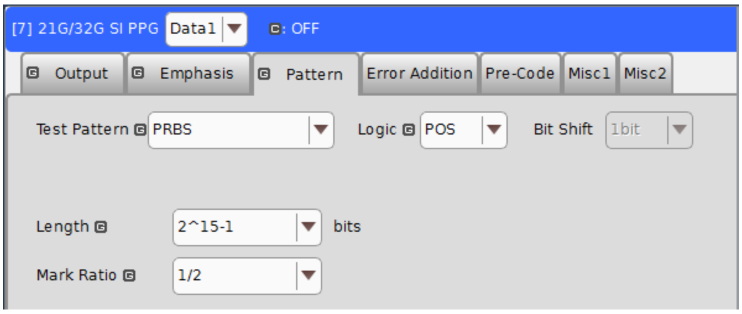


Figure 5.3-1 Pattern tab

5.3.1 Test Pattern type

The following six test patterns can be selected.

- PRBS
- ZeroSubstitution
- Data
- Mixed
- PAM4
- Sequence

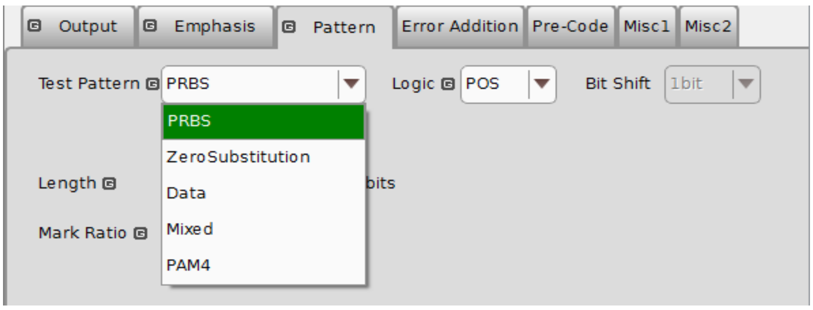


Figure 5.3.1-1 Selecting test pattern

How to set each test pattern is described in the subsequent sections.

5.3.2 Setting PRBS pattern

This section describes how to set the parameters required when **PRBS** is selected as the test pattern.

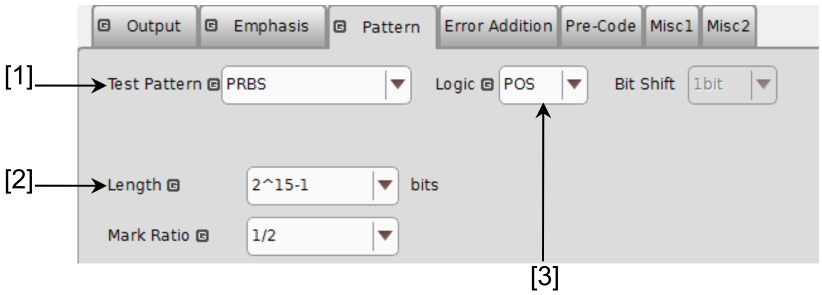


Figure 5.3.2-1 Setting items for Test Pattern (PRBS)

[1] Select **PRBS**.

[2] Set the number of the PRBS pattern stages.
Set the PRBS pattern length in the format of 2^n–1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31).

[3] Set the logic of the test pattern.

Table 5.3.2-1 Test pattern logic setting

Setting	Description
POS (positive logic)	The high level of a signal is defined as “0”.
NEG (negative logic)	The high level of a signal is defined as “1”.

Refer to Appendix A “Pseudo-Random Pattern” for the PRBS pattern generation principle.

5.3.3 Setting ZeroSubstitution pattern

This section describes how to set the parameters required when **ZeroSubstitution** is selected as the test pattern.

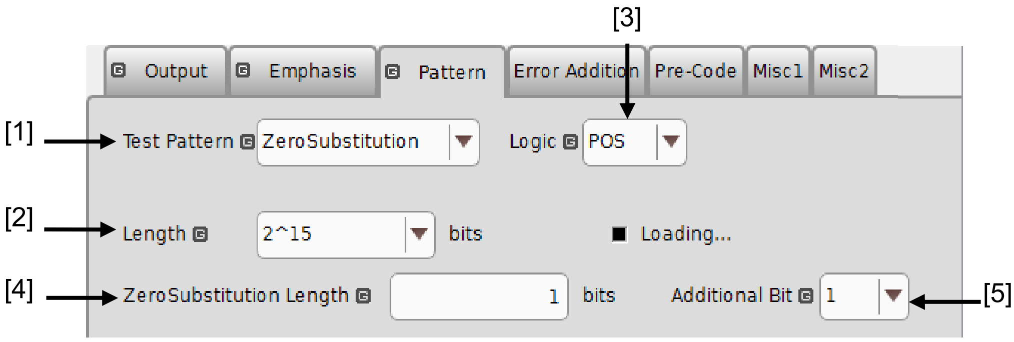


Figure 5.3.3-1 Setting items for ZeroSubstitution pattern

[1] Select **ZeroSubstitution** from the Test Pattern drop-down list. Test pattern loading starts and the **Loading...** LED lights.

[2] Set the configuration (number of stages) of the zero-insertion pattern test signal.

Select either of the following test pattern signals.
2^n (n = 7, 9, 10, 11, 15, 20, or 23) [Compatible with the MP1800A]
$2^n–1$ (n = 7, 9, 10, 11, 15, 20, or 23) [Pure PRBS signal]

[3] Set the logic of the test pattern.

Table 5.3.3-1 Test pattern logic setting

Setting	Description
POS (positive logic)	The high level of a signal is defined as “1”.
NEG (negative logic)	The high level of a signal is defined as “0”.

[4] Set the number of 0-insertion (substitution) bits. The number of available 0-insertion bits varies depending on the pattern test signal selected from the Length drop-down list ([2] in Figure 5.3.3-1) as follows.

(a) When $2^n–1$ is set for Length: 1 to $2^n–2$, in 1-bit steps

(b) When 2^n is set for Length: 1 to $2^n–1$, in 1-bit steps

[5] Set the final bit of the zero-insertion pattern.
Note that this setting is invalid when Length is set to 2^n–1.

Table 5.3.3-2 Setting of last bit of zero-insertion pattern

Setting	Description
1	The 2^nth bit is set to "1" (compatible with the MP1800A).
0	In order to make an M-series signal, 1 bit of "0" is added to the last of consecutive 0 strings to configure a zero-insertion pattern.

Note:

The data amplitude of MU195020A output with the following patterns may be attenuated by around 50% or the offset voltage (Vth) may be fluctuated.

- The pattern in the period of approximately 5 μs which follows continuous "0" or "1" with 5 μs or more.
  This kind of pattern may be generated by inserting continuous "0" or "1" or by a burst pattern.
- The pattern other than its mark ratio of 1/2.

When MU195040A receives the data with such a pattern, the optimum threshold voltage may not match the offset voltage of MU195020A.

This mismatch may cause bit errors. In this case, check the data signal using an oscilloscope etc. to adjust the threshold voltage.

5.3.4 Setting Data pattern

This section describes how to set the parameters required when **Data** is selected as the test pattern.

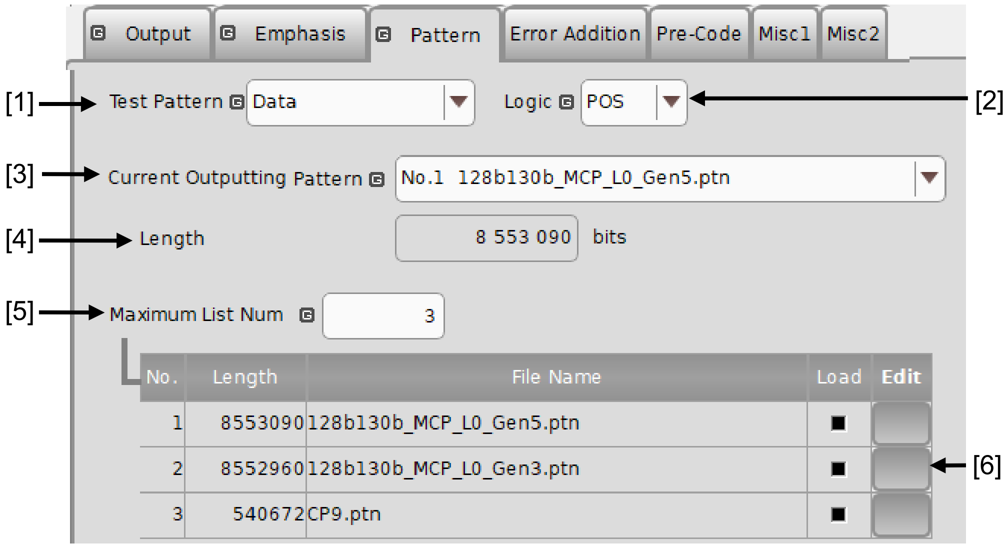


Figure 5.3.4-1 Setting items for Data pattern

[1] Select **Data** from the Test Pattern drop-down list.
Test pattern loading starts and the **Loading…** LED lights.

[2] Set the logic of the test pattern.

Table 5.3.4-1 Test pattern logic setting

Setting	Description
POS (positive logic)	The high level of a signal is defined as “1”.
NEG (negative logic)	The high level of a signal is defined as “0”.

[3] Select a test pattern to output.
From the test patterns loaded by [5] and [6], select one to actually output. If the test pattern is changed here, the MU195020A can switch test patterns without interruption.

[4] The length of the test pattern data currently set is displayed.

Notes:

- It may take a long time to load a test pattern when the data length is long.

  Refer to the following reference loading time values, for the cases where the data length is set to maximum. These values are only references and do not guarantee the Loading time.

  Maximum loading time for 1ch: About 4 min.
  Maximum loading time for 2ch: About 8 min.

- The data amplitude of MU195020A output with the following patterns may be attenuated by around 50% or the offset voltage (Vth) may be fluctuated.

  - The pattern in the period of approximately 5 μs which follows continuous “0” or “1” with 5 μs or more.
    This kind of pattern may be generated by inserting continuous “0” or “1” or by a burst pattern.
  - The pattern other than its mark ratio of 1/2.

  When MU195040A receives the data with such a pattern, the optimum threshold voltage may not match the offset voltage of MU195020A.

  This mismatch may cause bit errors. In this case, check the data signal using an oscilloscope etc. to adjust the threshold voltage.

- When the Test Pattern is Data or Mixed, if the MU195040A receives a signal that is a combined signal of “PRBS pattern after continuous **0** bits (shown in [-])” and “PRBS pattern after continuous **1** bits”, then the optimum threshold voltages of them are each different. Due to this difference, bit errors in all patterns may not be measured.

[5] Select the maximum number of test patterns that can be loaded to the MU195020A.
When, after the application is started, Data is selected in Test Pattern, the selected number of test patterns are loaded. When an already loaded test pattern is selected at [3], you can switch to it without loading again.

[6] Touch **Edit** to open the **Pattern Editor** dialog box in which test patterns can be edited.
When editing of a test pattern is finished, touch **OK** to close the **Pattern Editor** dialog box. The edited test pattern is then loaded to the hardware. The **Loading…** LED lights during Data pattern loading. Refer to “5.3.7 Editing test pattern in Pattern Editor dialog box” for details on how to edit test patterns in the **Pattern Editor** dialog box.

5.3.5 Setting Mixed pattern

When **Mixed** is selected, a block consisting of programmable test patterns and PRBS patterns can be set.

A programmable test pattern added with a PRBS pattern is defined as “row”, one block is composed of two or more rows. A mixed data test pattern is set by configuring multiple blocks.

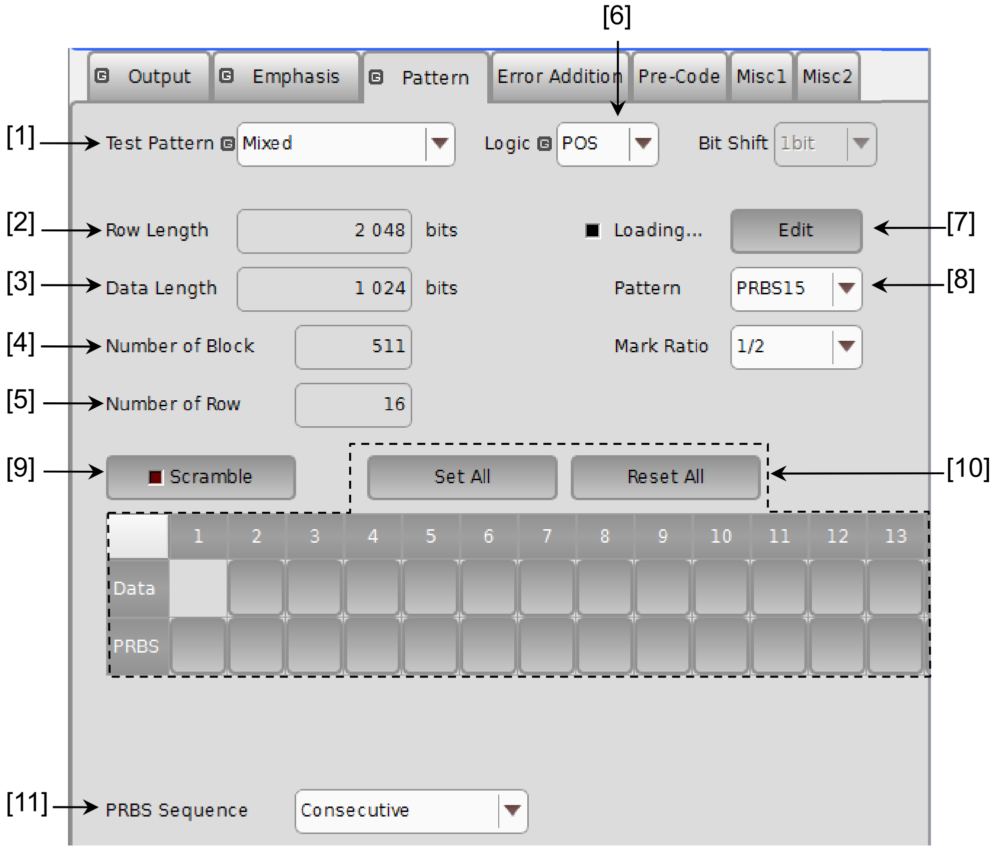


Figure 5.3.5-1 Setting items for Test Pattern (Mixed Data)

[1] Select **Mixed**.

[2] The length of rows edited in the **Pattern Editor** dialog box is displayed.

[3] The length of the Data pattern edited in the **Pattern Editor** dialog box is displayed.

[4] The number of all blocks in the pattern data edited in the **Pattern Editor** dialog box is displayed. The maximum number of blocks is 511.

[5] The length of 1 row of the pattern data edited in the **Pattern Editor** dialog box is displayed.

[6] Set the logic of the test pattern.

Table 5.3.5-1 Test pattern logic setting

Setting	Description
POS (positive logic)	The high level of a signal is defined as “1”.
NEG (negative logic)	The high level of a signal is defined as “0”.

[7] Touch **Edit** to open the **Pattern Editor** dialog box in which test patterns can be edited.
When editing of a test pattern is finished, touch **OK** to close the **Pattern Editor** dialog box. The edited test pattern is then loaded to the hardware (Loading). The **Loading…** LED lights during test pattern loading. Refer to “5.3.7 Editing test pattern in Pattern Editor dialog box” for details on how to edit test patterns in the **Pattern Editor** dialog box.

Notes:

- It may take a long time to load a test pattern when the data length is long.

  Refer to the following reference loading time values, for the cases where the data length is set to maximum. These values are only references and do not guarantee the Loading time.

  Maximum loading time for 1ch: About 1 min.
  Maximum loading time for 2ch: About 2 min.

- The data amplitude of MU195020A output with the following patterns may be attenuated by around 50% or the offset voltage (Vth) may be fluctuated.

  - The pattern in the period of approximately 5 μs which follows continuous “0” or “1” with 5 μs or more.
    This kind of pattern may be generated by inserting continuous “0” or “1” or by a burst pattern.
  - The pattern other than its mark ratio of 1/2.

  When MU195040A receives the data with such a pattern, the optimum threshold voltage may not match the offset voltage of MU195020A.

  This mismatch may cause bit errors. In this case, check the data signal using an oscilloscope etc. to adjust the threshold voltage.

- When the Test Pattern is Data or Mixed, if the MU195040A receives a signal that is a combined signal of “PRBS pattern after continuous **0** bits” and “PRBS pattern after continuous **1** bits”, then the optimum threshold voltages of them are each different. Due to this difference, bit errors in all patterns may not be measured.

[8] Set the number of the PRBS pattern stages.
Set the PRBS pattern length in the format of 2^n-1 (n = 7, 9, 10, 11, 15, 20, 23, 31).

[9] Set scramble ON/OFF.

Scramble of PRBS7 can be set for the area specified by the setting of [10].

When **Scramble** is touched while the LED on the button is off, the LED lights and scramble is executed for the output signal. The scramble area is displayed red in the block configuration display area.
When **Scramble** is touched while the LED on the button is on, the LED goes off and scramble for the output signal is stopped.

[10] Configure the scramble settings.

Touch **Set All** to enable all area. Touch **Reset All** to disable all area. Select at least one desired area to enable scramble individually.

Note:

Scramble cannot be set for the data area of the first row in each block.

[11] Set the PRBS signal generation method.
Set the continuity of the PRBS pattern strings in a Mixed pattern.

Table 5.3.5-2 PRBS signal generation method setting

Setting	Description
Restart	The end of the PRBS of the specified last block and the start of the PRBS of the next subsequent block are not continuous.
Consecutive	The end of the PRBS of the specified last block and the start of the PRBS of the next subsequent block are continuous.

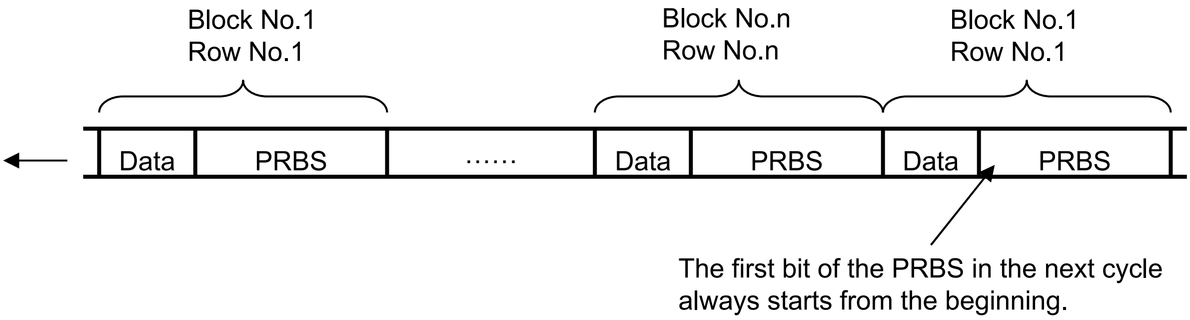


Figure 5.3.5-2 Continuity of PRBS pattern strings (Restart)

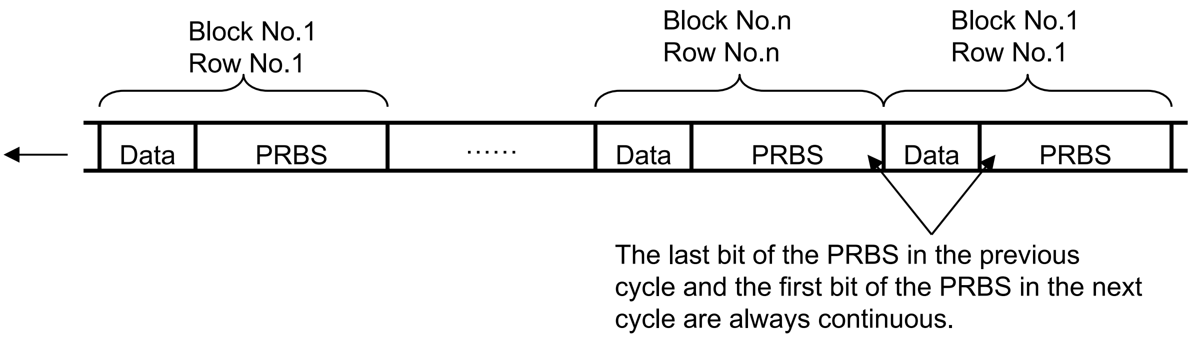


Figure 5.3.5-3 Continuity of PRBS pattern strings (Consecutive)

5.3.6 Setting PAM4

Set various parameters when **PAM4** is selected for Test Pattern.
PAM4 is displayed when **2 ch Combination** or **64 G × 2 ch Combination** is set using the inter-module synchronization function.
For details of the inter-module synchronization function, see 5.9 “Inter-module Synchronization Function”.

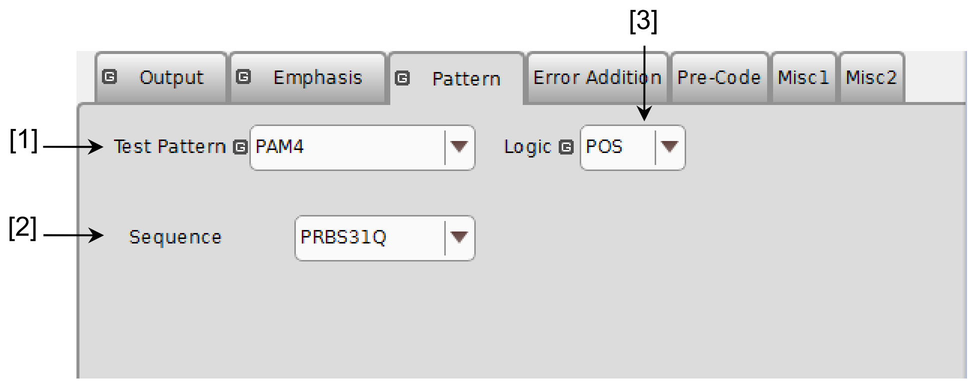


Figure 5.3.6-1 Test Pattern (PAM4) Setting Dialog Box

[1] Select **PAM4**.

[2] Set the sequence of the test pattern.

[3] Set the logic of the test pattern.

Table 5.3.6-1 Test pattern logic setting

Setting	Description
POS (positive logic)	The high level of a signal is defined as “1”.
NEG (negative logic)	The high level of a signal is defined as “0”.

When Sequence is selected as **User Define**, it is possible to set arbitrary number of PRBS steps and user defined patterns.

By setting **PRBS** to Raw Data, it is possible to generate a test pattern based on the PRBS pattern.

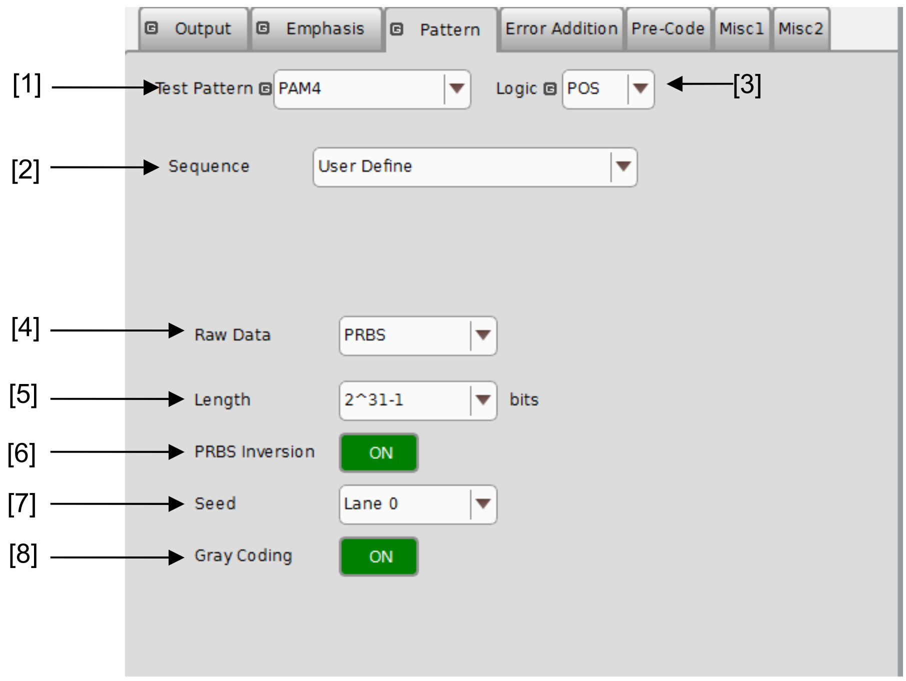


Figure 5.3.6-2 Setting Items for Test Pattern (PAM4-PRBS)

[1] Select **PAM4**.

[2] Set the sequence of the test pattern.

[3] Set the logic of the test pattern.

[4] Select the Raw Data **PRBS**.

[5] Set the number of the PRBS pattern stages (Length).
Set the PRBS pattern length in the format of 2^n-1 (n = 7, 9, 10, 11, 15, 20, 23, 31).

[6] Set the logic (PRBS Inversion) of ON or OFF.

The relationship of PRBS Inversion, test pattern logic and Gray Coding is as the figure below.

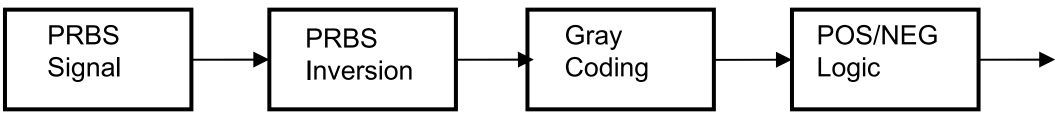


Figure 5.3.6-3 Block Diagram of Pattern Generation

[7] Set the initial value (Seed) of the PRBS.

Considering that multiple PAM4 signals may be used (Lane0 to 3), a phase between lanes can be shifted by changing the initial value (Seed) of PRBS pattern.

[8] Set the Gray Coding ON or OFF.

Gray Coding is as the following table. And the PAM4 pattern waveform is as the following figure.

Table 5.3.6-2 Gray Coding Chart

Binary Code	Gray Code
00	00
01	01
10	11
11	10

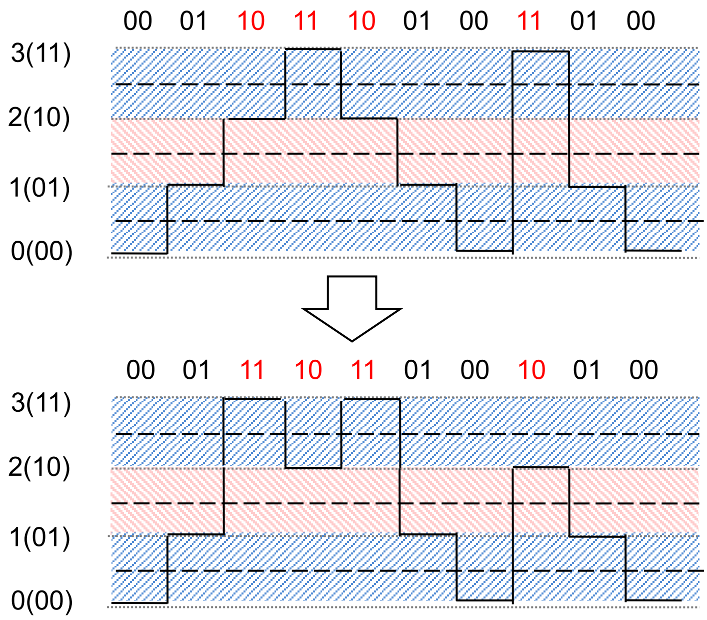


Figure 5.3.6-4 Gray Coding PAM4 Pattern Waveform

Refer to Appendix A “Pseudo-Random Pattern” for PRBS generation principle.

It is possible to generate a test pattern based on an editable pattern file by setting **Data** to Raw Data.

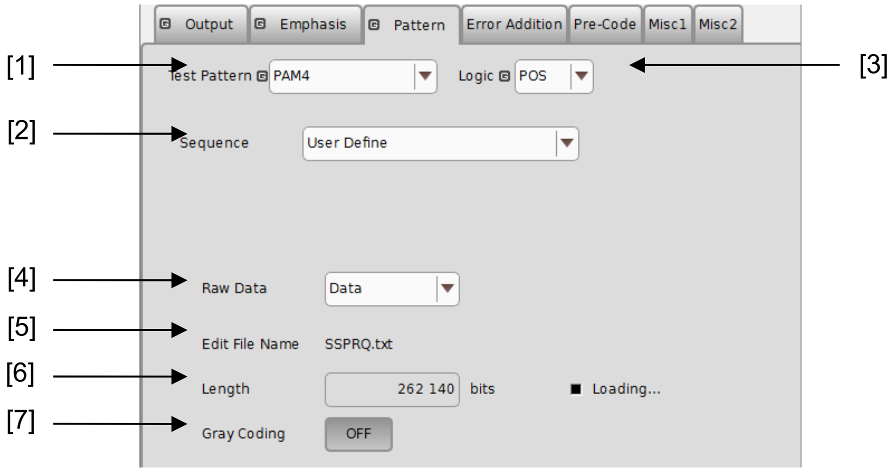


Figure 5.3.6-5 Test Pattern (PAM4-Data) Setting Dialog Box

[1] Select **PAM4**.

[2] Set the sequence of the test pattern.

[3] Set the logic of the test pattern.

[4] Set the Raw Data **Data**.
Test pattern loading starts and the **Loading...** LED lights.

[5] The name of set pattern file is shown here.
If file name is not set, "---" is displayed.

[6] The data length of the set test pattern is displayed.

[7] Set the Gray Coding ON or OFF.

Notes:

- It may take a long time to load a test pattern when the data length is long.

  Refer to the following reference loading time values, for the cases where the data length is set to maximum. These values are only references and do not guarantee the Loading time.

  The maximum loading time: Around 8 minutes

- The data amplitude of MU195020A output with the following patterns may be attenuated by around 50% or the offset voltage (Vth) may be fluctuated.

  - The pattern in the period of approximately 5 μs which follows continuous "0" or "1" with 5 μs or more.
    This kind of pattern may be generated by inserting

continuous “0” or “1” or by a burst pattern.

- The pattern other than its mark ratio of 1/2.

When MU195040A receives the data with such a pattern, the optimum threshold voltage may not match the offset voltage of MU195020A.

This mismatch may cause bit errors. In this case, check the data signal using an oscilloscope etc. to adjust the threshold voltage.

5.3.7 Editing test pattern in Pattern Editor dialog box

This section describes how to edit test patterns with the following patterns selected on the **Pattern** tab.

- Data
- Mixed

5.3.7.1 Common setting items

Touch **Edit** on the **Pattern** tab to display the **Pattern Editor** dialog box.

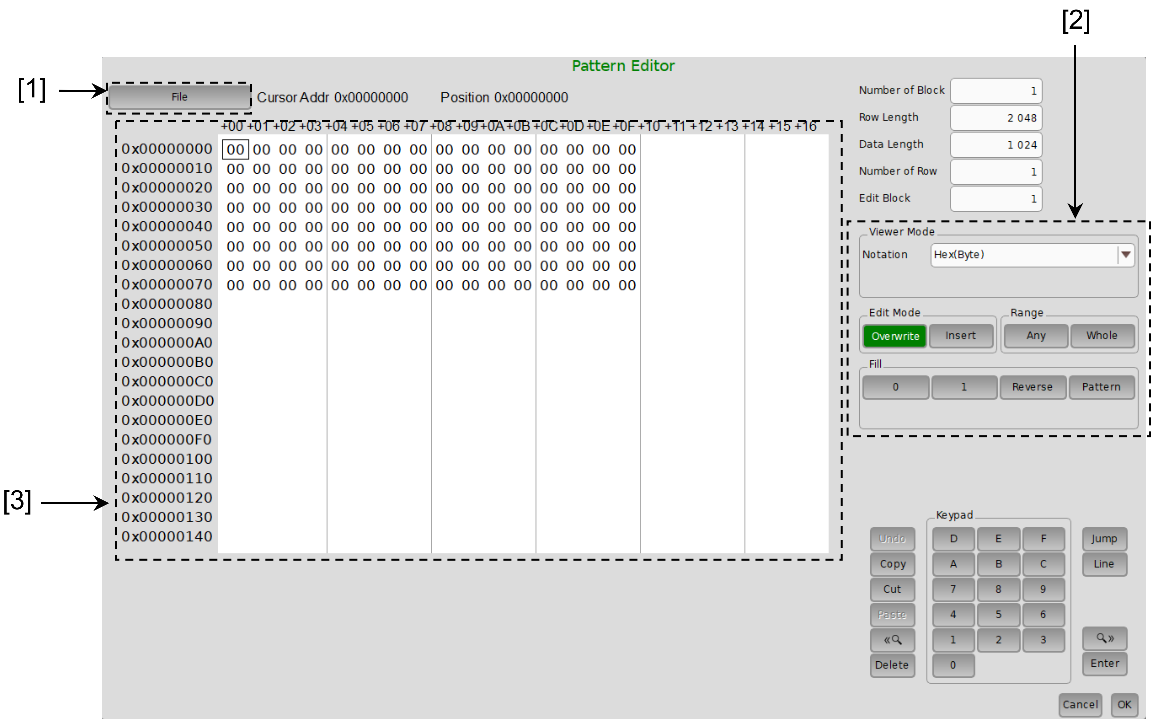


Figure 5.3.7.1-1 Pattern Editor Dialog Box

[1] Menu items on menu bar

Table 5.3.7.1-1 Menu bar configuration

Button	Menu item	Description
File	Open	Opens a setup file saved in the binary pattern, binary text pattern, or hexadecimal text pattern format. For file compatibility, refer to 5.3.7.7 “Compatibility with test pattern files of existing models”.
	Save	Saves a setting file in the binary pattern (Binary Pattern), binary text pattern (BIN Text Pattern), or hexadecimal text pattern (HEX Text Pattern) format. ***Note:*** The settings will not be read from the saved file if the file name is changed.
Undo		Restores the previous state.
Copy		Copies the pattern selected in the Pattern View area into the internal memory.
Cut		Over write: Cuts the pattern selected in the Pattern View area and transfers it onto the clipboard. The area that has been cut out becomes 0. Insert: Cuts the selected pattern with its address domain. After cutting, zero pattern with the same amount of the cut domain is added instead at the end of pattern length.
Paste		Pastes the pattern copied in the internal memory to the cursor position.
Jump		Moves the cursor to a specified address or pattern.
	Head	Moves the cursor to the start of the editing pattern.
	Tail	Moves the cursor to the end of the editing pattern.
	Address	Opens the **Input Address** dialog box. The cursor can be moved to the specified address position.
	Pattern	Opens the **Input Pattern** dialog box. Specifies a pattern string to search by binary digits. If a pattern matching the search condition is found in the editing pattern, the cursor moves to that position. Both forward search and backward search are supported. The search pattern can be specified in the **Input Pattern** dialog box. **Set ALL**: Set all the bits to “1”. **Reset ALL**: Set all the bits to “0”. Select the search direction by touching **Forward** or **Backward**, and then touch **OK**.

Table 5.3.7.1-1 Menu bar configuration (Cont'd)

Button	Menu item	Description
Jump (Cont'd)	Forward Next	Searches for a pattern that matches the search pattern set in the **Input Pattern** dialog box in the forward direction. If a matching pattern is found, the cursor moves to that position.
	Backward Next	Searches for a pattern that matches the search pattern set in the **Input Pattern** dialog box in the backward direction. If a matching pattern is found, the cursor moves to that position.
Line		Specifies the number of characters per line in the Pattern View area. This is available when the pattern setting item Display is set to **Table**.

[2] Pattern setting items

Table 5.3.7.1-2 Pattern setting items

Setting item	Description
Notation	Specify the pattern display format in the Pattern View area. Bin: Binary Hex: Hexadecimal
Edit Mode	Specify the pattern editing method. This must be specified in advance when executing Paste from the Edit menu or when performing direct editing in the Pattern View area (except for the Fill setting area). Overwrite: The selected pattern is overwritten. Insert: The editing pattern is inserted into the position of the selected pattern. Note that Data Length is not changed when Insert is selected. The inserted pattern therefore exceeds the Data Length value, and becomes invalid.
Range	Specify the pattern editing range. Whole: All editing patterns are selected as the editing range. Any: The Input Range Dialog Box (see Figure 5.3.7.1-2) is displayed when this button is touched. The editing range can be specified by an address. Direct: Select an arbitrary area by specifying addresses. Use the cursor to specify addresses. Refer to 5.3.7.5 “Editing area” for details.
Fill	Edits the pattern part highlighted by the cursor. 0: The highlighted part in the Pattern View area is set to “0”. 1: The highlighted part in the Pattern View area is set to “1”. Reverse: The highlighted part in the Pattern View area is logically inverted. Pattern: The Input Pattern Dialog Box (see Figure 5.3.7.1-3) is displayed. The highlighted part in the Pattern View area can be edited in this dialog box. Repeat: The edited pattern for which the highlighted address is set to the first is repeated for the number of times specified here. Length: Specify the number of edit bits from the start address of the highlighted part. Set All: Sets all the bits selected by Length to “1”. Reset All: Sets all the bits selected by Length to “0”.

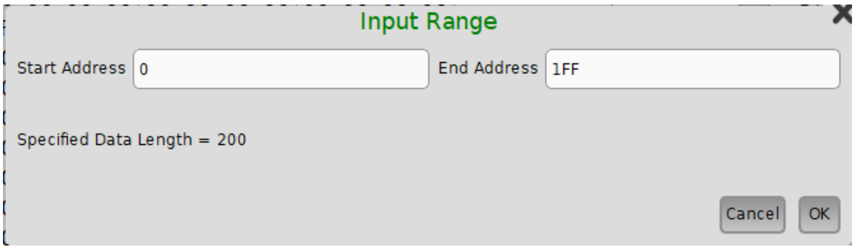


Figure 5.3.7.1-2 Input Range Dialog Box

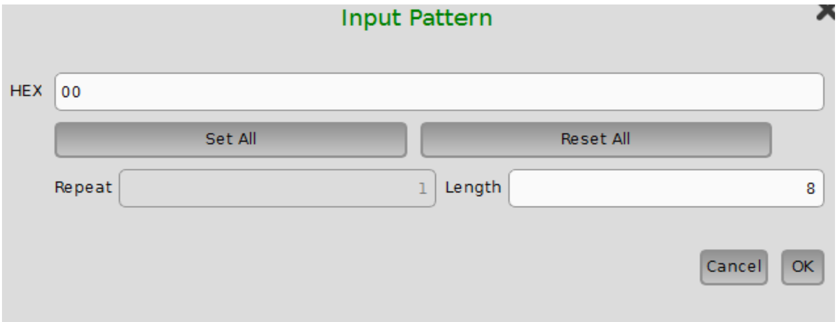


Figure 5.3.7.1-3 Input Pattern Dialog Box

[3] Pattern View area

The edited pattern is displayed in this area.
Touching a pattern enables the bit value to be changed.

5.3.7.2 Editing Data pattern

When **Edit** is touched while **Data** is selected for the test pattern, the **Pattern Editor** dialog box shown in Figure 5.3.7.2-1 is displayed.

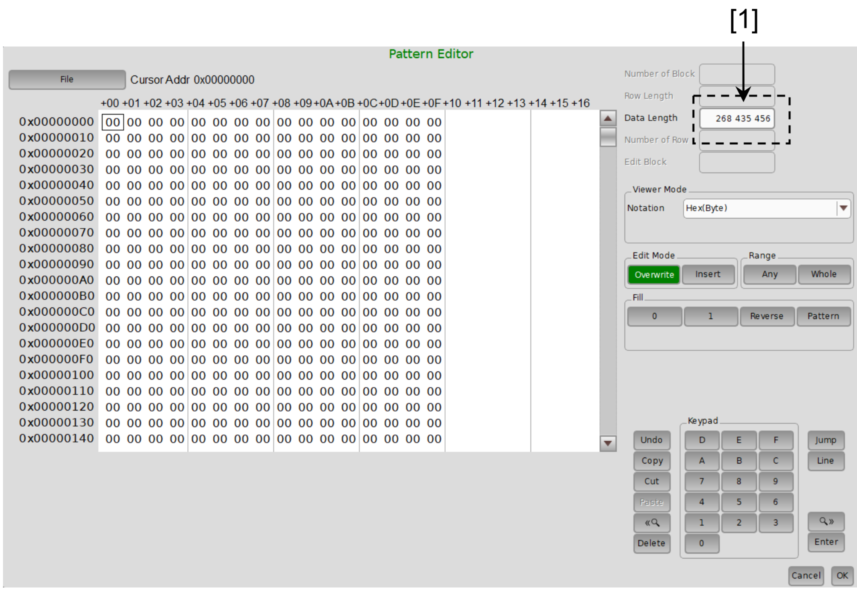


Figure 5.3.7.2-1 Pattern Editor Dialog Box for Data pattern

[1] Pattern setting item

Table 5.3.7.2-1 Pattern setting items (when Data is selected)

Setting item	Description
Data Length	Set the length of the Data pattern. The setting unit is one bit. 2 to 268 435 456 bits can be set, in 1-bit steps. In the case of 2ch Combination, 4 to 536 870 912 bits can be set, in 2-bit steps.

5.3.7.3 Editing Mixed pattern

When **Edit** is touched while Mixed is selected for the test pattern, the **Pattern Editor** dialog box shown in Figure 5.3.7.3-1 is displayed.

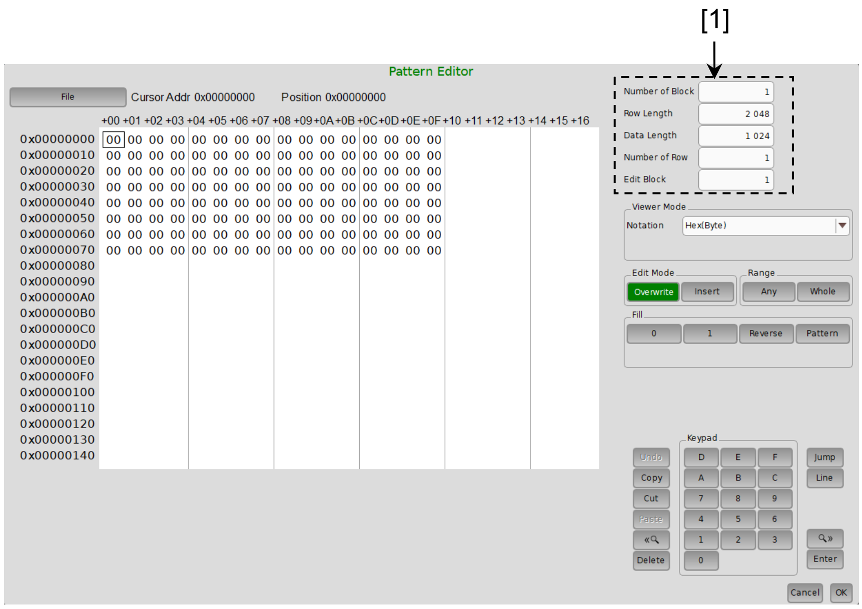


Figure 5.3.7.3-1 Pattern Editor Dialog Box for Mixed pattern

[1] Pattern setting items

Table 5.3.7.3-1 Pattern setting items (when Mixed is selected)

Setting item	Description
Number of Block	Set the number of blocks from 1 to 511, in 1-block steps.
Row Length	Set the row length. Can be set from 2 048 to 2 415 919 104 bits, in 256-bit steps. In the case of 2ch Combination, set from 4 096 to 4 831 838 208 bits in 512-bit steps.
Data Length	Set the pattern length. Can be set from 1 024 to 268 435 456 bits, in 1-bit steps. In the case of 2ch Combination, set from 2 048 to 536 870 912 bits in 2-bit steps.
Number of Row	Set the number of rows from 1 to 16, in 1-row steps.
Edit Block	Specify the number of blocks to be edited.

Note:

The number of blocks and the number of rows are restricted as follows.

Number of blocks

1 to the smallest number among a to d, below, in 1-block steps

a) 511

b) $\mathrm{INT}\left(\dfrac{256\mathrm{Mbits} \times x}{\mathrm{Number\ of\ rows} \times \mathrm{DataLength'}}\right)$

where Data Length' is:

- When Data Length is indivisible by (256 × x)

  $= (\mathrm{INT}(\dfrac{\mathrm{DataLength}}{256 \times x}) + 1) \times 256 \times x$

- When Data Length is divisible by (256 × x)

  = Data Length

Maximum Block number should satisfy:

Data Length' x Number of Rows × Number of Blocks ≤ 256 Mbits

c) $\mathrm{INT}\left(\dfrac{(256\mathrm{Mbits} + 2^{31}) \times x}{\mathrm{RowLength} \times \mathrm{Number\ of\ rows}}\right)$

where x is:

1 for Independent

2 for 2ch Combination

d) (Row Length – Data Length) × Number of blocks ≥2^31(2147483648)

Number of Rows

1 to the smallest number among a to c, below, in 1-row steps

a) 16

b) $\mathrm{INT}\left(\dfrac{256\mathrm{Mbits} \times x}{\mathrm{DataLength'}}\right)$

where Data Length' is:

- When Data Length is indivisible by (256 × x)

  $= (\mathrm{INT}(\dfrac{\mathrm{DataLength}}{256 \times x}) + 1) \times 256 \times x$

- When Data Length is divisible by (256 × x)

  = Data Length

Maximum Row number which meets:

Data Length' × Number of Rows × Number of Blocks ≤ 256 Mbits

c) $\mathrm{INT}\left(\dfrac{(256\mathrm{Mbits} + 2^{31}) \times x}{\mathrm{RowLength}}\right)$

where x is:

1 for Independent

2 for 2ch Combination

5.3.7.4 Creating and editing test pattern

This section describes how to create and edit a test pattern in the **Pattern Editor** dialog box.

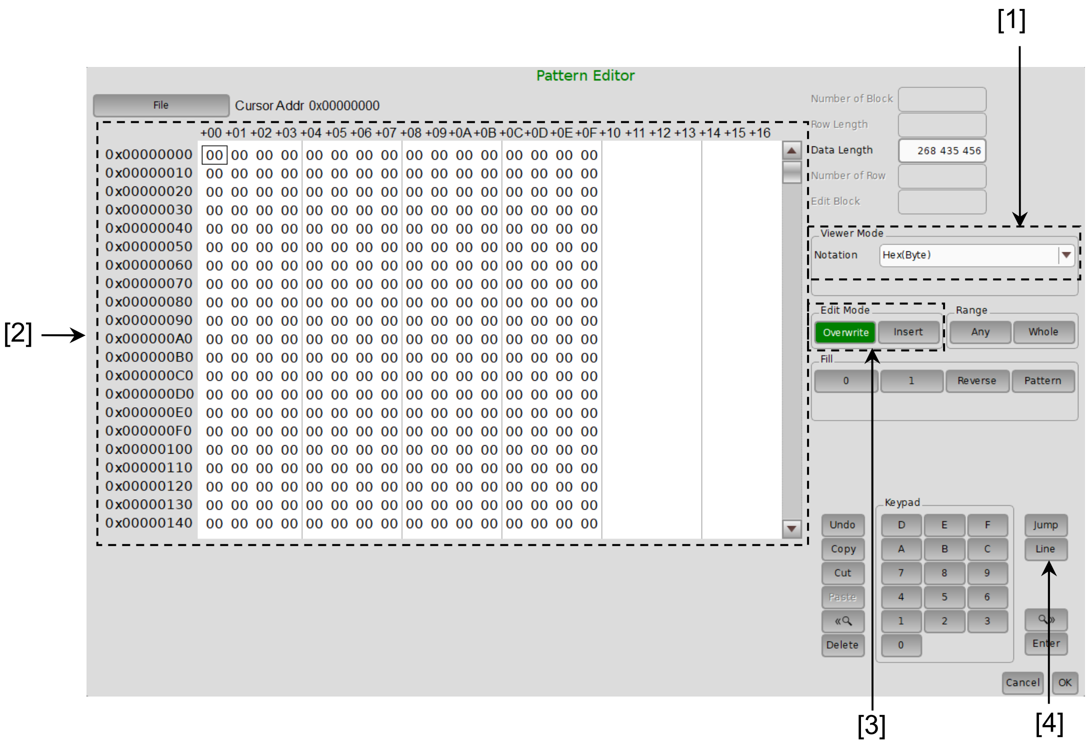


Figure 5.3.7.4-1 Pattern Editor Dialog Box

[1] Select the display format.

Table 5.3.7.4-1 Display format setting

Setting item	Description
Bin	A test pattern is displayed and edited in binary.
Hex	A test pattern is displayed and edited in hexadecimal format.

[2] Use the 0 and 1 buttons for pattern input when the display format is binary. Use 0 to 9 and A to F buttons when the display format is hexadecimal.

[3] Set the editing mode.
Editing is performed in the insertion mode when **Insert** is touched, and is performed in the overwriting mode when **Overwrite** is touched.

[4] The amount of data to be displayed in one line can be changed.
Touch **Line** to open the **Line** dialog box. Enter the number of bytes per line in the textbox, and then touch **OK**.

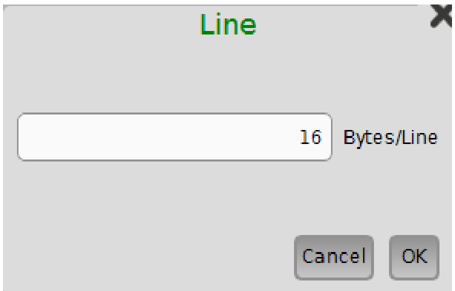


Figure 5.3.7.4-2 Line Dialog Box

5.3.7.5 Editing area

In the **Pattern Editor** dialog box, batch editing is possible for an area by selecting it consisting of multiple bits. In this area, perform replace input using the buttons in the Fill frame, or use Cut, Copy, and Paste editing commands.
The selection area setting procedure by using buttons in the Range frame is described below.

The function of each button is as follows:

Table 5.3.7.5-1 Area specification buttons

Button	Function
Whole	Specifies entire of the pattern as the selection area.
Any	Sets an arbitrary area as the selection area by specifying addresses. The address is specified by entering values in the **Input Range** dialog box.
Direct	Sets an arbitrary area as the selection area by specifying addresses. The address is specified by using a cursor.

How to specify the selection area using the **Any** is as follows.

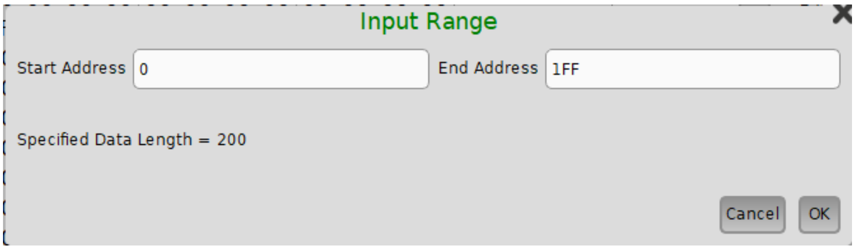


Figure 5.3.7.5-1 Input Range Dialog Box

1. Enter the start address of the selection area in the **Start Address** box.
2. Enter the end address of the selection area in the **End Address** box.
3. Touch **OK** to set the specified area as the selection area. The selection area is highlighted in the **Pattern Editor** dialog box.

How to specify the selection area using the **Direct** is as follows.

1. Touch **Direct**.
   The color of the button turns green and the operation changes to **Direct**. Note that pattern input and editing cannot be performed in the **Direct**.
2. Specify the start position of the selection area by touching twice the desired position.
3. Specify the end position of the selection area by touching once the desired position.
4. The selection area is now completely set.

The selection area can also be specified by dragging the mouse.

5.3.7.6 Inputting pattern

How to input a pattern by using the buttons in the Fill frame is described below. The function of each button is as follows:

Table 5.3.7.6-1 Fill button functions

Button	Function
0	Replaces the bit of the cursor position or the bits in the selection area to “0”.
1	Replaces the bit of the cursor position or the bits in the selection area to “1”.
Reverse	Inverts the bit of the cursor position or the bits in the selection area.
Pattern	Inputs an arbitrary pattern repeatedly.

■ How to input a pattern using the **Pattern** is as follows.

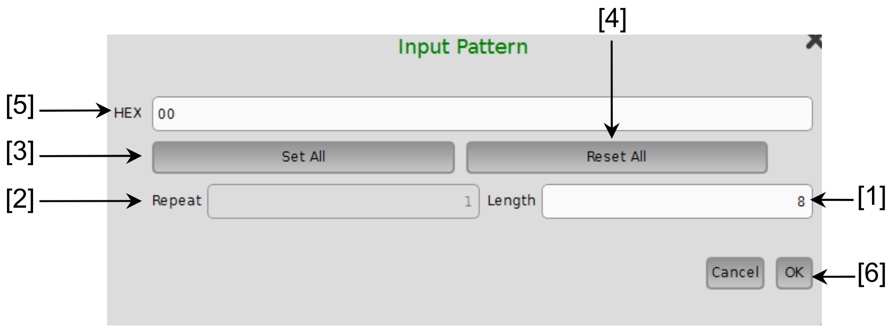


Figure 5.3.7.6-1 Input Pattern Dialog Box

[1] Enter the number of bits to be input.

[2] Enter the number of specified pattern repetition times.

[3] Touch **Set All** to set all the bits to “1”.

[4] Touch **Reset All** to set all the bits to “0”.

[5] Input a pattern into the BIN or HEX textbox.

[6] Touch **OK** to input the pattern to the cursor position.

Note:

When the **Input Pattern** dialog box is displayed while the selection area is specified, a repetition of the specified pattern is applied to the selection area, regardless of the number of repetition times specified in the Repeat spin box.

5.3.7.7 Compatibility with test pattern files of existing models

Pattern files (.PTN) created for the following existing models can be loaded into the **Pattern Editor** dialog box of the MU195020A.

MP1632C	Digital Data Analyzer
MP1761A/B/C	Pulse Pattern Generator
MP1762A/C/D	Error Detector
MP1775A	Pulse Pattern Generator
MP1776A	Error Detector
MU181020A/B	Pulse Pattern Generator
MU181040A/B	Error Detector
MU183020A	Pulse Pattern Generator
MU183021A	Pulse Pattern Generator
MU183040A/B	Error Detector
MU183041A/B	Error Detector

5.3.8 Setting Sequence

This section describes how to use the MU195020A-x50 Sequence Editor Function.

Setup

Launch the MX190000A, in the Module and Boxes screen, select the **FPGA** and **Firmware** check boxes for MU195020A, and touch **Program** at the top right of the screen.

Note:

When you touch **Program** for the first time after MU195020A-x50 addition, the **FPGA** check box will remain selected even after the FPGA has been programmed. In this case, touch **Program** again. It takes about 20 minutes to complete programming the FPGA twice.

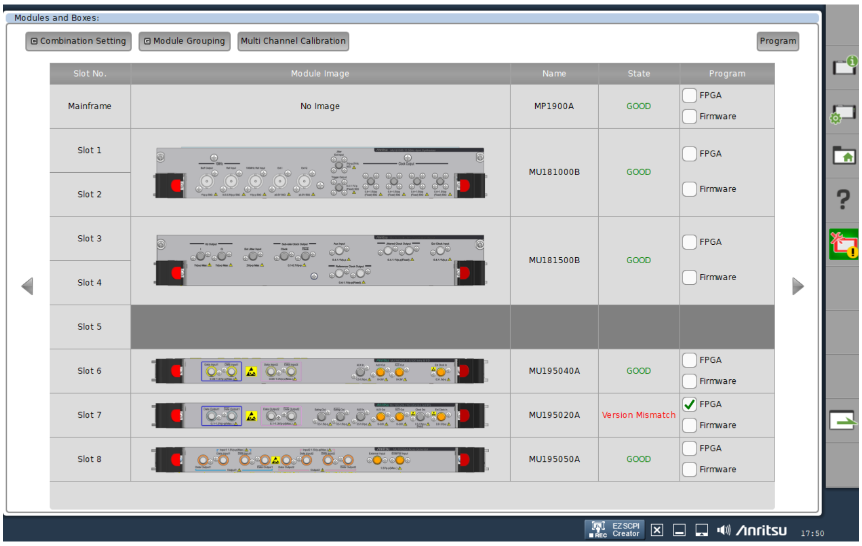


Figure 5.3.8-1 Module and Boxes Screen
(After Completion of 1st Time Program Processing)

When **Sequence** is selected in the Test Pattern box, set parameters as follows.

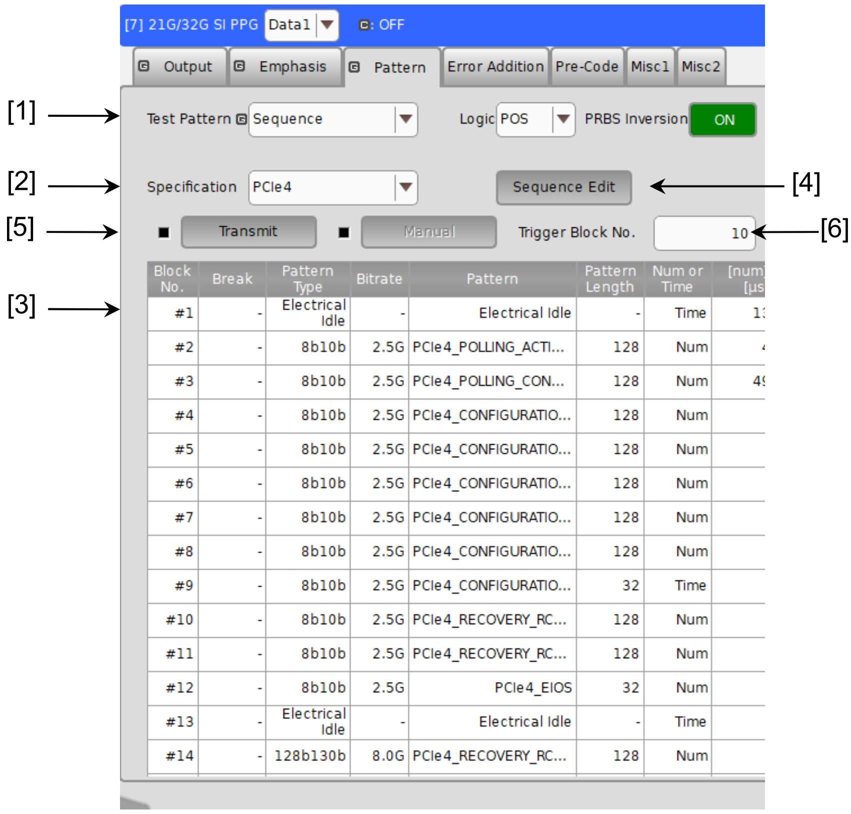


Figure 5.3.8-2 Parameters on the Pattern Tab (When Sequence is Selected)

[1] On the **Pattern** tab for MU195020A, select **Sequence** in the Test Pattern box.

[2] Select a test specification.

When on the **Misc2** tab, MU181000A/B and MU181500B are selected in the Clock Source box, the bitrate is set automatically.
When on the **Misc2** tab, **External** is selected in the Clock Source box, set the Clock Source frequency so that the bitrate becomes the value as specified in the selected specification. The Sequence Editor function cannot be used with bitrates other than the selected specification.

[3] Depending on the selected specification, the prepared sequence (hereinafter "the default sequence") is displayed. The default sequence describes a typical pattern for making the DUT enter the Loopback.Active state.

[4] Touch **Sequence Edit** to open the Sequence Editor.
In the Sequence Editor, set the block parameters.

[5] Touch **Transmit** to start outputting the sequence pattern.

[6] Set the block No. of the block to output a trigger signal from the AUX Output connector. In the AUX Output box of the **Misc1** tab, select **LTSSM Trigger**.

5.3.9 Editing test pattern in Sequence Editor dialog box

This section describes how to edit the test pattern when the following pattern is selected on the **Pattern** tab.

- Sequence

5.3.9.1 Common setting items

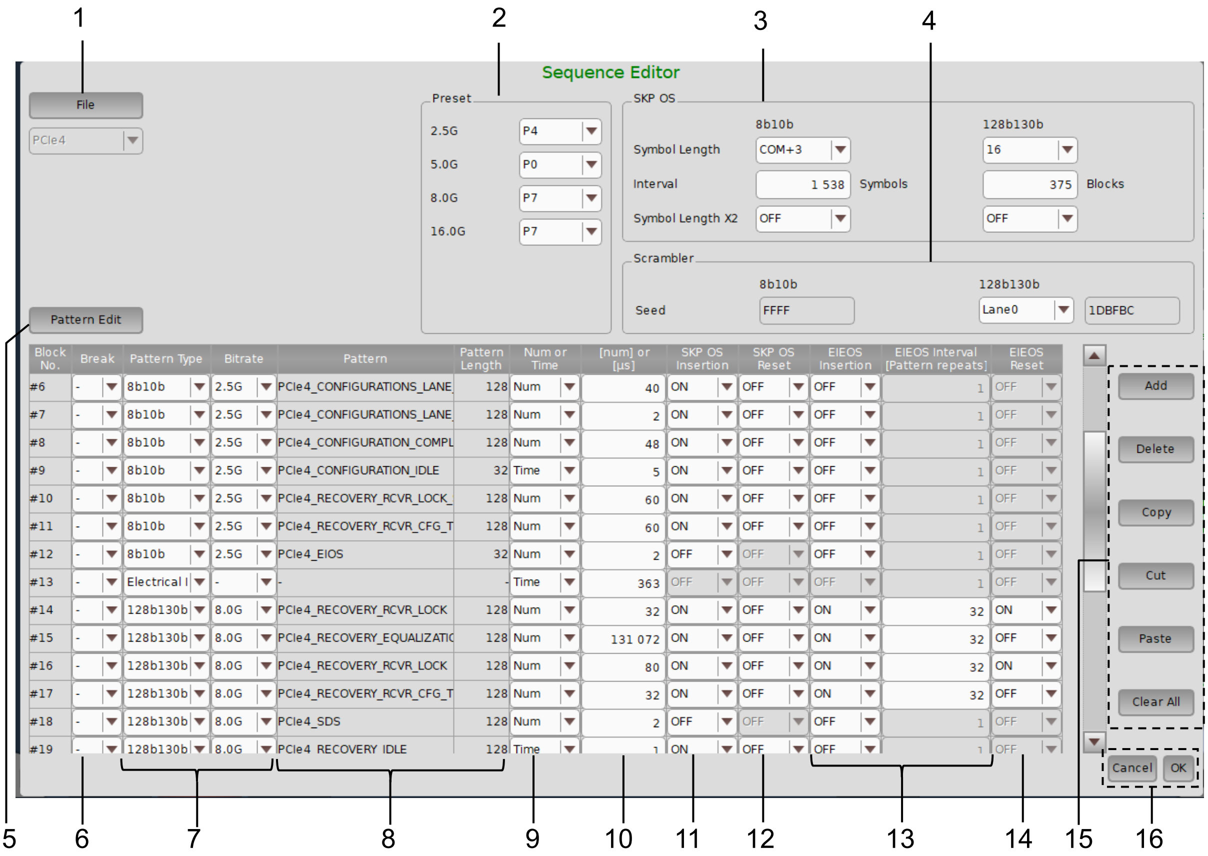


Figure 5.3.9.1-1 Sequence Editor Setting Items

Table 5.3.9.1-1 Sequence Editor Setting Items

No.	Item	Description
1	File	Saves all the editions, including the edited patterns, made in the Sequence Editor to a file. Touch **File** → **Save** to save to any directory.

Table 5.3.9.1-1 Sequence Editor Setting Items (Cont'd)

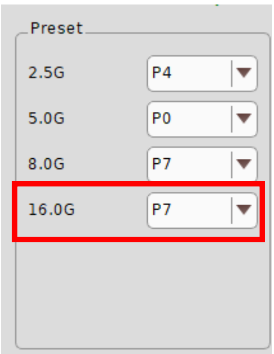
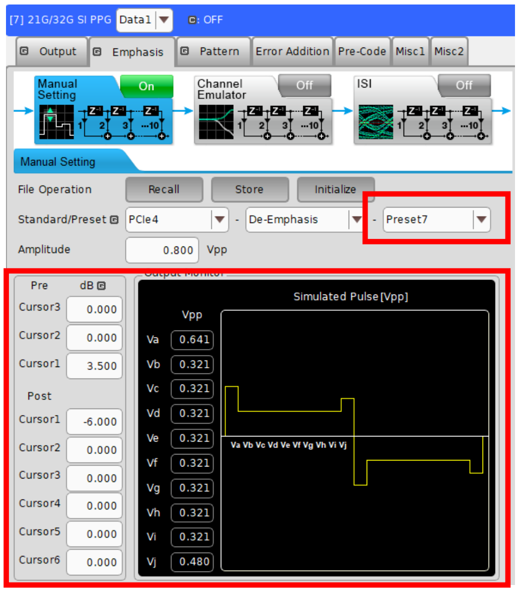
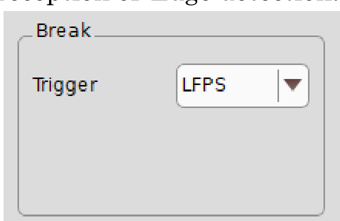
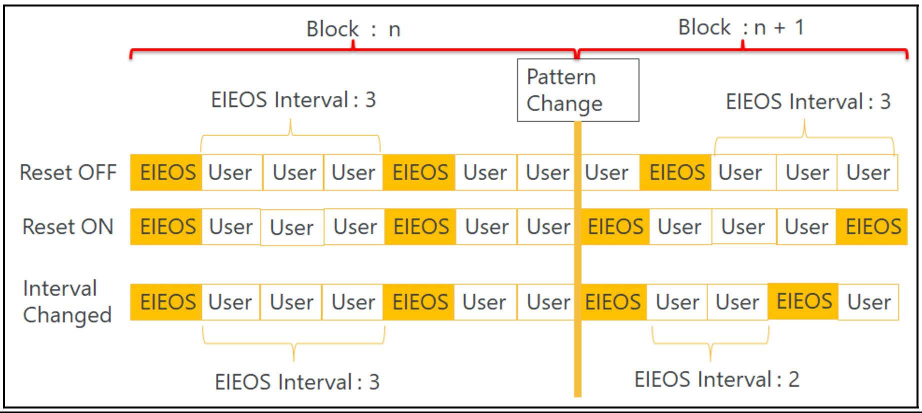
No.	Item	Description
2	Preset	Sets the Preset value of Emphasis used for each bitrate. P0 to P10 correspond to Preset0 to 10 on the **Emphasis** tab for MU195020A. In the following example, the emphasis set in Preset7 is used for outputting a 16G signal.  
3	SKP OS	Sets the conditions for SKP insertion interval and length for each encoding rule.
4	Scrambler	Displays the Scrambler seed value for each encoding rule. For 128b130b (PCIe3/4), the seed value varies by Lane. The generator polynomial for each encoding rule is shown below. • 8b10b (PCIe1, 2, USB3.0) $G(X) = X^{16} + X^{5} + X^{4} + X^{3} + 1$ • 128b130b (PCIe3, 4) / 128b132b (USB3.1 Gen2) $G(X) = X^{23} + X^{21} + X^{16} + X^{8} + X^{5} + X^{2} + 1$
5	Pattern Edit	Opens the **Pattern Editor** dialog box.
6	Break	Sets the conditions for suspending and resuming the pattern transition. When Break is set to Manual, the sequence transits from the block at which it paused to the next block if you touch **Manual** on the **Pattern** tab. When Break is set to External, the sequence transits from the block at which it paused to the next block upon detection of a trigger signal at the AUX Input connector of the MU195020A. When a USB standard is selected in the **Specification** box of the **Pattern** tab, you can select a trigger condition for External from LFPS signal reception or Edge detection. 

Table 5.3.9.1-1 Sequence Editor Setting Items (Cont'd)

No.	Item	Description
7	Pattern Type, Bitrate	To change the bitrate, insert Electrical Idle between blocks. (See Block No. 12 to 14 shown in Figure 5.3.9.1-1.) If Electrical Idle is not inserted between 2 consecutive Blocks, an unexpected pattern may be output when Bitrate is changed. Pattern Type can be set to **General** for the last block only. When **General** is selected, an available PRBS or Data pattern can be set.
8	Pattern / Pattern Length	By touching **Pattern Edit** with any block selected, the Pattern Editor displayed according to the pattern type. For details on how to use Pattern Editor, refer to 5.3.9.2 "Editing 8b10b Data pattern" through 5.3.9.4 "Editing 128b132b Data pattern".
9	Num or Time	Sets the repeated transmission mode of the selected block pattern to Num (number of repetitions) or Time (period of time).
10	[num] or [µs]	Sets the number or times or the period of time according to the setting made in the Num or Time box.
11	SKP OS Insertion	Inserts SKP OS into the pattern according to the Symbol Length and Interval settings under SKP OS at the top right of the Sequence Editor screen when set to **ON**.
12	SKP Reset	Inserts SKP OS at the beginning of the block after the block transition when set to **ON**.
13	EIEOS Insertion / Interval*	Inserts EIEOS into the pattern according to the EIEOS Interval setting when set to **ON**. Basically set to **ON** because EIEOS is required in pattern synchronization for 128b/130b.
14	EIEOS Reset	Inserts EIEOS at the beginning of the block after the block transition when set to **ON**. Even when set to **OFF**, if the EIEOS Interval differs among blocks, EIEOS is inserted at the beginning. 
15	Add, Delete, Copy, Cut, Paste, Clear All	Used for editing blocks.
16	OK, Cancel	**OK**: Sets the created sequence. **Cancel**: Discards the created sequence.

*: SYNCOS when USB3.1 Gen2 is selected.

5.3.9.2 Editing 8b10b Data pattern

Using the on-screen keypad at the right bottom or the keyboard, set a pattern per 8-bit symbol. Set patterns with K and D codes.

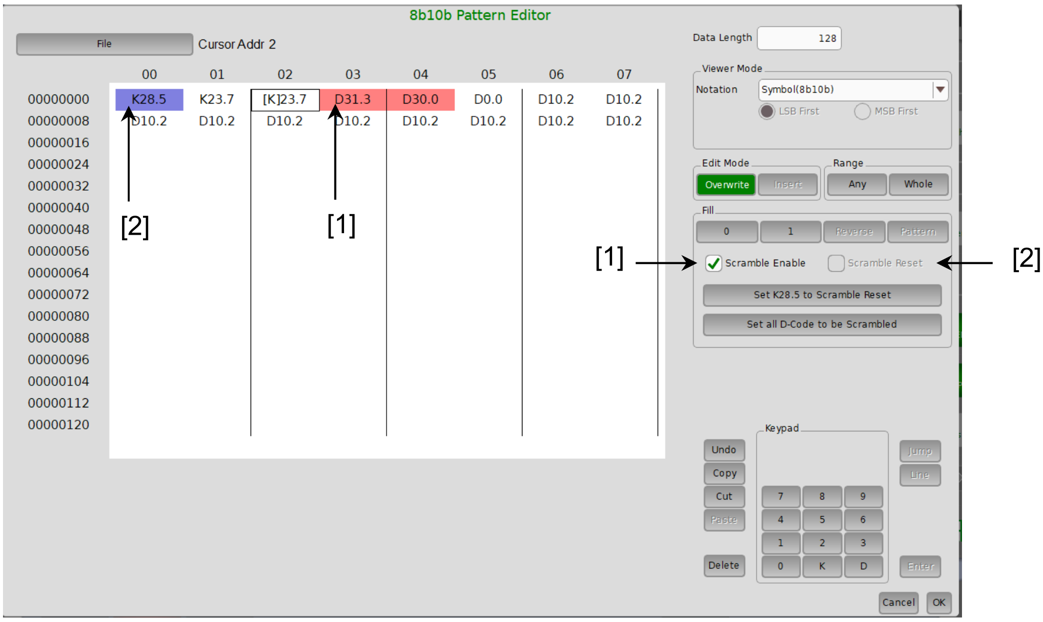


Figure 5.3.9.2-1 8b10b Pattern Editor

[1] To use a scrambler, select the **Scrambler Enable** check box, select (touch) at least one pattern symbol where to enable the scrambler, and touch **1** under **Fill**. The symbols displayed with red background are subject to scrambler. Scrambling is applied only to D codes.

[2] LFSR is initialized upon transmission of a symbol(s) with **Scrambler Reset** turned on. LFSR is also initialized when a COM symbol (K28.5) is sent. LFSR is initialized at the symbol displayed with blue background.

5.3.9.3 Editing 128b130b Data pattern

Set a pattern for each 128bit pattern + Sync Header.

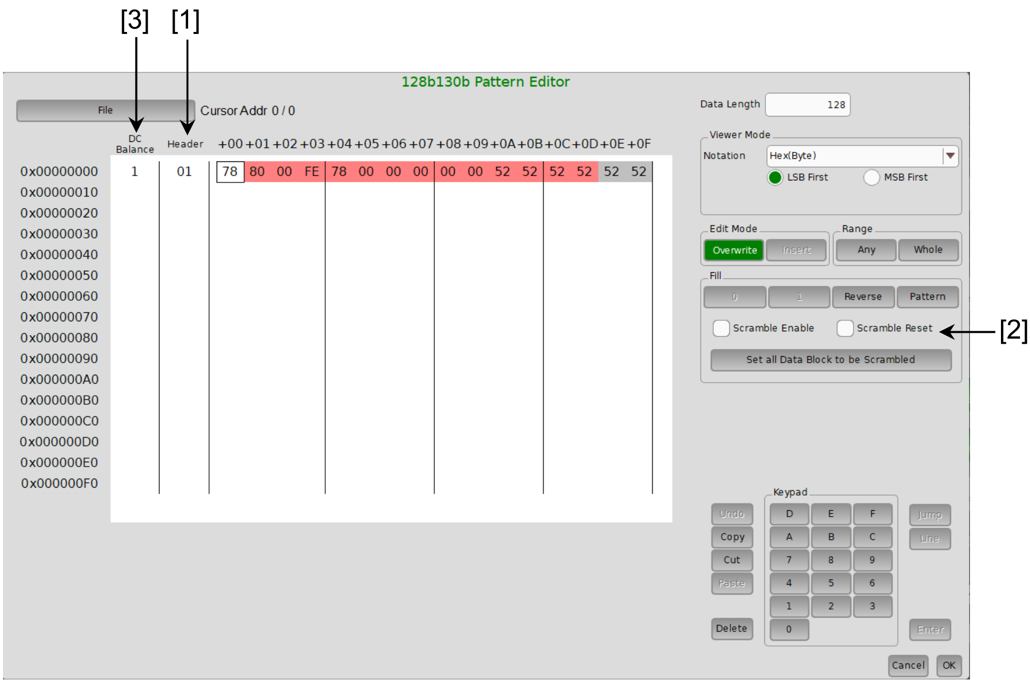


Figure 5.3.9.3-1 128b130b0 Pattern Editor

[1] Set Sync Header for each Data and Ordered Set as shown in the table below.

Table 5.3.9.3-1 Sync Headers for 128b130b Pattern Editor

	Sync Header	
	10	**01**
LSB First	Data	Ordered set
MSB First	Ordered set	Data

[2] Scrambler Enable and Scrambler Reset can be set in the same way as 8b10b.

[3] When DC Balance is set to 1, the transmission pattern of Symbol 14 and Symbol 15 is determined by the following rule.

Table 5.3.9.3-2 Rule on Determination of Transmission Pattern

DC Balance at the end of Symbol 11 of the TS Ordered Set	Transmission Pattern of Symbol 14 and Symbol 15
> 31	Transmit DFh for Symbol 14 and F7h for Symbol 15 to reduce the number of 0s, or 20h for Symbol 14 and 08h for Symbol 15 to reduce the number of 1s.
≤31 and >15	Transmit F7h for Symbol 15 to reduce the number of 0s, or 08h for Symbol 15 to reduce the number of 1s. Transmit the normal TS Identifier Symbol (scrambled) for Symbol 14.
≤15	Transmit the normal TS Identifier Symbol (scrambled) for Symbols 14 and 15.

5.3.9.4 Editing 128b132b Data pattern

Except that the number of Sync Header bits is 4, it is used in the same way as the 128b130b Pattern Editor in ii.

Set Sync Header for each Data and Ordered Set as shown in the table below.

Table 5.3.9.4-1 Sync Headers for 128b132b Pattern Editor

	Sync Header	
	1100	**0011**
LSB First	Ordered set	Data
MSB First	Data	Ordered set

5.4 Adding Errors

An error can be added to output data by configuring the error occurrence settings on the **Error Addition** tab of the MU195020A operation window.

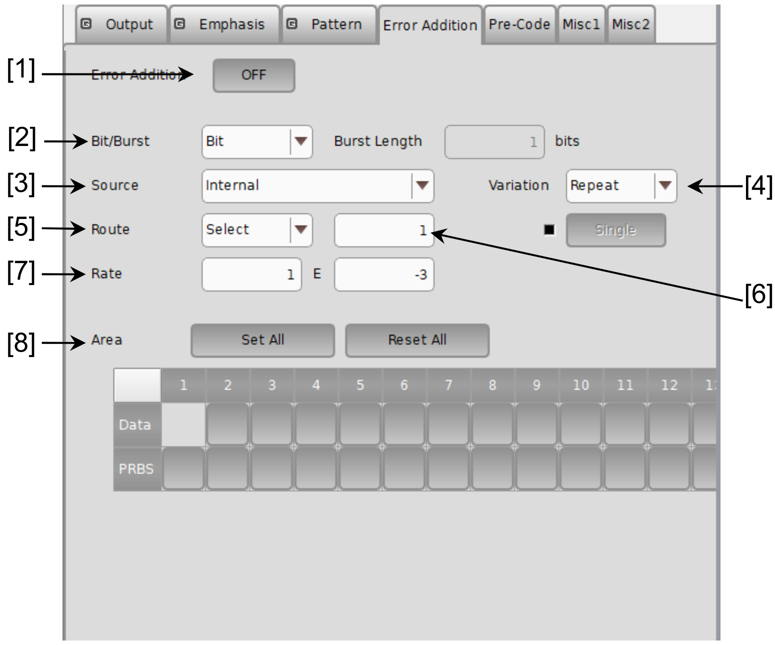


Figure 5.4-1 Error Addition tab

[1] Enables/disables generating a bit error for the test pattern.

ON: Enables the error addition function.
OFF: Disables the error addition function.

Note that this setting affects all error addition functions. When set to **OFF**, bit error addition triggered by an external error signal is also disabled.

[2] Select an error addition mode from **Bit** and **Burst**. When **Burst** is selected, up to 127 consecutive errors can be added.

5

Operation Method

[3] Selecting error adding source

Select the method for generating the timing to add a specified bit error to the test pattern.

This can be set when Error-Injection is set for AUX Input on the **Misc1** tab.

Table 5.4-1 Error addition source setting

Selection item	Description
Internal	The error addition timing is generated by the internal circuit.
External-Trigger	The error addition timing is generated in synchronization with the trigger edge of the external signal input from the Auxiliary Input connector.
External-Disable	The error addition timing is generated by the internal circuit, but an error is not added when the external signal input from the Auxiliary Input connector is low.

[4] When Internal or External-Disable for Source, error-addition variation can be selected. Select the error addition method when adding an error (internal Gating).

Table 5.4-2 Error Addition method setting

Selection item	Description
Repeat	An error is continuously added.
Single	An error is added once when the button is touched. In Combination function, errors as many as the number of Combined channels are added once when the button is touched.

[5] Select the method for adding an error addition route

MU195020A outputs test pattern synthesizing by multiplexer.

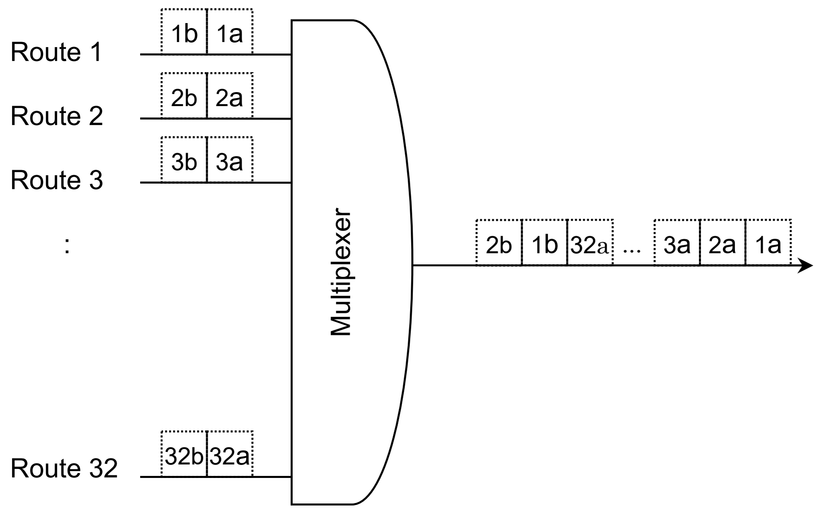


Figure 5.4-2 Parallel-Serial Conversion of Test Pattern

Input signal from the multiplexer is called “Route”. MU195020A has 32 routes.

Table 5.4-3 Error addition route setting

Selection item	Description
Scan	Changes a route to add an error by turns.
Select	An error is added to the specified route.

[6] Specify a route to generate a 1-bit error for the test pattern. The route can be specified from 1 to 32, in single steps.

Note that the following restrictions apply.

(a) E This setting is valid even when the error addition function is set to **OFF**.

(b) This setting is invalid when Scan is selected in the Route drop-down list.

[7] Select the bit error rate to generate a 1-bit error for the test pattern.

xE–n: x can be set to 1 to 9, in single steps.
n can be set to 3 to 12, in single steps.

Note that the following restrictions apply.

(a) The setting is valid even when the error addition function is set to **OFF**.

(b) This setting is invalid when the error addition variation setting is set to Single.

(c) This setting is invalid when the error addition source is set to External-Trigger.

(d) x can be set to 1 to 5 when n is set to 3.

(e) Maximum insertion bit rate is 5E–3.

[8] For the Mixed pattern, select the block (Data, PRBS and Block No.) where a bit error is to be added.

5.5 Setting Pre-Code Function

Pre-Code function can be set when Combination in 5.8 “Multi-channel Function” is selected for the MU195020A-x20.

Since this function supports DQPSK, it can calculate and output Data as shown in the following Pre-Code logic diagram.

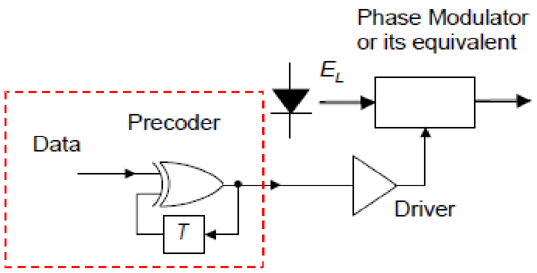


Figure 5.5-1 Pre-Code Logic (DQPSK) Diagram

To set the Pre-Code function, touch the **Pre-Code** tab of the MU195020A application.

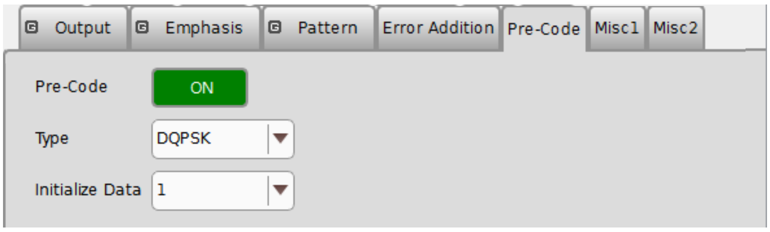


Figure 5.5-2 Pre-Code tab

Note:

Pre-Code Settings are common to all channels where Combination function is set.

5.5.1 Pre-Code setting

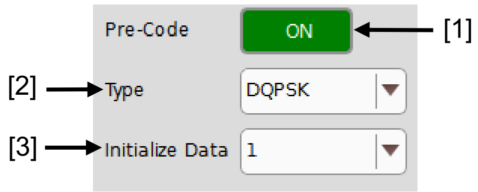


Figure 5.5.1-1 Pre-Code Setting Area

Table 5.5.1-1 Pre-Code Setting item

No.	Item	Function
[1]	Pre-Code	Sets Pre-Code ON and OFF
[2]	Type	Sets Pre-Code modulation method When 2ch Combination selected: DQPSK
[3]	Initialize Data	Sets Pre-Code to default values (Default: 1)

5.6 Misc1 Function (MU195020A)

The settings of the signal generating method, synchronized output, and auxiliary input/output can be configured.
Touch the **Misc1** tab of the MU195020A operation window to configure the Misc function.

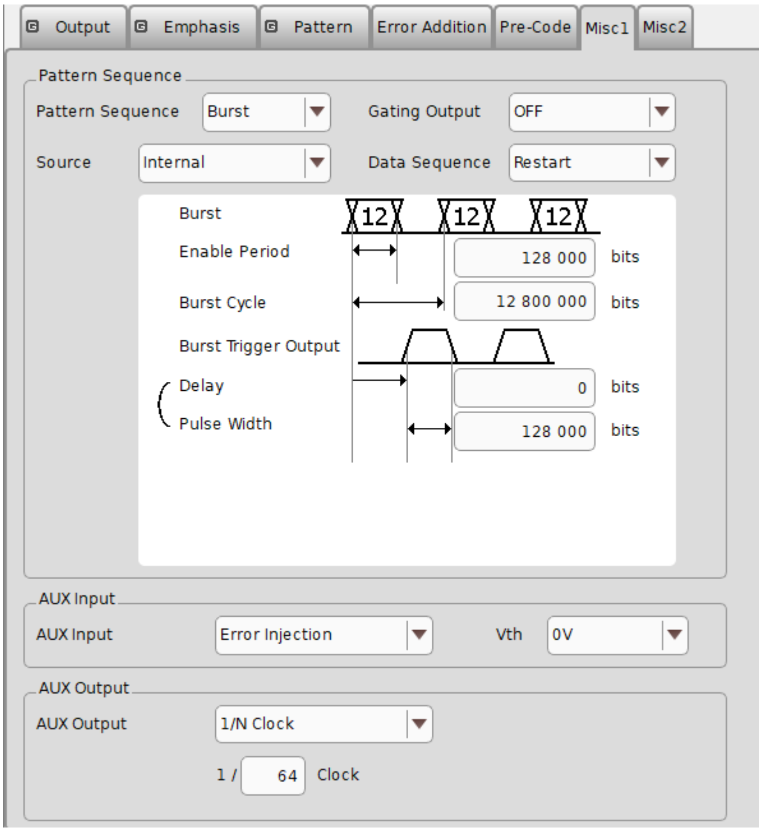


Figure 5.6-1 Misc1 tab

Table 5.6-1 Setting items

Setting area	Description
Pattern Sequence	Set the test pattern generating method.
AUX Input	Configure the settings for the auxiliary input function.
AUX Output	Configure the settings for the auxiliary output function.
Gating Output	Set the timing signal output.

Settings on the **Misc1** tab are common to Data 1 to Data 2 of MU195020A.
Settings related to the pattern length depend on the Data1 settings.

5.6.1 Setting pattern sequence

Select the signal generating method.

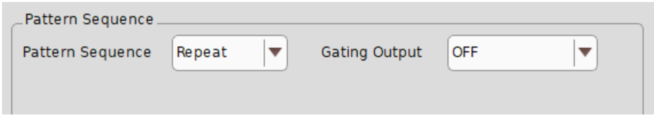


Figure 5.6.1-1 Selecting pattern sequence

Table 5.6.1-1 Pattern sequence setting

Selection item	Description
Repeat	Select when transmitting the test pattern Repeat data. Mainly used for electric device evaluation.
Burst	Select when transmitting the test pattern Burst data. Mainly used for long-distance optical transmission tests such as an optical circulating loop test, and packet communications evaluation. The target test patterns are PRBS, ZeroSubstitution, Data, and Mixed (Data).

5.6.1.1 Setting Repeat pattern

Select **Repeat** from the Pattern Sequence drop-down list to transmit the test pattern Repeat data.

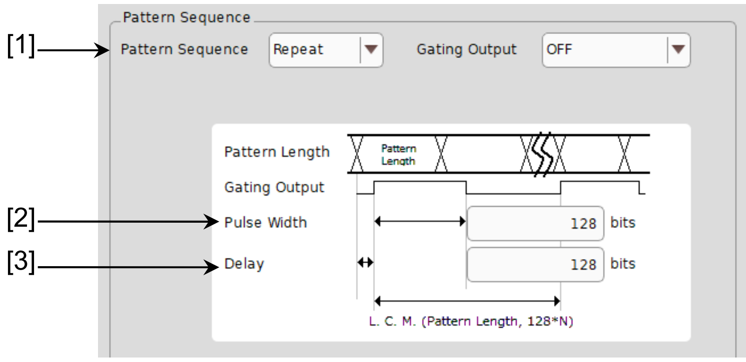


Figure 5.6.1.1-1 Setting items for Repeat pattern sequence

[1] Select **Repeat** from the Pattern Sequence drop-down list, and generate continuous test patterns and data signals.

[2] In the Pulse Width textbox, specify the high level pulse width of the synchronization signal that is output from the Gating Out connector on the MU195020A front panel. The pulse width should be a multiple of 8. The Pulse Width value can be calculated by the expression in Table 5.6.1.1-1.

Table 5.6.1.1-1 Pulse width setting range

Periodic Signal	Setting Range
PRBS, Data, ZeroSubstitution	128 to (Least common multiple of Pattern length and 128) – 128* (The maximum settable number is 34 359 738 240) Setting step: 8 bit In the case of 2ch Combination (the target test patterns are PRBS, Data, and ZeroSubstitution) is 256 to (Least common multiple of Pattern Length and 256) – 256 and the setting step becomes 16 bits. (The maximum settable number is 68 719 476 480)
Mixed	128 to (Row length × Number of Rows × Block count) – 128 (The maximum settable number is 2 415 918 976) Setting step: 8 bit In the case of 2ch Combination is 256 to (Row length × Number of rows × Block count) – 256, and the setting step becomes 16 bits.

*: The pattern length described here is the number multiplied by an integer so that it becomes 512 bits or more, when the length on the Figure 5.3-1 Pattern tab is 511 bit or less.

At 2ch Combination, the pattern length described here is the number multiplied by an integer so that it becomes 1024 or more, when the length on the Figure 5.3-1 Pattern tab is 1023 or less.

[3] In the Delay textbox, specify the number of bits the high level pulse output is delayed from the beginning of the data pattern.
The delay should be a multiple of 8 and is calculated by the expression in Table 5.6.1.1-2.

Table 5.6.1.1-2 Delay setting range

Periodic Signal	Setting Range
PRBS, Data, ZeroSubstitution	128 to (Least common multiple of Pattern length and 128) – 128* (The maximum settable number is 34 359 738 240) Setting step: 8 bit In the case of 2ch Combination (the target test patterns are PRBS, Data, and ZeroSubstitution), is 256 to (Least common multiple of Pattern Length and 256) –256 and the setting step becomes 16 bits. (The maximum settable number is 68 719 476 480)
Mixed	128 to (Row length × Number of Rows × Block count) –128 (The maximum settable number is 2 415 918 976) Setting step: 8 bit In the case of 2ch Combination is 256 to (Row length × Number of rows × Block count) –256, and the setting step becomes 16 bits.

*: The pattern length described here is the number multiplied by an integer so that it becomes 512 bits or more, when the length on the Figure 5.3-1 Pattern tab is 511 bit or less.

At 2ch Combination, the pattern length described here is the number multiplied by an integer so that it becomes 1024 or more, when the length on the Figure 5.3-1 Pattern tab is 1023 or less.

5.6.1.2 Setting Burst pattern

Select **Burst** from the Pattern Sequence drop-down list to transmit the test pattern Burst data.

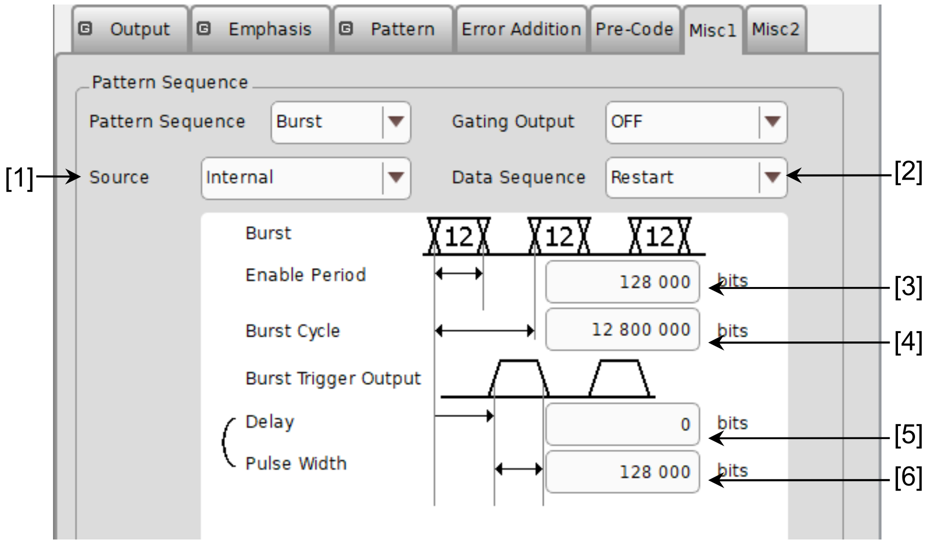


Figure 5.6.1.2-1 Setting items for Burst pattern sequence

Note:

The Burst Trigger Output signal is output from the Gating Out connector.

[1] Select the timing to generate test patterns with the Burst signal.

Table 5.6.1.2-1 Burst setting items

Selection item	Description
Internal	The Burst signal occurrence timing is generated by the internal circuit.
External-Trigger	The Burst signal occurrence period is generated based on the gate signal input from the AUX In connector. Burst pattern generation starts at the rising edge of the input gate signal.
External-Enable	The Burst signal occurrence period is generated based on the gate signal input from the AUX In connector. The Burst data is generated when the gate signal is high, and is not generated when the gate signal is low.

[2] Specify the burst pattern generating sequence.

Table 5.6.1.2-2 Burst pattern generation sequence setting

Selection item	Description
Restart	The specified test pattern is restarted from the beginning each time a Burst data signal occurs.
Consecutive	The specified test pattern is continuously output between Burst data signals.
Continuous	The specified test pattern is continuously output, and outputs other than the Burst occurrence timing are masked.

[3] When **External-Trigger** or **Internal** is selected from the Source drop-down list, set the continuous signal generation period for the Burst cycle of the test pattern to be input to the AUX Input connector, by entering the number of bits in the **Enabled Period** box.

The setting ranges for Enable Period are shown in Table 5.6.1.2-3.

[4] When **Internal** is selected from the Source drop-down list, set the Burst cycle (one cycle of the Burst signal of the test pattern to be input) by entering the number of bits in the **Burst Cycle** box.

The setting ranges for Burst Cycle are shown in Table 5.6.1.2-3.

Table 5.6.1.2-3 Setting ranges for Enable Periods and Burst Cycles

No. of Channel Combinations	Enable Period (bit)	Burst Cycle (bit)	Setting Steps (bit)
1	When **Internal** is set: 12 800 to 2 147 483 392	25 600 to 2 147 483 648	256
	When **External-Trigger** is set: 12 800 to 2147 483 648		
2	When **Internal** is set: 25 600 to 4294 966 784	51 200 to 4 294 966 296	512
	When **External-Trigger** is set: 25 600 to 4294 967 296		

Note:

A Disable period of at least 512 bits is required between Burst Cycle and Enable Period.
The Disable period is doubled at 2ch Combination.

[5], [6]

Set the Burst timing signal that is output from the Burst Trigger Output connector.

Delay: Specify how many bits the data output is delayed from the beginning of the Burst data pattern.

Pulse Width: Specify the high level pulse width of the synchronization signal that is output from the Burst Trigger Output connector.

The setting ranges for Delay and Pulse Width are shown in Table 5.6.1.2-4.

Table 5.6.1.2-4 Setting ranges for Delay and Pulse Width

No. of Channel Combinations	Delay (bit)	Pulse Width (bit)	Setting Steps (bits)
1	0 to (Burst cycle – 128)	0 to (Burst cycle – 128)	8
2	0 to (Burst cycle – 256)	0 to (Burst cycle – 256)	16

5.6.2 Setting AUX Input

Use the AUX Input connector when adding an error based on the externally-generated timing signal.
The following table shows the functions that use AUX Input connector.

Figure 5.6.2-1 Setting item for AUX Input

Table 5.6.2-1 Setting items

Selection item	Description
Error Injection	Select when adding an error based on the timing of an external signal. This is used when **External-Trigger** or **External-Disable** is selected from the Source drop-down list on the **Error Addition** tab (refer to 5.4 “Adding Errors” for details).
Burst	Select when Burst is selected from the Pattern Sequence drop-down list, and **External-Trigger** or **External Enable** is selected from the Source drop-down list. Refer to 5.6.1.2 “Setting Burst pattern” for details.
Vth	Select input threshold from 0V, –0.25V, or –0.5V.

5.6.3 Setting AUX Output

The output settings of auxiliary signals, such as the synchronization signal, can be configured.

5.6.3.1 Setting 1/N Clock

When **1/N Clock** is selected from the AUX Output drop-down list, a clock can be output from the AUX Output connector in synchronization with the test pattern.

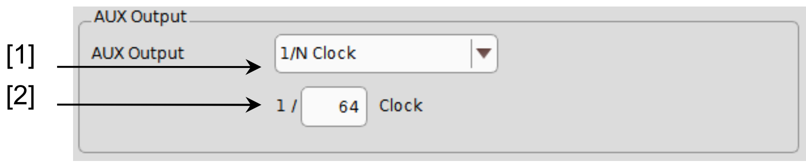


Figure 5.6.3.1-1 Setting items for AUX Output Clock

[1] When **1/N Clock** is selected from the AUX Output drop-down list, a clock can be output from the AUX Output connector in synchronization with the test pattern.

[2] The frequency dividing ratio for the synchronization clock (N) can be set.
The setting range for the setting frequency is 4 to 512, stepping 2.

5.6.3.2 Setting Pattern Sync

When **Pattern Sync** is selected from the AUX Output drop-down list, a timing signal can be generated in synchronization with the test pattern period.

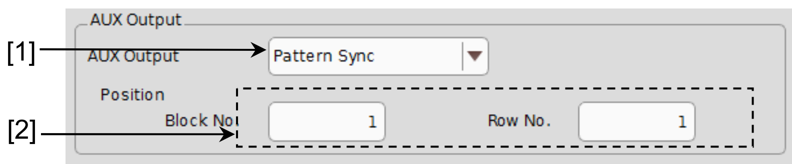


Figure 5.6.3.2-1 Setting items for AUX Output Pattern Sync (Mixed)

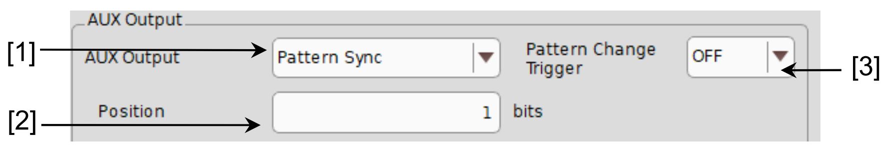


Figure 5.6.3.2-2 Setting for AUX Output Pattern Sync (Other Than Mixed)

[1] When **Pattern Sync** is selected from the AUX Output drop-down list, a pulse signal can be output from the AUX Output connector in synchronization with the set data pattern period.

[2] The synchronization signal pulse generation position can be set. The setting method varies depending on the test pattern.

[3] When **ON** is selected, a trigger signal is output from the AUX Output connector at test-pattern changeover.

Table 5.6.3.2-1 Synchronization signal pulse generation position setting

Test pattern	Description
PRBS, Data, ZeroSubstitution	A signal pulse is generated in a pattern period. The pulse position can be specified within the range below, starting from the beginning of the pattern. 1 to {(Least common multiple of Pattern Length* and 128)–135}, in 8-bit steps. The maximum settable number is 34 359 738 105 In the case of 2ch Combination: 1 to {(Least common multiple of Pattern Length* and 256) –287}, in 16-bit steps. The maximum settable number is 68 719 476 209
Mixed (Data)	A signal pulse is generated during the entire block generation pattern period. The pulse position can be specified by the positions of Block and Row.

*: The pattern length described here is the number multiplied by an integer so that it becomes 512 bits or more, when the length on the Figure 5.3-1 Pattern tab is 511 bit or less.

At 2ch Combination, the pattern length described here is the number multiplied by an integer so that it becomes 1024 or more, when the length on the Figure 5.3-1 Pattern tab is 1023 or less.

5.6.3.3 Setting Pattern Burst Output2

When **Burst** is selected from the Pattern Sequence drop-down list, a timing signal similar to the Burst Trigger Output signal can be outputted from the AUX Output connector.

Table 5.6.3.3-1 Burst Output2 setting

Setting item	Description
Delay	Specify how many bits the data output is delayed from the beginning of the Burst data pattern. The setting range is similar to Table 5.6.1.2-4 Setting ranges for Delay and Pulse Width.
Pulse Width	Specify the high level pulse width of the synchronization signal that is output from the Burst Trigger Output connector. The setting range is similar to Table 5.6.1.2-4 Setting ranges for Delay and Pulse Width.

5.6.3.4 Setting output to Off

When set to OFF, the AUX Output connector does not output signals.

5.6.4 Setting Gating Output

Set the output from the Gating Output connector to On or Off.

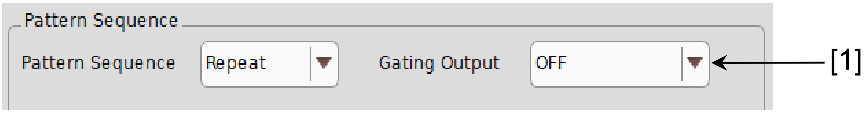


Figure 5.6.4-1 Gating Output Setting

Table 5.6.4-1 Gating Output Setting

Selection item	Description
ON	The Gating Output connector outputs synchronization signals set by pattern sequence.
OFF	The Gating Output connector does not output signals.

5.7 Misc2 Function

On the **Misc 2** tab, you can perform the Clock Setting and Combination Setting of multiple channels.

To set up Misc2, touch the **Misc2** tab on the MU195020A operation screen.

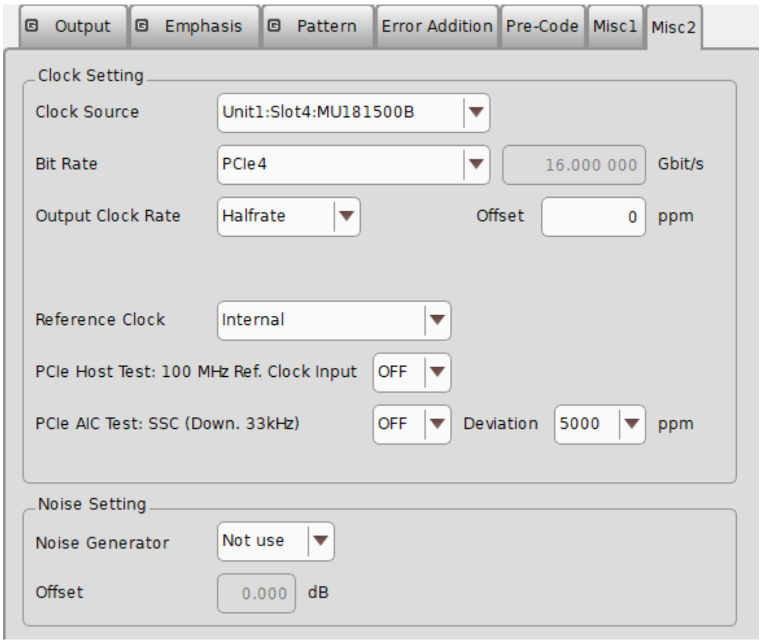


Figure 5.7-1 Misc2 tab

5.7.1 Setting Clock

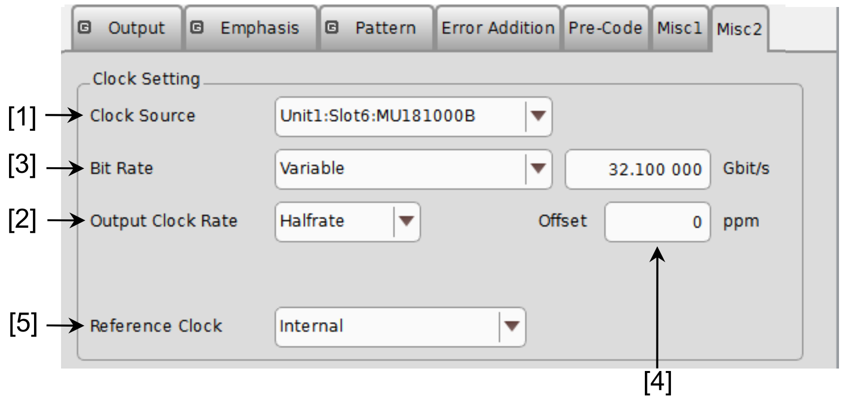


Figure 5.7.1-1 Setting items for Clock setting (when MU181000B is selected)

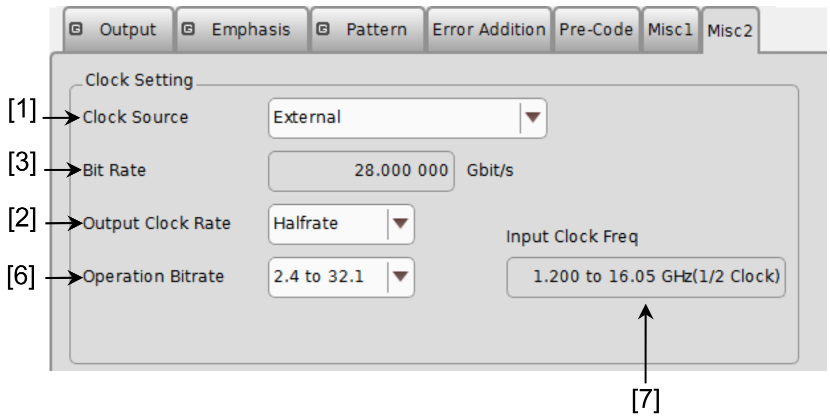


Figure 5.7.1-2 Setting items for Clock setting (when External is selected)

[1] Clock source can be selected from the drop-down list

Table 5.7.1-1 Clock Source setting items

Selection item	Description
External	The clock input into Ext Clock Input connector of MU195020A.
MU181000A	The clock of an MU181000A that is installed in MP1900A.
MU181000B	The clock of an MU181000B that is installed in MP1900A.
MU181500B	The clock of an MU181500B that is installed in MP1900A.

[2] Set the clock rate to be output to the Clock Out connector.

Fullrate: Clock frequency is same as output data rate.

Halfrate: Clock frequency is half of output data rate.

When Clock Source is MU181000A/B

[3] Set the output bit rate. Select **Variable** or a preset standard value. For details, refer to 5.1.4 “Setting bit rate”.

[4] Set the frequency offset of the synthesizer module within the range from –1000 to 1000 ppm.

Offset is not displayed when Clock source is **External**.

[5] Set the reference clock of MU181000A/B.

When Clock Source is External

[3] Bit rate of output data is displayed.

[6] Output clock frequency range of MU195020A is displayed.

[7] Frequency of clock input to Input connector of MU195020A is displayed.

If “MU181500B” is selected in the Clock Source drop-down list [1], the frequency of the clock input to the MU181500B is displayed. The relationship between operation bitrate and input clock frequency that vary depending on the options selected in the list boxes [2] and [6] is shown below. The values enclosed in parentheses apply when the 32G bit/s Extension MU195020A-x01 is not installed.

Table 5.7.1-2 Relationship Between Operation Bitrate and Input Clock Frequency (When Using External Clock)

Output Clock Rate setting	Operation Bitrate setting (Range)	Input Clock Freq value (Display)	Relationship Between Bitrate and Clock Frequency
Full Rate Clock	2.4 to 16.0 Gbit/s	2.4 to 16.0 GHz	Operate at 1/1 clock
	16.0 to 20.0 Gbit/s	8.0 to 10.0 GHz	Operate at 1/2 clock
	20.0 to 32.1 (21.0) Gbit/s	10.0 to 16.05 (10.5) GHz	Operate at 1/2 clock
	25.0 to 32.1 Gbit/s	6.25 to 8.025 GHz	Operate at 1/4 clock
Half Rate Clock	2.4 to 32.1 (21.0) Gbit/s	1.2 to 16.05 (10.5) GHz	Operate at 1/2 clock
	25.0 to 32.1 Gbit/s	6.25 to 8.025 GHz	Operate at 1/4 clock

Table 5.7.1-3 Relationship Between Operation Bitrate and Input Clock Frequency (When Using MU181500B and External Clock)

Output Clock Rate setting	Operation Bitrate setting (Range)	Input Clock Freq value (Display)	Relationship Between Bitrate and Clock Frequency
Full Rate Clock	2.4 to 15.0 Gbit/s	2.4 to 15.0 GHz	Operate at 1/1 clock
	15.0 to 20.0 Gbit/s	7.5 to 10.0 GHz	Operate at 1/2 clock
	20.0 to 30.0 (21.0) Gbit/s	10.0 to 15.0 (10.5) GHz	Operate at 1/2 clock
	25.0 to 32.1 Gbit/s	6.25 to 8.025 GHz	Operate at 1/4 clock
Half Rate Clock	2.4 to 30.0 (21.0) Gbit/s	1.2 to 15.0 (10.5) GHz	Operate at 1/2 clock
	30.0 to 32.1 Gbit/s	7.5 to 8.025 GHz	Operate at 1/4 clock

Clock connection and screen settings

Depending on the used clock source, change both clock connection with MU195020A and settings in the screen. The procedure for connecting MU195020A, clock source, and jitter source and setting the screen items that varies by used clock source is described below.

Note:

Install the MU181000A/B synthesizer and/or the MU181500B Jitter Modulation Source to the MP1900A to which MU195020A is installed when the modules are included in the following configuration.

Connection and setting of MU195020A used by the following configurations are described.

(1) MU195020A, MU181000A/B, and MU181500B

(2) MU195020A and MU181000A/B

(3) MU195020A, MU181500B, and external clock source

(4) MU195020A and external clock source

Description is given according to the following configuration of MP1900A:

- MU181500B is installed to Slot1-2.
- MU195020A is installed to Slot3.
- MU181000B is installed to Slot6-7.

In addition, the procedure is described from the state that the clock source setting for each MU195020A and MU181500B is External (Default).

5.7.1.1 MU195020A, MU181000A/B synthesizer, and MU181500B Jitter Modulation Source

Connecting to the clock

For connecting the MU195020A, MU181000A/B, and MU181500B to the clock, refer to the connection diagram and description in 3.2.3 "Adding Jitter to Output Signal".

Setting in the screen

1. Select **Unit1:Slot6: MU181000B** from the Synthesizer Clock Source drop-down list in the MU181500B screen to make MU181500B and MU181000B track each other. (Refer to Figure 5.7.1.1-1.)
2. Select **Unit1:Slot2: MU181500B** from the Clock Source drop-down list in the MU195020A screen to make MU195020A and MU181500B track each other. (Refer to Figure 5.7.1.1-2.)
3. Now, you can set the bit rate of the output data to the Bit Rate box in the MU195020A screen. Figure 5.7.1.1-2 shows an example when the output data is set to 32.1 Gbit/s.

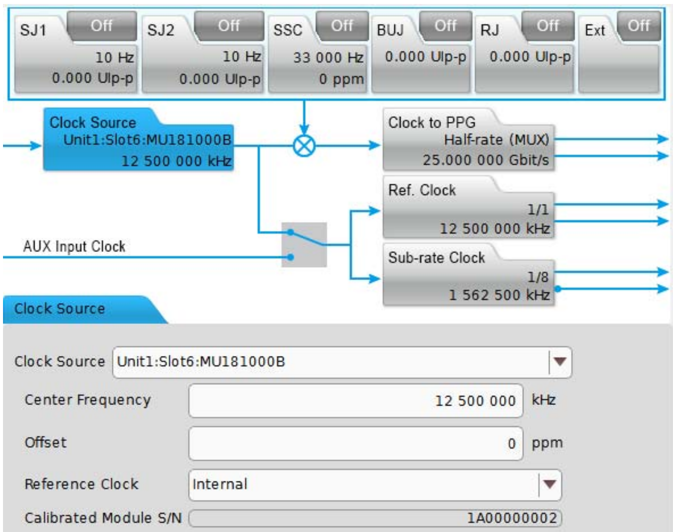


Figure 5.7.1.1-1 MU181500B Clock Source Settings

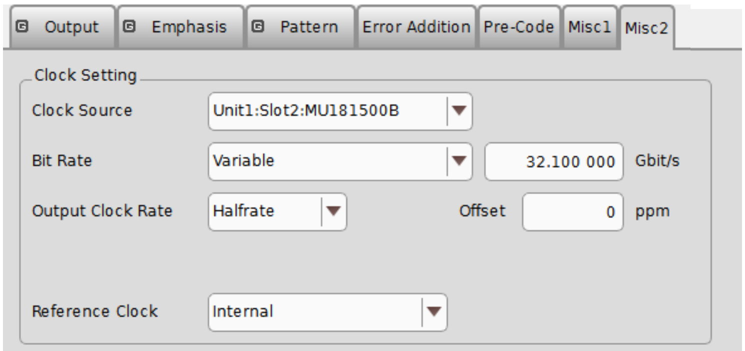


Figure 5.7.1.1-2 Clock Source Settings (When Tracking Operation of Jitter and Synthesizer)

Note:

Follow the above-mentioned procedure and set to make MU181500B and MU181000B track each other. If the steps are performed in the wrong order, a **Warning** dialog box appears as shown in Figure 5.7.1.1-3.

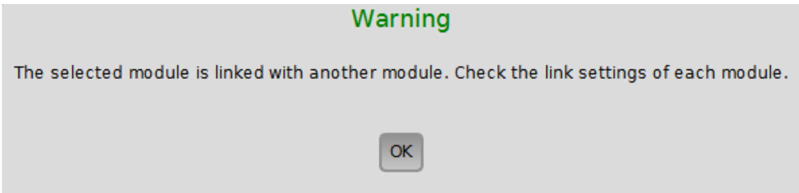


Figure 5.7.1.1-3 Warning Dialog Box for Module-Tracking Operation

5.7.1.2 MU195020A and MU181000A/B synthesizer

Connecting to the clock

For the clock connection between the MU195020A and MU181000A/B, refer to the connection diagram and description in 3.2.1 “Measuring Errors”.

Setting in the screen

1. Select **Unit1:Slot6: MU181000B** from the Clock Source drop-down list in the MU195020A screen to make MU195020A and MU181000B track each other.
2. Now, you can set the bit rate of the output data to the Bit Rate box in the MU195020A screen. Figure 5.7.1.2-1 shows an example when the output data is set to 32.1 Gbit/s.

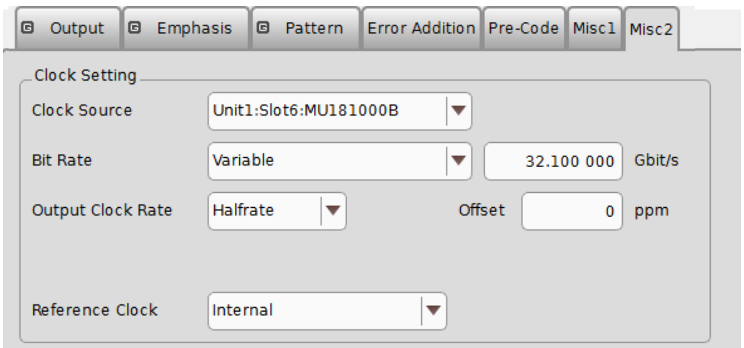


Figure 5.7.1.2-1 Clock Source Settings (When Tracking with Synthesizer)

5.7.1.3 MU195020A, MU181500B Jitter Modulation Source, and external clock source

Connecting to the clock

For connecting MU195020A and MU181500B to the external clock, refer to the connection diagram and description in 3.2.3 "Adding Jitter to Output Signal", replacing MU181000A with "external clock source".

Setting in the screen

1. Select **Unit1:Slot2: MU181500B** from the Clock Source drop-down list in the MU195020A screen to make MU195020A and MU181500B track each other.
2. In the MU195020A screen, select a bit rate of data to output from the Operation Bitrate drop-down list. To output 28 Gbit/s data, select **2.4 to 30.0** as shown in the example of Figure 5.7.1.3-1.
3. To the Ext Clock Input connector of the MU181500B, input the clock of the frequency displayed in the Input Clock Freq box in the MU195020A screen. In the example in Figure 5.7.1.3-1, 14 GHz clock is input to output 28 Gbit/s data.
4. The Bit Rate box in the MU195020A screen displays the bit rate of the output data. Check that the clock that is input in step 3 can change the bit rate of the output data.

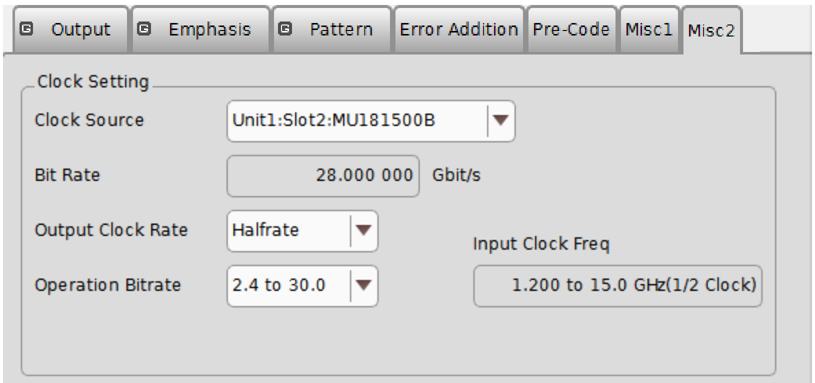


Figure 5.7.1.3-1 Clock Source Settings (When Using Jitter and External Clock Source)

5.7.1.4 MU195020A and external clock source

Connecting to the clock

For connecting MU195020A to the clock, refer to 3.2.1 "Measuring Errors" replacing MU181000A in the explanation by external clock source.

Setting in the screen

1. In the MU195020A screen, select **External** from the Clock Source drop-down list.
2. In the MU195020A screen, select a bit rate band of data to output from the Operation Bitrate drop-down list. In the example in Figure 5.7.1.4-1, select **2.4 to 32.1** to output 28 Gbit/s data.
3. To the Ext Clock Input connector of the MU195020A, input the clock of the frequency displayed in the Input Clock Freq box in the MU195020A screen. In the example in Figure 5.7.1.4-1, 14 GHz clock is input to output 28 Gbit/s data.
4. The Bit Rate box in the MU195020A screen displays the bit rate of the output data. Check that the clock that is input in step 3 can change the bit rate of the output data.

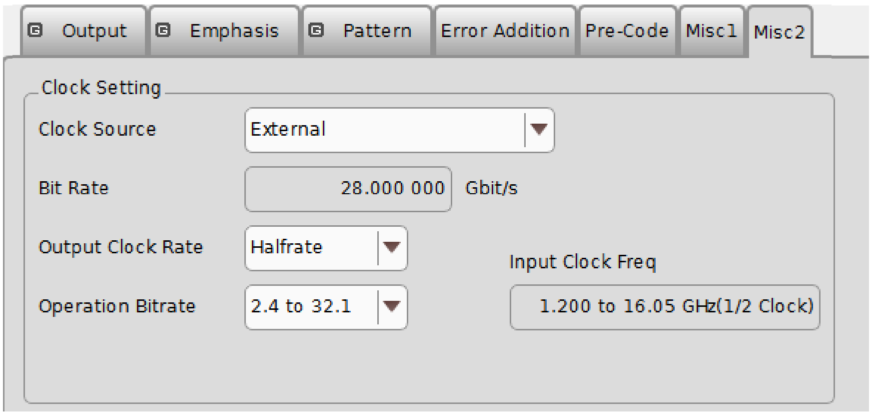


Figure 5.7.1.4-1 Clock Source Settings (When Using External Clock Source)

5.7.2 Setting Noise

Set whether to use the MU195050A or not.

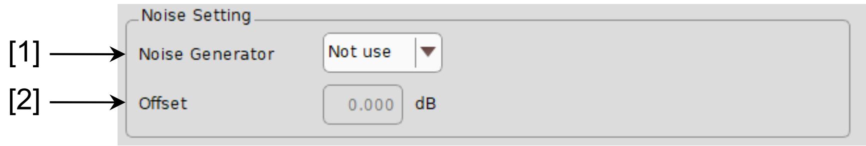


Figure 5.7.2-1 Noise Setting Items

[1] Sets whether to use the Noise Generator or not.

Table 5.7.2-1 Noise Generator Setting

Selection item	Description
Not Use	Does not use the Noise Generator.
Use	Uses the Noise Generator. The amplitude value on the Output and Emphasis tabs is calculated using the attenuation by the Noise Generator.

[2] Sets the offest value.

5.8 Multi-channel Function

The MU 195020A has a Multi-Channel function that generates data by combining data of multiple channels. The Multi Channel function can be categorized into Combination and Channel Synchronization. Available functions vary depending on model and its option.

For details of setting Multi Channel, refer to the *MX190000A Signal Quality Analyzer-R Control Software Operation Manual*.

Combination Function Types

(1) 2ch Combination: MU195020A-x20

(2) 64G × 2ch Combination: MU195020A-x20 × 2 modules

Channel Synchronization Function Types

(1) CH Synchronization: MU195020A-x20

(2) 2ch CH Synchronization: MU195020A-x20

(3) Inter modules CH Synchronization: MU195020A

Table 5.8-1 Multi-channel functions that the respective models support

Model/Option	2ch Combination	Ch Synchronization	Inter-module Ch Synchronization	64G × 2ch Combination
MU195020A	One module or more	One module or more	Two modules or more	Two modules or more
MU195020A-x10	–	–	–	–
MU195020A-x20	✓	✓	✓	✓
MU195020A-x30/x31	-x31	-x31	✓	-x31

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5.8.1 Combination Function

The Combination function enables MU195020A or MU195040A to evaluate the 40 Gbit/s and 50 Gbit/s applications by synchronizing pattern generations or receptions between the channels.

By combining two channels of 20 Gbit/s data, 40 Gbit/s serial data that is bit rate of 40GbE or OTU3 can be generated.

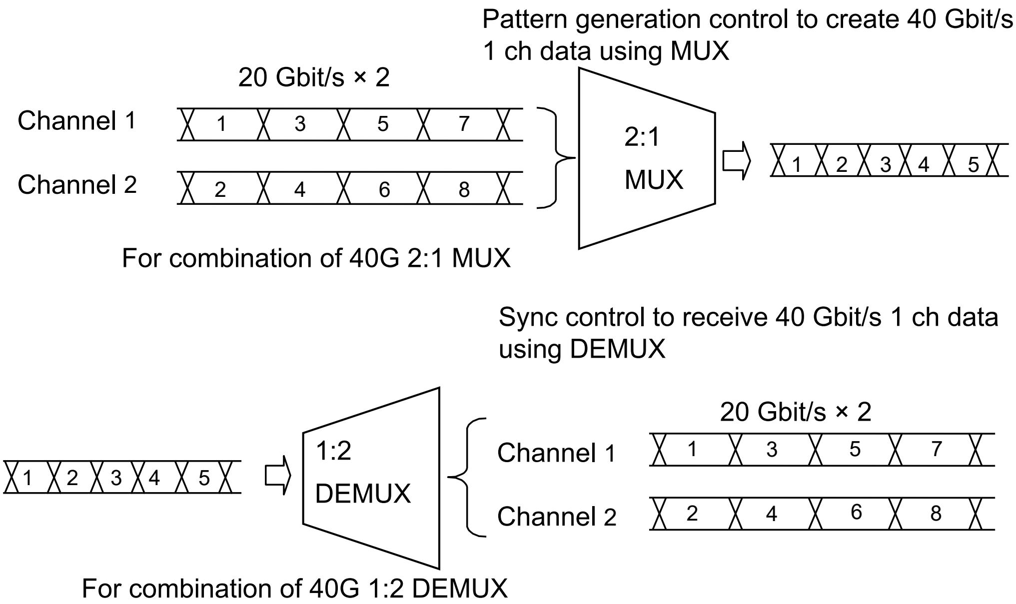

Figure 5.8.1-1 2ch Combination pattern generation/reception

By using the 64G × 2ch Combination function, it is possible to generate four sets of 32 G data combining up to two sets of 64 G data. These two data patterns can be serialized with an external MUX.

This function is available when two modules of MU195020A-x20 + x31 are installed.

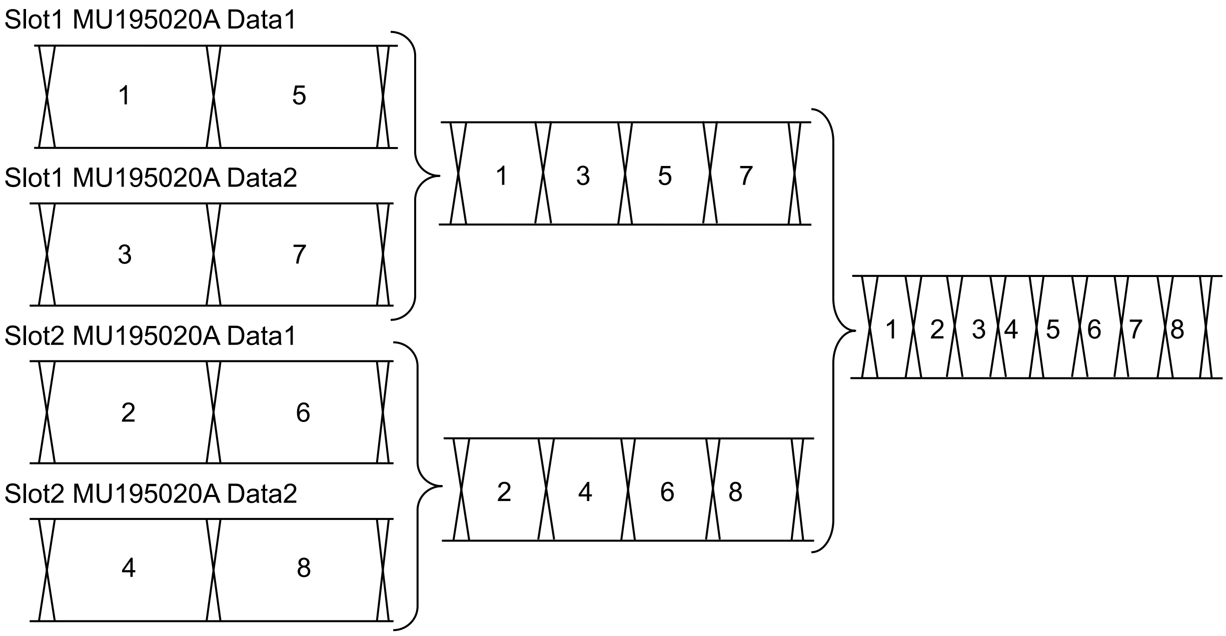

Figure 5.8.1-2 64G x 2ch Combination Pattern Generation (Using 2 modules of MU195020A)

5.8.2 Synchronization Function

Channel Synchronization function synchronizes the timing of data of multiple channels.

This function can also synchronize the timing of inter-modules (MU195020As). In addition, you can adjust the time delay between channels by setting the skew.

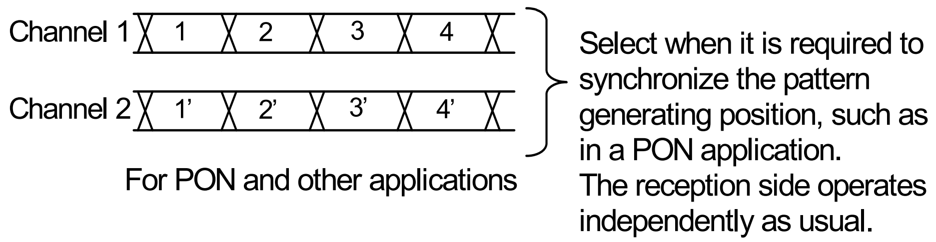

Figure 5.8.2-1 Channel Synchronization pattern generation/reception

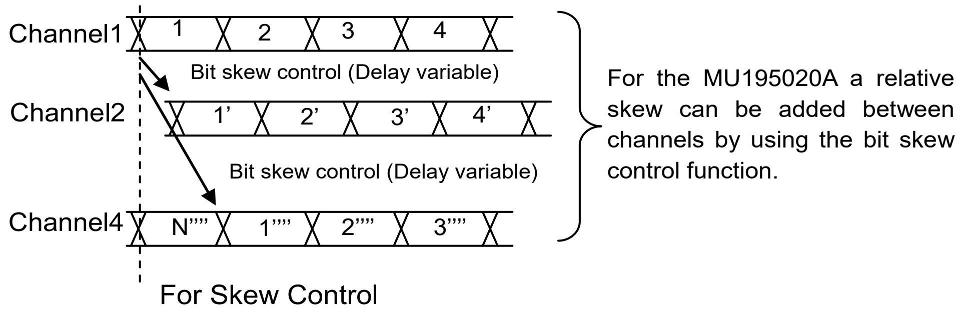

Figure 5.8.2-2 Skew Channel Synchronization Pattern

It is possible to Ch Synchronize the two signals of Combination 1 - 2 using two modules of MU195020A-x20 and synthesized by 2 ch Combination.

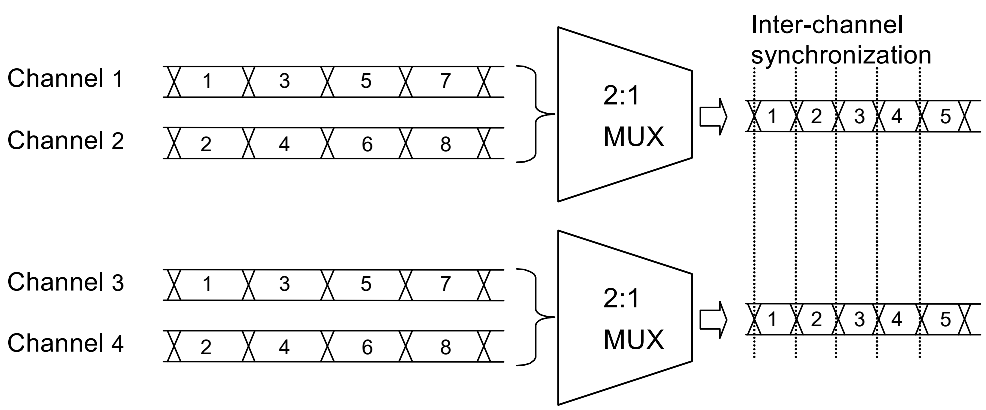

Figure 5.8.2-3 Channel Synchronization of 2Ch Combination

5.9 Inter-module Synchronization Function

To use the Inter-module synchronization function, touch the **Combination Setting** on the menu and set the parameters on the Combination Setting screen.
For details of the settings, refer to the *MX190000A Signal Quality Analyzer-R Control Software Operation Manual*.

Table 5.9-1 Setting items for Combination Setting

Operation Settings		Description
Independent		Select when operating the MU195020A independently.
Channel Synchronization	CH Sync[*1,*2]	Sets the Channel Synchronization function to all channels of the target modules.
	2ch Combination[*1,*2]	Sets the 2ch Combination to the target modules and sets the Channel Synchronization between modules.
	64G × 2ch Combination[*1,*2]	Install two modules of MU195020A. Set the 2ch Combination to the target modules, And then the pattern between modules are shifted by 1/4 pattern cycle each other. When using this setting, set the same pattern for each of the two MU195020A.

*1: MU195020A-x30 or MU195020A-x31 is required.

*2: MU195020A-x20 is required.

5.10 Multi Channel Calibration Function

Calibration must be executed to use the Multi Channel function or the Inter-module Synchronization function under the optimum conditions. These functions are required when changing the configuration such as rearranging the MU195020A installed in the MP1900A.

For details of the settings, refer to the *MX190000A Signal Quality Analyzer-R Control Software Operation Manual*.

5.11 Displaying Measurement Results

To see the measurement results, touch the **Result** tab on the MU195040A operation screen.

The **Result** tab consists of the item setting area (upper) and the result display area (lower). Measurement results can be viewed while changing the setting items of the MU195040A.

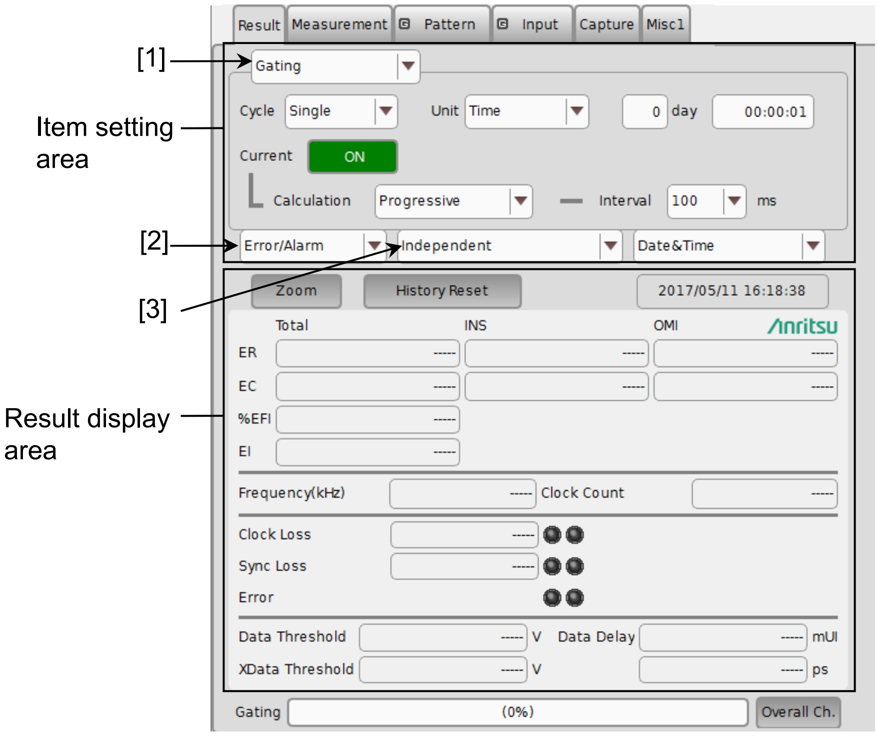

Figure 5.11-1 Result tab

The setting items change according to the item selected in the list box ([1] in the figure above) in the item setting area.

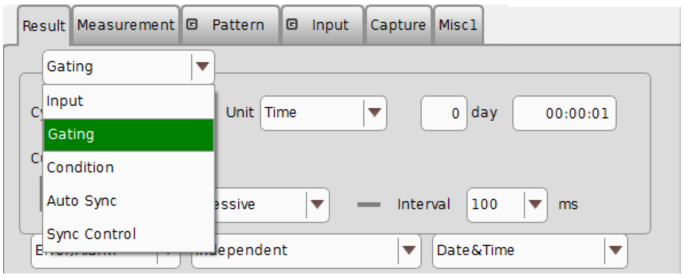

Figure 5.11-2 Item setting area

Table 5.11-1 Setting items of list box in item setting area

Item	Description
Input	Select to configure the settings related to the input signal interface.
Gating	Select to configure the settings related to the measurement period.
Condition	Select to configure the settings related to the measurement conditions.
Auto Sync	Select to configure the settings related to the automatic synchronization establishment function.
Sync Control	Select to configure the settings related to the synchronization establishment method.

The display items change according to the item selected in the list box ([2] in the Figure 5.11-1) in the result display area.
Note that the current version provides only **Error/Alarm** results.

Figure 5.11-3 Result display area

Table 5.11-2 Setting items of list box in result display area

Item	Description
Error/Alarm	Select to display the Error/Alarm measurement results.

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Display of channel combination can be switched by selecting from the list box ([3] in the Figure 5.11-1) result display area.

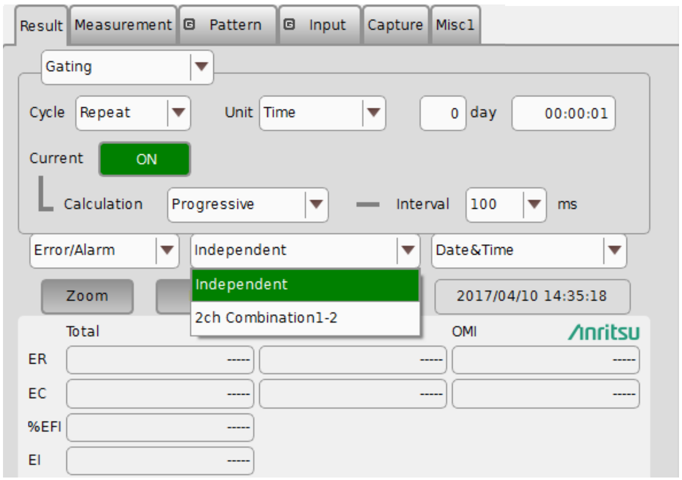

Figure 5.11-4 Result display area

Table 5.11-3 Setting items in list box in result display area

Item	Description
Independent	Single channel measurement result.
2ch Combination 1-2*	2ch combination measurement result of Data 1/2.

*: MU195040A-x20 has this item.

5.11.1 Setting when Input is selected

Set [1] to **Input** in the item setting area (Figure 5.11-1).

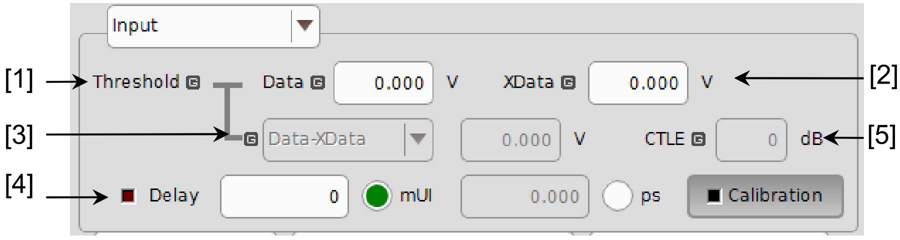

Figure 5.11.1-1 Items when Input is selected

[1] [2] Set the threshold voltage for Data input and XData input.

The Data signal is input from the Data Input connector of the MU MU195040A, and the XData signal is input from the Da Input connector. Hereinafter, the settings for the XData Input connector are described as the settings for Da.

The threshold voltage can be set within the range from –3.500 to +3.300 V, in 0.001 V steps.

Note, however, that the absolute difference between the threshold values set for Data and XData inputs is limited to 3.000 V or less if **Input Condition** is set to **Differential 50Ohm** or **Differential 100Ohm** on Figure 5.14.1-1 Input tab.

[3] Set the difference between the threshold voltages for Data and XData inputs.
This item is enabled when **Input Condition** is set to **Differential 50Ohm** or **Differential 100Ohm**, and **Alternate** is selected on Figure 5.14.1-1 Input tab.

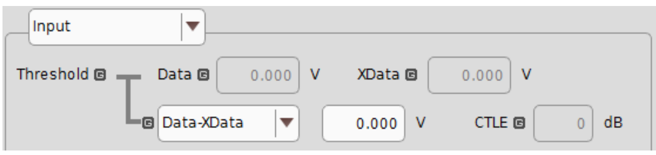

Figure 5.11.1-2 Input voltage threshold difference setting items

Select **Data-XData** or **XData-Data**. Set a value within the range from –3.000 to +3.000 V, in 0.001 V steps.

[4] Set the clock phase unit and phase variable.

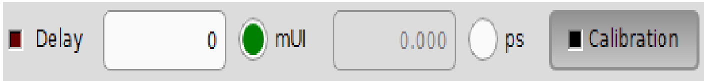

Figure 5.11.1-3 Clock phase setting item

Select the unit from mUI or ps by touching the radio button.

<When mUI is selected>

The setting range is from –1000 to +1000 mUI, in 2 mUI steps

<When ps is selected>

Delay time can be set by ps step that is equivalent to 2 mUI.

The setting range is equivalent to the range when the unit is mUI (–1000 to +1000 mUI), converted into ps units.

Table 5.11.1-1 Clock phase setting (in ps units)

Frequency	Setting range
32.1 GHz	–31.14 to 31.14
25 GHz	–40 to 40
2.4 GHz	–416 to 416

Notes:

- When the frequency or the temperature condition is changed, the LED on the “Calibration” lights, prompting performance of calibration. If calibration is not performed at this time, the error in the phase setting may be greater than at a normal phase setting.
- Values displayed in ps units vary as the frequency changes, because the MU195040A sets phases in mUI units as an internal standard.

[5] When MU195040A-x11/x21 is installed, set the CTLE gain. The value can be set in the range of 0 to –12 dB, in 0.1 dB steps.

Figure 5.11.1-4 CTLE setting

Select the CTLE Band on the **Input** tab.

Refer to the description in 5.14.1 “Input setting items”.

5.11.2 Setting when Gating is selected

Set [1] to **Gating** in the item setting area (Figure 5.11-1).

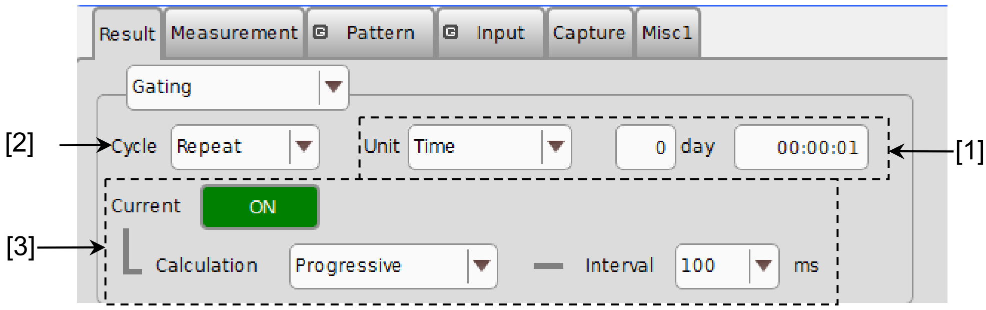

Figure 5.11.2-1 Gating setting items

[1] Select the unit of the measurement period from the Unit list box, and set the measurement period in the upper-right text box. When **Untimed** is selected from the **Cycle** list box, the value set by this parameter becomes invalid.

Table 5.11.2-1 Measurement period setting

Unit	Description
Time	Time can be set from 1 second to 99 days 23 hours 59 minutes 59 seconds in second units.
Clock Count	The setting range is from E+4 to E+16, in E+1 units. The minimum measurement time resolution is 1 second, so the measurement will end at the end of the 1-second period in which the clock count reaches the number specified by this parameter (refer to Figure 5.11.2-2).
Error Count	The setting range is from E+4 to E+16, in E+1 units. The minimum measurement time resolution is 1 second, so the measurement will end at the end of the 1-second period in which the error count reaches the number specified by this parameter (refer to Figure 5.11.2-2).
Block Count	The number of blocks to be executed is set to Gating when the test pattern is Mixed Pattern. The setting range is from E+2 to E+14, in E+1 units. The minimum measurement time resolution is 1 second, so the measurement will end at the end of the 1-second period in which the block count reaches the number specified by this parameter (refer to Figure 5.11.2-2).

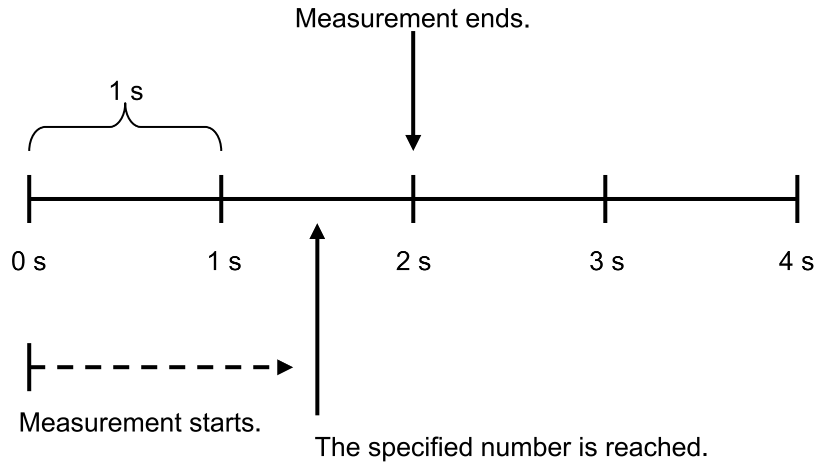

Figure 5.11.2-2 Measurement end timing

[2] Select the measurement operation from the **Cycle** list box.

Table 5.11.2-2 Setting Measurement Operation

Cycle	Description
Repeat	Specified-period measurement is performed repeatedly.
Single	Measurement ends when it is performed once for the specified period.
Untimed	Measurement is performed continuously from the measurement start instruction to the measurement end instruction.

[3] Set the measurement progress display method.

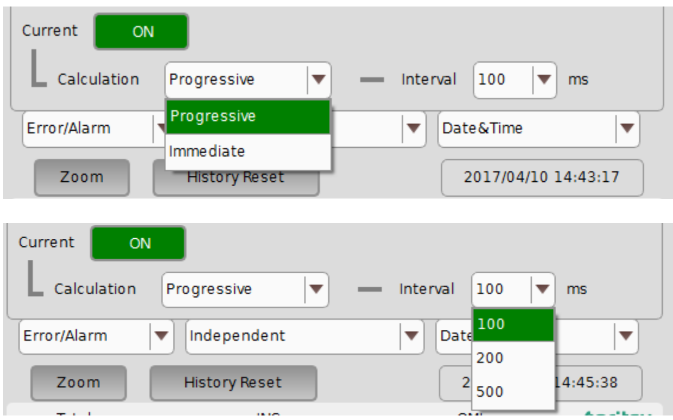

Figure 5.11.2-3 Measurement progress display setting items

Table 5.11.2-3 Measurement progress display setting

Current	Description
ON	The accumulated measurement result, up to the current time, is displayed in the specified interval (cycle time). Select 100 (ms), 200 (ms) or 500 (ms)* from the **Interval** list box for the cycle time. Select **Progressive** or **Immediate** from the Calculation list box for the method to display measurement results in the middle of the measurement. In the Progressive mode, the measurement result accumulated from the measurement start is displayed. In the Immediate mode, the immediate-value result for each cycle time is displayed.
OFF	The measurement result in the last measurement period is displayed. The display remains until the measurement ends for the next measurement period.

*: 500 (ms) is available only during 2ch Combination.

The following figure shows a correspondence between the selection in the Calculation list box (Progressive/Immediate) and the measurement result when the measurement period is 1 second and Interval is set to 200 ms.

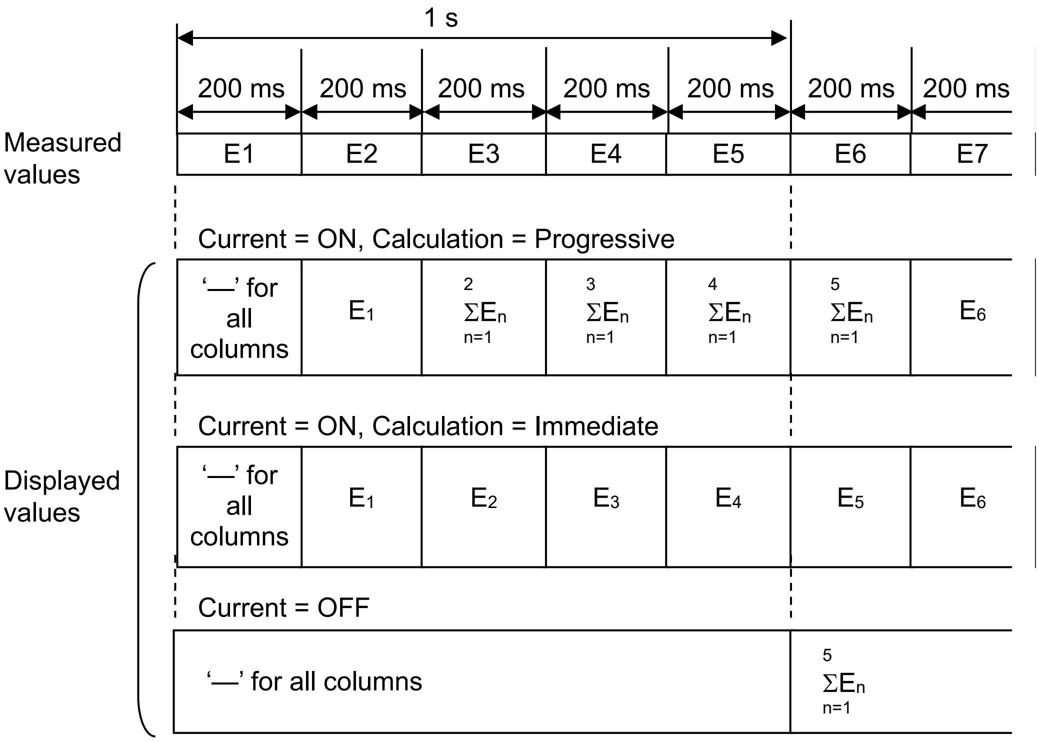

Figure 5.11.2-4 Relationship between measured values and displayed values

5.11.3 Setting when Condition is selected

Set [1] to **Condition** in the item setting area (Figure 5.11-1).

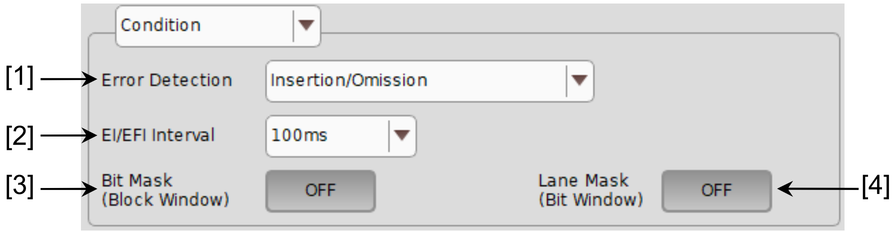

Figure 5.11.3-1 Items when Condition is selected

[1] Select the error detection method from the **Error Detection** list box.

Table 5.11.3-1 Error detection method setting

Error Detection	Description
Insertion/Omission	Counts errors where the bit pattern changes between 0 and 1. Insertion error: An error where the bit pattern changes from 0 to 1 Omission error: An error where the bit pattern changes from 1 to 0
Transition/Non Transition	Counts errors that occur in a transition or non-transition bit. Cannot be selected for Combination.

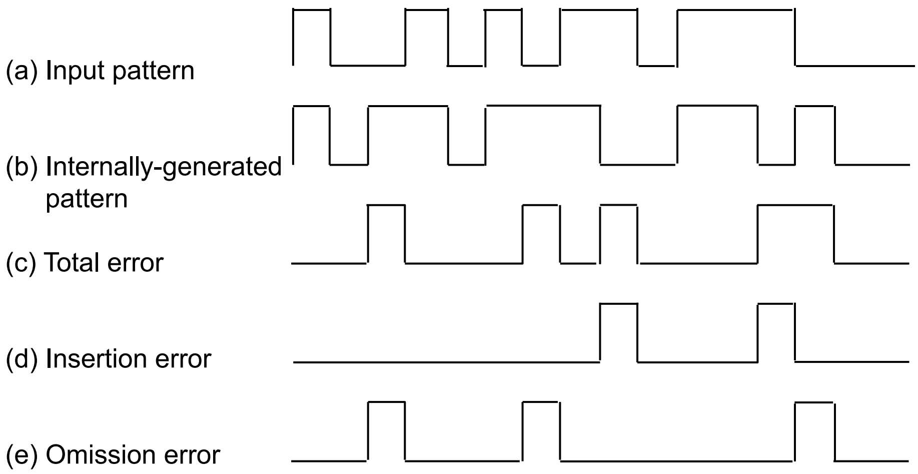

Figure 5.11.3-2 Error detection (Total, Insertion, and Omission errors)

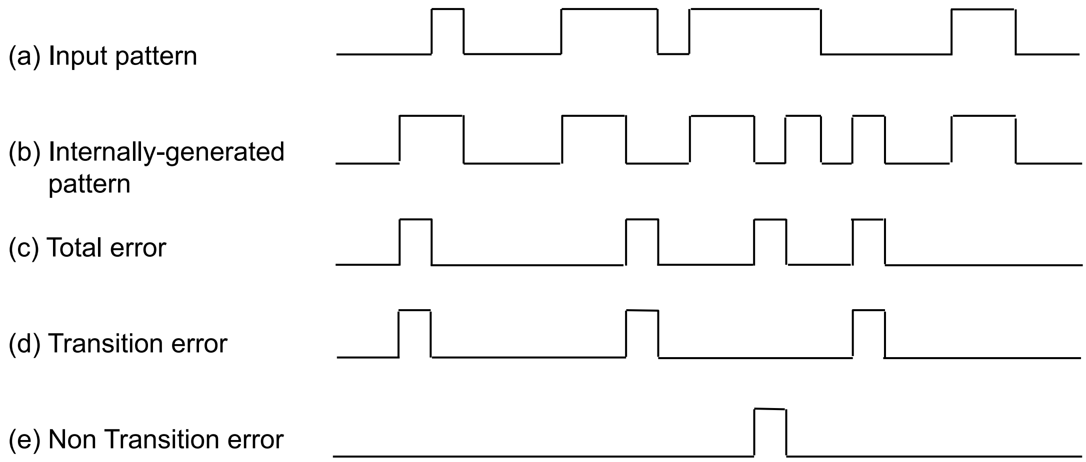

Figure 5.11.3-3 Error detection (Total, Transition, and Non Transition errors)

[2] Select the interval for error interval and error free interval measurements from the **EI/EFI Interval** list box.

Table 5.11.3-2 Interval time setting

EI/EFI Interval	Description
1ms	Sets the interval to 1 ms. The interval counter value indicates the number of intervals.
10ms	Sets the interval to 10 ms. The interval counter value indicates the number of intervals.
100ms	Sets the interval to 100 ms. The interval counter value indicates the number of intervals.
1s	“1” is applied if the result of 1-second accumulation of interval counter values is not 0.

[3] Specify whether to enable the Block Window function.
The Block Window function masks errors in the set area by setting a mask area for the patterns occurring internally. Refer to 5.3.7 “Editing test pattern in Pattern Editor dialog box” for details.

Table 5.11.3-3 Block window function setting

Block Window	Description
ON	Enables the Block Window function. Error measurement is masked for bits for which the Block Window setting is set to “1”.
OFF	Disables the Block Window function.

Note that Block Window cannot be set in the following cases:

- When the test pattern is **PRBS** or **Mixed**
- When capturing has started

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[4] Specify whether to enable the Bit Window function. The Bit Window function enables/disables measurement for every 32 bits of the test pattern. Refer to 5.3.7 “Editing test pattern in Pattern Editor dialog box” for details.

Table 5.11.3-4 Bit window function setting

Bit Window	Description
ON	Enables the Bit Window function.
OFF	Disables the Bit Window function.

5.11.4 Setting when Auto Sync is selected

Set [1] to **Auto Sync** in the item setting area (Figure 5.11-1).

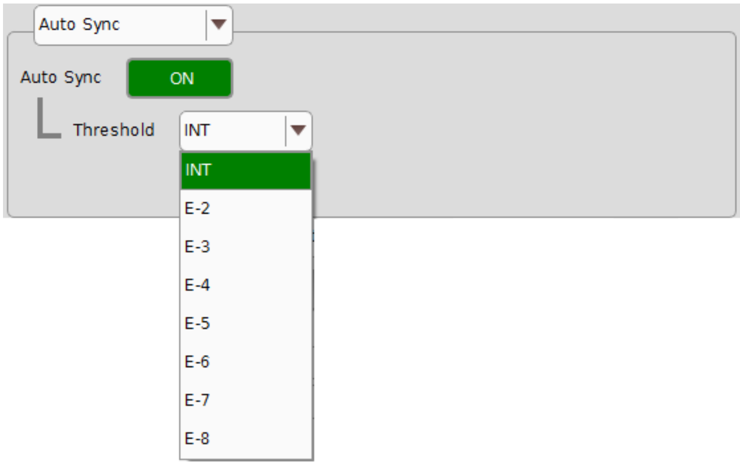

Figure 5.11.4-1 Items when Auto Sync is selected

[1] Specify whether to start resynchronization automatically when the synchronization threshold is exceeded from Sync Gain to Sync Loss.

Table 5.11.4-1 Auto sync setting

Auto Sync	Description
ON	Automatically starts resynchronization.
OFF	Does not start resynchronization automatically.

[2] Select the error rate threshold to execute resynchronization when Auto Sync is set to **ON**. From the **Threshold** list box, 10^{-N} (N = 2 to 8) or **INT** can be set.
When **INT** is set, whether the synchronization is established (Sync Gain) or lost (Sync Loss) is judged according to the synchronization threshold. If the error rate exceeds the synchronization threshold in the Sync Gain state, it is judged as a Sync Loss. On the other hand, if the error rate falls to the synchronization threshold or below in the Sync Loss state, it is judged as a Sync Gain.
For details on the synchronization threshold, refer to Table 5.11.4-2 for **INT** and Table 5.11.4-3 for 10^{-N} (N = 2 to 8).

Table 5.11.4-2 Synchronization thresholds when INT is set

Sync Control	Test Pattern	Data Length	Threshold error rate = $\left[\frac{\text{Error Count}}{\text{Clock Count}}\right]$ Sync Gain → Sync Loss	Threshold error rate = $\left[\frac{\text{Error Count}}{\text{Clock Count}}\right]$ Sync Loss → Sync Gain
–	PRBS, Mixed Pattern, PRBS part of Mixed Pattern	2n-1 (n=7, 9, 10, 11, 15, 20, 23, 31)	$\frac{(128) \times 2{,}000}{(2{,}048) \times 5{,}000} = \frac{1}{40} = 2.5\text{ E}-2$	$\frac{(128)}{(2{,}048) \times 4} = \frac{1}{64} = 1.56\text{ E}-2$
Frame ON, Quick	Mixed Data Part, ZeroSubstitution Data	128 to 5,120	$\frac{(128) \times 200}{(2{,}048) \times 64{,}000} = \frac{1}{5{,}120} = 1.95\text{ E}-4$	$\frac{(128) \times 1}{(2{,}048) \times \frac{\text{DataLength}}{128 \times 8}}$
		5,121 to 10,240	$\frac{(128) \times 200}{(2{,}048) \times 128{,}000} = \frac{1}{10{,}240} = 9.77\text{ E}-5$	$\frac{(128) \times 1}{(2{,}048) \times \frac{\text{DataLength}}{128 \times 8}}$
		10,241 to 51,200	$\frac{(128) \times 200}{(2{,}048) \times 640{,}000} = \frac{1}{51{,}200} = 1.95\text{ E}-5$	$\frac{(128) \times 1}{(2{,}048) \times \frac{\text{DataLength}}{128 \times 8}}$
		51,201 to 102,400	$\frac{(128) \times 200}{(2{,}048) \times 1{,}280{,}000} = \frac{1}{102{,}400} = 9.77\text{ E}-6$	$\frac{(128) \times 1}{(2{,}048) \times \frac{\text{DataLength}}{128 \times 8}}$
		102,401 to 204,800	$\frac{(128) \times 200}{(2{,}048) \times 2{,}560{,}000} = \frac{1}{204{,}800} = 4.88\text{ E}-6$	$\frac{(128) \times 1}{(2{,}048) \times \frac{\text{DataLength}}{128 \times 8}}$
		204,801 to 307,200	$\frac{(128) \times 200}{(2{,}048) \times 3{,}840{,}000} = \frac{(256) \times 200}{(4{,}096) \times 3{,}840{,}000} = \frac{1}{307{,}200} = 3.26\text{ E}-6$	$\frac{(128) \times 1}{(2{,}048) \times \frac{\text{DataLength}}{128 \times 8}} = \frac{(512) \times 1}{(8{,}192) \times \frac{\text{DataLength}}{128 \times 8}}$

Table 5.11.4-2 Synchronization thresholds when INT is set (Cont'd)

Sync Control	Test Pattern	Data Length	Threshold error rate = $\left[\frac{\text{Error Count}}{\text{Clock Count}}\right]$ Sync Gain → Sync Loss	Sync Loss → Sync Gain
Frame ON, Quick (cont'd)	Mixed Data Part, ZeroSubstitution Data (cont'd)	307,201 to 409,600	$\frac{(128) \times 200}{(2,048) \times 5,120,000} = \frac{(256) \times 200}{(4,096) \times 5,120,000} = \frac{1}{409,600} = 2.44\ E-6$	$\frac{(128) \times 1}{(2,048) \times \frac{DataLength}{128 \times 8}} = \frac{(512) \times 1}{(8,192) \times \frac{DataLength}{128 \times 8}}$
		409,601 to 524,288	$\frac{(128) \times 200}{(2,048) \times 6,553,600} = \frac{(256) \times 200}{(4,096) \times 6,553,600} = \frac{1}{524,288} = 1.91\ E-6$	$\frac{(128) \times 1}{(2,048) \times \frac{DataLength}{128 \times 8}} = \frac{(512) \times 1}{(8,192) \times \frac{DataLength}{128 \times 8}}$
		524,289 to 1,048,576	$\frac{(128) \times 200}{(2,048) \times 13,107,200} = \frac{(256) \times 200}{(4,096) \times 13,107,200} = \frac{1}{1,048,576} = 9.54\ E-7$	$\frac{(128) \times 1}{(2,048) \times \frac{DataLength}{128 \times 8}} = \frac{(512) \times 1}{(8,192) \times \frac{DataLength}{128 \times 8}}$
		1,048,577 to 2,097,152	$\frac{(128) \times 200}{(2,048) \times 26,214,400} = \frac{(256) \times 200}{(4,096) \times 26,214,400} = \frac{1}{2,097,152} = 4.77\ E-7$	$\frac{(128) \times 1}{(2,048) \times \frac{DataLength}{128 \times 8}} = \frac{(512) \times 1}{(8,192) \times \frac{DataLength}{128 \times 8}}$
		2,097,153 to 4,194,304	$\frac{(128) \times 200}{(2,048) \times 52,428,800} = \frac{(256) \times 200}{(4,096) \times 52,428,800} = \frac{1}{4,194,304} = 2.38\ E-7$	$\frac{(128) \times 1}{(2,048) \times \frac{DataLength}{128 \times 8}} = \frac{(512) \times 1}{(8,192) \times \frac{DataLength}{128 \times 8}}$

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Table 5.11.4-2 Synchronization thresholds when INT is set (Cont'd)

Sync Control	Test Pattern	Data Length	Threshold error rate = $\left[\frac{\text{Error Count}}{\text{Clock Count}}\right]$ Sync Gain → Sync Loss	Sync Loss → Sync Gain
Frame ON, Quick (cont'd)	Mixed Data Part, ZeroSubstitution Data (cont'd)	4,194,305 to 8,388,608	$\frac{(128)\times 200}{(2,048)\times 104,857,600}$ $=\frac{1}{8,388,608}$ $= 1.19\ E-7$	$\frac{(128)\times 1}{(2,048)\times \frac{\text{DataLength}}{128\times 8}}$
		8,388,609 to 16,777,216	$\frac{(128)\times 200}{(2,048)\times 209,715,200}$ $=\frac{1}{16,777,216}$ $= 5.96\ E-8$	$\frac{(128)\times 1}{(2,048)\times \frac{\text{DataLength}}{128\times 8}}$
		16,777,217 to 33,554,432	$\frac{(128)\times 200}{(2,048)\times 419,430,400}$ $=\frac{1}{33,554,432}$ $= 2.98\ E-8$	$\frac{(128)\times 1}{(2,048)\times \frac{\text{DataLength}}{128\times 8}}$
		33,554,433 to 67,108,864	$\frac{(128)\times 200}{(2,048)\times 838,860,800}$ $=\frac{1}{67,108,864}$ $= 1.49\ E-8$	$\frac{(128)\times 1}{(2,048)\times \frac{\text{DataLength}}{128\times 8}}$
		67,108,865 to 134,217,728	$\frac{(128)\times 200}{(2,048)\times 1,677,721,600}$ $=\frac{1}{134,217,728}$ $= 7.45\ E-9$	$\frac{(128)\times 1}{(2,048)\times \frac{\text{DataLength}}{128\times 8}}$
		134,217,729 to 268,435,456	$\frac{(128)\times 200}{(2,048)\times 3,355,443,200}$ $=\frac{1}{268,435,456}$ $= 3.73\ E-9$	$\frac{(128)\times 1}{(2,048)\times \frac{\text{DataLength}}{128\times 8}}$

Table 5.11.4-3 Synchronization thresholds when one of E-2 to E-8 is set

Sync Control	Threshold error rate = $\left[\frac{\text{Error Count}}{\text{Clock Count}}\right]$	
	Sync Gain → Sync Loss	Sync Loss → Sync Gain
E–2	$\frac{(128)\times 2{,}000}{(2{,}048)\times 5{,}000} = \frac{1}{40} = 2.5\text{ E}-2$	$\frac{(128)}{(2{,}048)\times 4} = \frac{1}{64} = 1.56\text{ E}-2$
E–3	$\frac{(128)\times 2{,}000}{(2{,}048)\times 50{,}000} = \frac{1}{400} = 2.5\text{ E}-3$	$\frac{(128)}{(2{,}048)\times 40} = \frac{1}{640} = 1.56\text{ E}-3$
E–4	$\frac{(128)\times 2{,}000}{(2{,}048)\times 500{,}000} = \frac{1}{4{,}000} = 2.5\text{ E}-4$	$\frac{(128)}{(2{,}048)\times 400} = \frac{1}{6{,}400} = 1.56\text{ E}-4$
E–5	$\frac{(128)\times 2{,}000}{(2{,}048)\times 5{,}000{,}000} = \frac{1}{40{,}000} = 2.5\text{ E}-5$	$\frac{(128)}{(2{,}048)\times 4{,}000} = \frac{1}{64{,}000} = 1.56\text{ E}-5$
E–6	$\frac{(128)\times 2{,}000}{(2{,}048)\times 50{,}000{,}000} = \frac{1}{400{,}000} = 2.5\text{ E}-6$	$\frac{(128)}{(2{,}048)\times 40{,}000} = \frac{1}{640{,}000} = 1.56\text{ E}-6$
E–7	$\frac{(128)\times 2{,}000}{(2{,}048)\times 500{,}000{,}000} = \frac{1}{4{,}000{,}000} = 2.5\text{ E}-7$	$\frac{(128)}{(2{,}048)\times 400{,}000} = \frac{1}{6{,}400{,}000} = 1.56\text{ E}-7$
E–8	$\frac{(128)\times 2{,}000}{(2{,}048)\times 5{,}000{,}000{,}000} = \frac{1}{40{,}000{,}000} = 2.5\text{ E}-8$	$\frac{(128)}{(2{,}048)\times 4{,}000{,}000} = \frac{1}{64{,}000{,}000} = 1.56\text{ E}-8$

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5.11.5 Setting when Sync Control is selected

Set [1] to **Sync Control** in the item setting area (Figure 5.11-1).

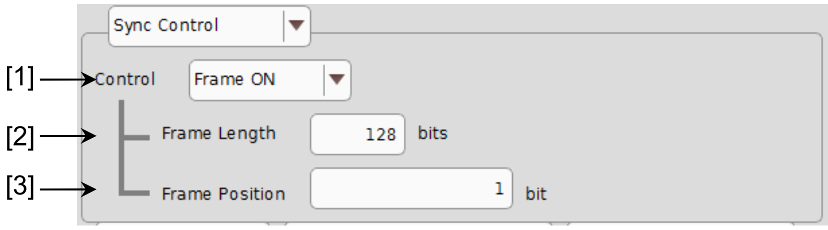

Figure 5.11.5-1 Items when Sync Control is selected

[1] Select the test pattern synchronization method.

Table 5.11.5-1 Sync control setting

Control	Description
Frame ON	Selects the frame synchronization method. This can be selected when the test pattern is ZeroSubstitution, Data, or Mixed. Synchronization is established upon frame pattern detection.
Quick	Selects the quick synchronization method. This can be selected when the test pattern is ZeroSubstitution or Data. Error measurement is performed using the pattern that has been saved into the internal memory as the reference pattern.

The test pattern synchronization methods selectable from the Control list box vary depending on the test pattern selected on the **Pattern** tab. Refer to the Table 5.11.5-2.

Table 5.11.5-2 Synchronization method setting

Test Pattern	Control setting	
	Frame ON	Quick
PRBS	Not available	Not available
ZeroSubstitution	Available	Available
Data	Available	Available
Mixed	Available	Not available

[2] Set the frame pattern length when **Frame ON** is selected from the Control list box. In the Frame Length text box, 4 to 64 can be set in 4-bit steps.

The number of frame bits increases by N times (N ch Combi) when a Channel Combination is set.

Note:

If synchronization is hardly achieved during the combination, set the frame pattern length to 64 bits.

[3] Set the start position of the pattern for frame detection when **Frame ON** is selected from the **Control** list box. The setting range of Frame Position is shown below:

- In case of Independent:
  1 to {(Length of pattern for frame detection) – (Frame Length + 1)} in 1-bit steps.
- In case of 2ch Combination:
  1 to 1+2n, in 2-bit steps
  Maximum value of n = INT((Length of pattern for frame detection – Frame Length) / 2)

The length of the pattern for frame detection varies depending on the test pattern selected on the **Pattern** tab. Refer to the table below.

Table 5.11.5-3 Setting of pattern length for frame detection

Test Pattern	Length of pattern for frame detection
ZeroSubstitution	Pattern length
Data	Pattern length
Mixed	Pattern length of Row1 of Block1

Note:

When **Frame ON** is set, synchronization may take a long time if there is another pattern that is the same as the set frame pattern. The frame pattern is therefore recommended to be specific.
The pattern length described here is the number multiplied by an integer so that it becomes 512 bits or more, when the length on the "Figure 5.3-1 Pattern tab" is 511 bit or less.

5.11.6 Setting items when Error/Alarm is selected

Set [2] to **Error/Alarm** in the item setting area (Figure 5.11-1).

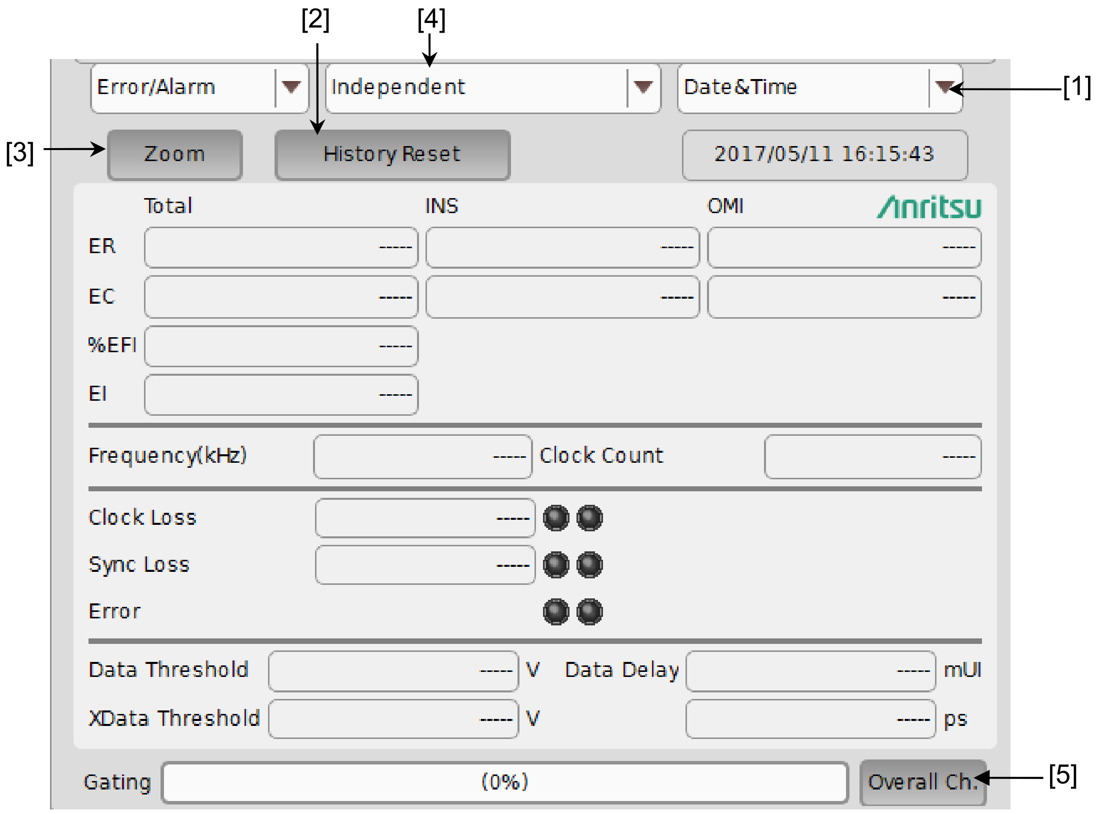

Figure 5.11.6-1 Items when Error/Alarm is selected

[1] Select the measurement time display type.

Date&Time: Select to display the current time.

Start Time: Select to display the measurement start time.

Elapsed Time: Select to display the elapsed time in the measurement period.

Remaining Time: Select to display the remaining time in the measurement period.

[2] Reset Error/Alarm history data.

History Reset: Touch to reset the history data of the error/alarm display.

[3] Enable or disable enlarged display of Error/Alarm measurement result.

Zoom: Touch to enlarge the display of the error count, error rate, error interval count, Clock Loss interval count, Sync Loss interval count, Clock Loss occurrence state, Sync Loss occurrence state, and error occurrence state.

When the enlarged display is disabled (Zoom is not selected), the items shown in Table 5.11.6-1 are displayed in the result display area with Error/Alarm selected.

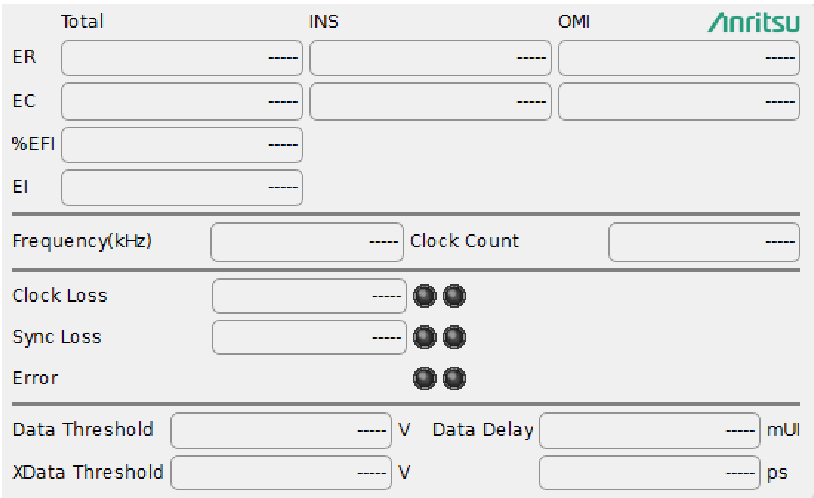

Figure 5.11.6-2 Items when Zoom is not selected

Total/INS/OMI or Transition/Non Transition is displayed according to the error detection method set in the setting item area when Condition is selected (refer to Section 5.11.3).

Table 5.11.6-1 Items (controls) when Zoom is not selected

Item		Function
ER	Total	Displays the total error rate.
	INS	Displays the insertion error rate.
	OMI	Displays the omission error rate.
	Transition	Displays the transition bit error rate.
	Non Transition	Displays the non-transition bit error rate.
EC	Total	Displays the total error count.
	INS	Displays the insertion error count.
	OMI	Displays the omission error count.
	Transition	Displays the transition bit error count.
	Non Transition	Displays the non-transition bit error count.
%EFI		Displays the error free interval rate.
EI		Displays the number of intervals where an error occurs.
Frequency(kHz)		Displays the frequency.
Clock Count		Displays the clock count.
Clock Loss		Displays the Clock Loss interval count and monitored occurrence state. Lights in red: Current data Lights in yellow: History data
Sync Loss		Displays the Sync Loss interval count and monitored occurrence state. Lights in red: Current data Lights in yellow: History data
Error		Displays the monitored error occurrence state. Lights in red: Current data Lights in yellow: History data
Data Threshold		Displays the Data Threshold voltage when Auto Adjustment is executed.
XData Threshold		Displays the XData Threshold voltage when Auto Adjustment is executed.
Data Delay		Displays the Delay value when Auto Adjustment is executed.

When the enlarged display is enabled (Zoom is selected), the items shown in Table 5.11.6-2 are displayed in the result display area with Error/Alarm selected.

Figure 5.11.6-3 Items when Zoom is selected

Table 5.11.6-2 Items (controls) when Zoom is selected

Item	Function
ER	Displays the error rate.
EC	Displays the error count.
Clock Loss	Displays the Clock Loss interval count and monitored occurrence state. Lights in red: Current data Lights in yellow: History data
Sync Loss	Displays the Sync Loss interval count and monitored occurrence state. Lights in red: Current data Lights in yellow: History data
Error	Displays the monitored error occurrence state. Lights in red: Current data Lights in yellow: History data

[4] Combination display
Select Combination condition of result display.

[5] Open/close Overall Ch Error/Alarm display.

Open/close test result dialog box.

Table 5.11.6-3 shows Overall Ch contents.

Table 5.11.6-3 Overall Ch contents

Item		Function
ER	Total	Displays the total error rate.
	INS	Displays the insertion error rate.
	OMI	Displays the omission error rate.
	Transition	Displays the transition bit error rate.
	Non Transition	Displays the non-transition bit error rate.
EC	Total	Displays the total error count.
	INS	Displays the insertion error count.
	OMI	Displays the omission error count.
	Transition	Displays the transition bit error count.
	Non Transition	Displays the non-transition bit error count.
Clock Loss		Displays the Clock Loss interval count and monitored occurrence state. Lights in red: Current data Lights in yellow: History data
Sync Loss		Displays the Sync Loss interval count and monitored occurrence state. Lights in red: Current data Lights in yellow: History data
Error		Displays the monitored error occurrence state. Lights in red: Current data Lights in yellow: History data

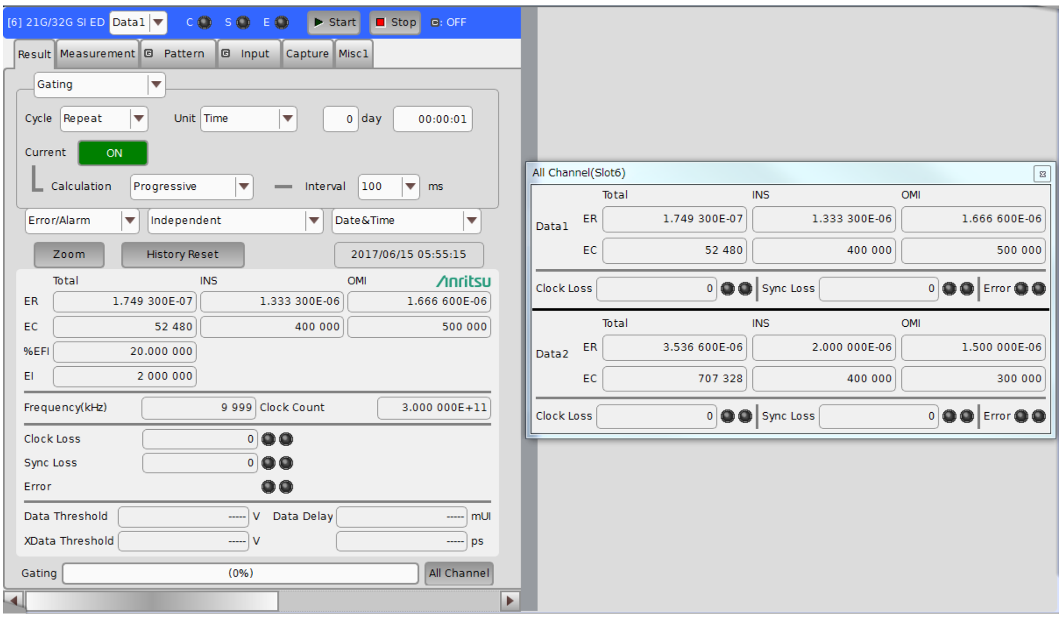

Figure 5.11.6-4 Result Sub Display window (2ch Combination)

5.11.7 When inputting jitter-modulated signals

- When executing jitter tolerance test, etc. by inputting jitter-modulated clock, set **Jitter Input** of Delay to **ON** to avoid malfunction of Delay caused by excess jitter modulation. (Refer to Figure 5.11.7-1.) When using the MU181000A/B (with Option 001 Jitter Modulation) or MU181500B, set **Jitter Input** of Delay to **ON**, and then set **Jitter Modulation** of the MU181000A/B or MU181500B to **ON**.
- When executing Calibration of Delay, set jitter modulation of input signal to non-modulation.

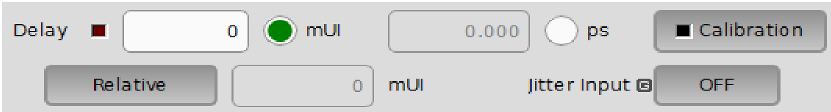

Figure 5.11.7-1 Clock delay setting items

Notes:

- When jitter-modulated clock is input while **Jitter Input** of Delay is set to **OFF**, the phase may become unstable.
- The Delay lamp may light up when a jitter-modulated clock signal is input. In addition, phase setting error may increase.
- The Delay function has feedback process to improve its setting accuracy at default setting (**Jitter Input** is set to **OFF**.). However, if **Jitter Input** is set to **ON**, the setting accuracy is lowered because the feedback process is stopped. Set Jitter Input according to the use as shown in the table below.

Jitter Input	Use
ON	Jitter Tolerance Measurement BER measurement when jitter amount applied to clock signal is big. (Delay is unstable when **Jitter Input** is **OFF**.)
OFF	Phase margin measurement Eye Margin measurement, Eye Diagram measurement, Bathtub measurement

5.12 Setting Measurement Conditions

Set the measurement conditions on the **Measurement** tab on the MU195040A operation screen.

The **Measurement** tab consists of five setting and displaying areas. Figure 5.12-1 and Table 5.12-1 show the configuration of the **Measurement** tab.

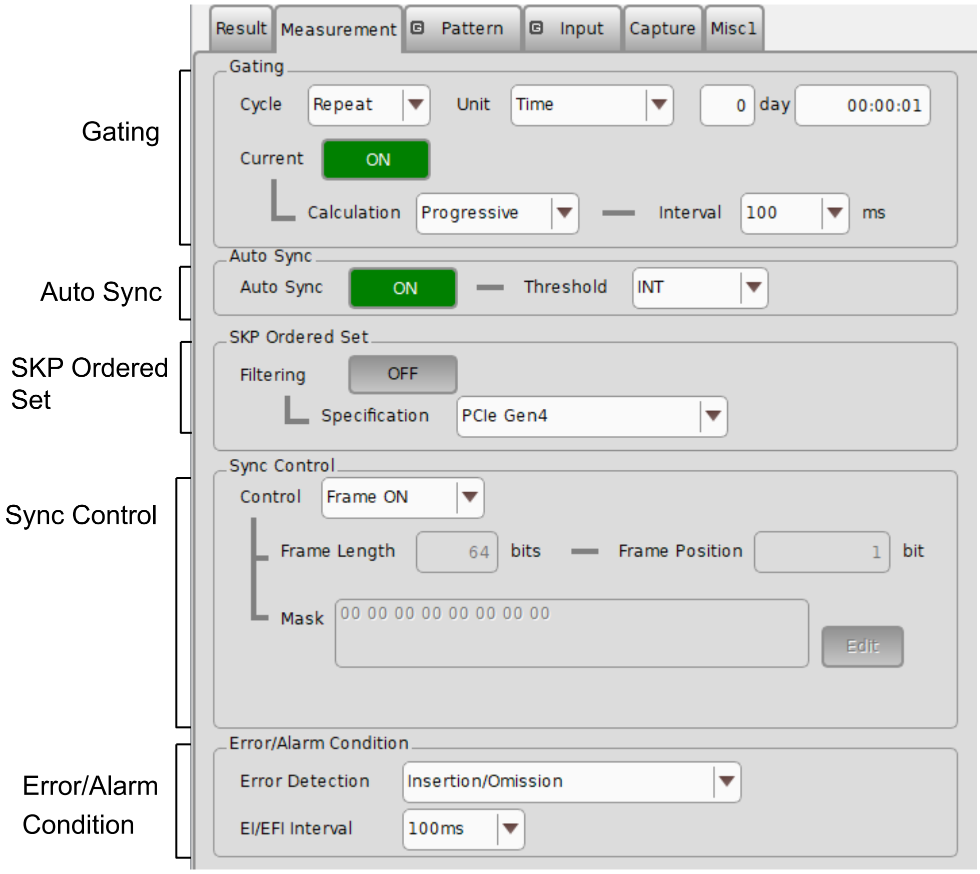

Figure 5.12-1 Measurement tab

Table 5.12-1 Setting/displaying areas of Measurement tab

Area	Description
Gating	Contains items for configuring the settings related to the measurement period.
Auto Sync	Contains items for configuring the settings related to the automatic synchronization establishment function.
SKP Ordered Set	Contains items for configuring the settings related to the SKP Ordered Set filtering.
Sync Control	Contains items for configuring the settings related to the synchronization establishment method.
Error/Alarm Condition	Contains items for configuring the settings related to the measurement method.

Although similar settings can be configured on the **Result** tab, more detailed settings are possible from the Sync Control and Error/Alarm areas on the **Measurement** tab.

5.12.1 Gating area

The setting operations in the Gating area are the same as those in the setting item area of the **Result** tab when **Gating** is selected. Refer to 5.11.2 “Setting when Gating is selected” for details.

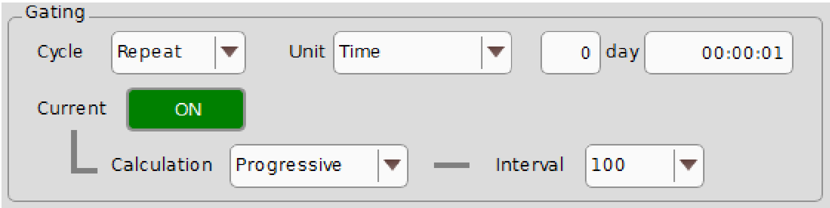

Figure 5.12.1-1 Measurement period setting items in Gating area

5.12.2 Auto Sync area

The setting operations in the Auto Sync area are the same as those in the setting item area of the **Result** tab when **Auto Sync** is selected. Refer to 5.11.4 “Setting when Auto Sync is selected” for details.

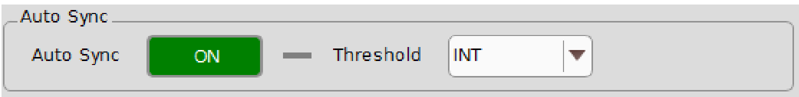

Figure 5.12.2-1 Measurement period setting items in Auto Sync area

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5.12.3 SKP Ordered Set area

Contains items for configuring the settings related to the SKP Ordered Set filtering.

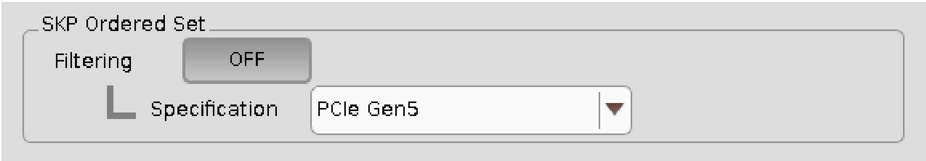


Figure 5.12.3-1 Filtering setting items in SKP Ordered Set area

Table 5.12.3-1 Items to Set in the SKP Ordered Set Area

Item	Description
Filtering	Sets whether to filter the SKP Ordered Set . The filtered Ordered Set is not included in the error count. ON: Filters the SKP Ordered Set. OFF: Does not filter the SKP Ordered Set.
Specification	Select one of the PCIe Gen1 to PCIe Gen5 standards. This is not available when **Filtering** is set to **ON**.

The following are the restrictions applicable when using the SKP Filtering function.

- The MU195040A interface uses Data1.
- The MU195040A is installed with the MU195040A-x22.
- On the **Input** tab, **Clock and Data Recovery** is set for the clock source.
- In the **Combination Setting** dialog box, MU195040A is set to **Independent**.
- The pattern is set to **Data**, and the selected test pattern includes the SKP Ordered Set adhering to the encoding rule defined in the specifications.
  In the SKP Ordered Set area, Filtering cannot be turned **ON** if Test Pattern is set to PRBS, ZeroSubstitution or Mixed.

The following shows examples of test patterns to set.

Table 5.12.3-2 Test Pattern Recommended for SKP Ordered Set Filtering

Spec.	Test Pattern to Set for MU195020A	Test Pattern to Set for MU195040A
PCIe1	8b10b_CP_L0_SKP.ptn	8b10b_CP_L0.ptn
PCIe2	8b10b_CP_L0_SKP.ptn	8b10b_CP_L0.ptn
PCIe3	128b130b_MCP_L0_Gen3.ptn	128b130b_MCP_L0_Gen3_SRIS_NOSKP.ptn
PCIe4	128b130b_MCP_L0_Gen4.ptn	128b130b_MCP_L0_Gen4_SRIS_NOSKP.ptn
PCIe5	128b130b_MCP_L0_Gen5.ptn	128b130b_MCP_L0_Gen5_SRIS_NOSKP.ptn

5.12.4 Sync Control area

In the Sync Control area, the setting operations for the test pattern synchronization method, frame length, and start position of the pattern for frame detection are the same as those in the setting item area of the **Result** tab when **Sync Control** is selected.

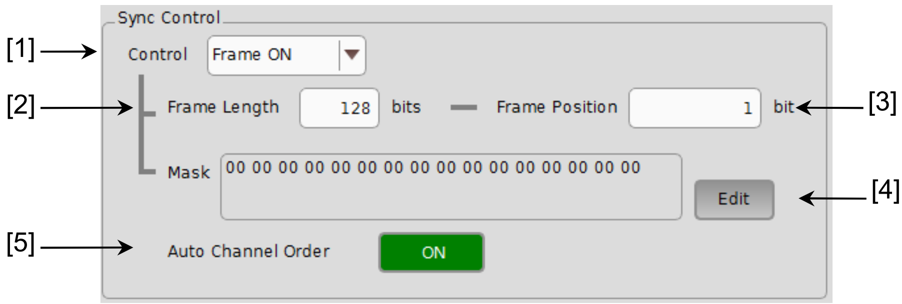


Figure 5.12.4-1 Synchronization establishment method setting items in Sync Control area

[1] Select the test pattern synchronization method.

[2] Set the frame pattern length. (Available when **Frame ON** is selected from the **Control** list box.)

[3] Set the start position of the pattern for frame detection. (Available when **Frame ON** is selected from the **Control** list box.) Refer to 5.11.5 "Setting when Sync Control is selected" for details.

[4] Edit the mask pattern.
(Available when **Frame ON** is selected from the **Control** list box.)

[5] Automatically arranges the 2 input channels in right order at 2ch Combination.
When this is On, it automatically detects the demultiplexed data at 2ch Combination and synchronize it.
When it is Off, the measurement is not performed properly if the 2 data channels are not arranged in right order.

5.12.5 Error/Alarm Condition area

In the Error/Alarm Condition area, the setting operations for the error detection method, error interval, and error free interval are the same as those in the setting item area of the **Result** tab when **Condition** is selected.

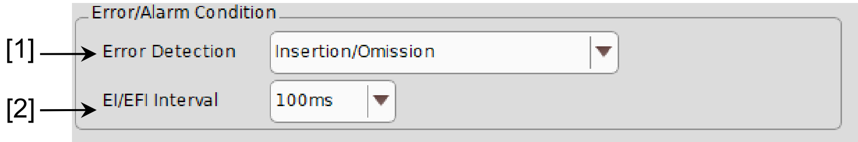


Figure 5.12.5-1 Measurement setting items in Error/Alarm Condition area

[1] Select the error detection method. Refer to 5.11.3 "Setting when Condition is selected" for details.

[2] Select the error interval and error free interval. Refer to 5.11.3 "Setting when Condition is selected" for details.

5.13 Setting Test Patterns (MU195040A)

To set the ED pattern, touch the **Pattern** tab on the MU195040A operation screen. Select a test pattern and set other items.

The operation is common with MU195020A, so refer to 5.3 “Setting Test Patterns (MU195020A)".

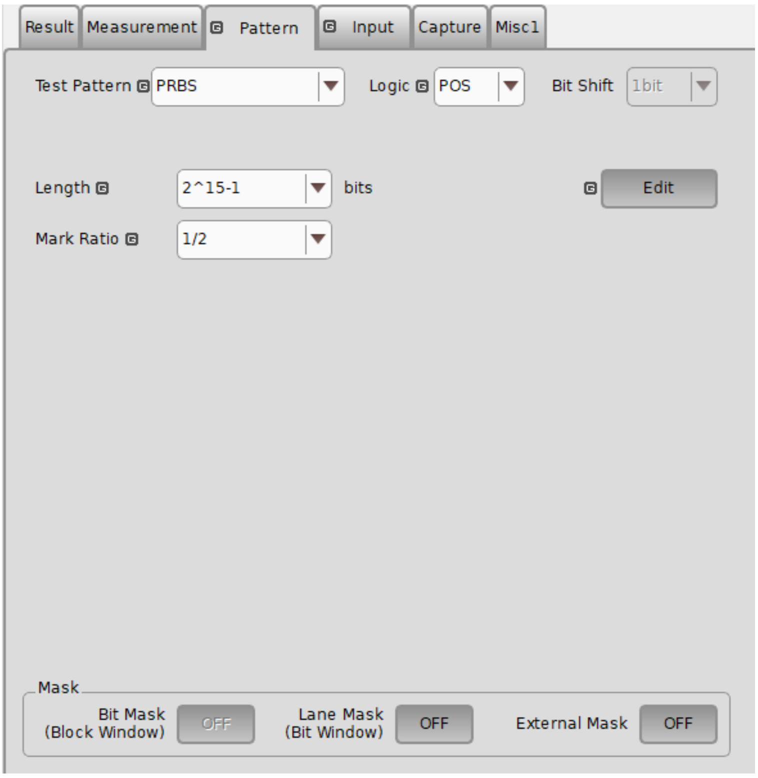


Figure 5.13-1 Pattern tab

Table 5.13-1 Setting/displaying areas in Pattern tab

Area	Description
Test Pattern	Select a test pattern. The setting items vary depending on the selected test pattern. The following five test patterns, are the same as 5.3.1 “Test Pattern type”. ● PRBS ● ZeroSubstitution ● Data ● Mixed ● PAM4
Mask	Contains items for setting Bit Mask, Lane Mask, and External Mask.

5.13.1 Mask selection

This section describes the controls in the mask area, which are used to mask a route and bit for the test pattern.
The mask positions can be set in the **Pattern Editor** dialog box.

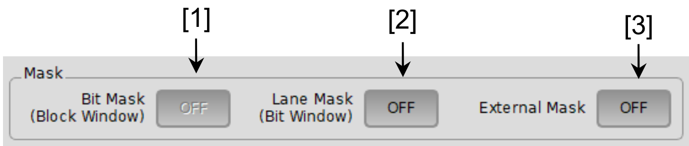


Figure 5.13.1-1 Controls in Mask area

[1] Enables (ON) or disables (OFF) the Block Window function.
The Block Window function specifies whether to enable or disable measurement (measurement mask) for each bit of the test pattern to be received. The mask positions can be set in the **Pattern Editor** dialog box.

Table 5.13.1-1 Block Window ON/OFF setting

Block Window	Description
ON	Enables the Block Window function.
OFF	Disables the Block Window function.

Note that the following restrictions apply:

- The Block Window cannot be executed when the test pattern is **PRBS** or **Mixed**.

In Block Window function, the bit which 1 bit of Block Window takes charge of with pattern length changes as follows.
N is number of Combination. At the time of Combination, Pattern Length and Step increase N times.

Pattern Length setting			Block Window step
2*N	to	2,097,152*N bits	1*N bits
2,097,153*N	to	4,194,304*N bits	2*N bits
4,194,305*N	to	8,388,608*N bits	4*N bits
8,388,609*N	to	16,777,216*N bits	8*N bits
16,777,217*N	to	33,554,432*N bits	16*N bits
33,554,433*N	to	67,108,864*N bits	32*N bits
67,108,864*N	to	134,217,728*N bits	64*N bits
134,217,729*N	to	268,435,456*N bits	128*N bits

Example:

When Control is 2ch Combination and Pattern length is 4,194,300 bits, the Block Window Step is set to 2 bits.

[2] Enables (ON) or disables (OFF) the Bit Window function.
While test pattern measurement is usually performed using 32 error counters, the Bit Window function can mask measurement of the specified counter (route).
The following figure shows an example where the test pattern is a 32-bit length Data pattern and the error counters 2 and 4 are masked.

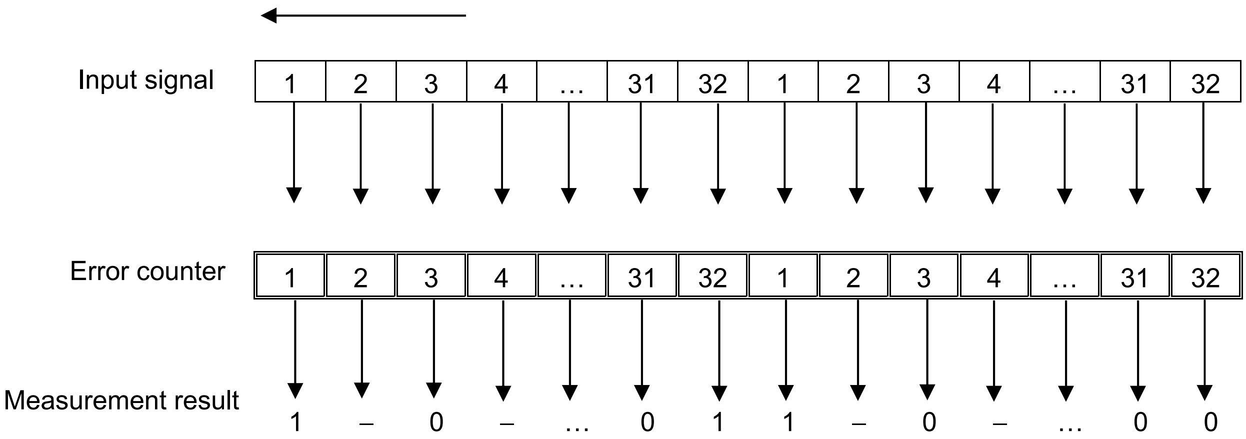


Figure 5.13.1-2 Bit Window Function

In this example, even if an error is detected by the masked counter 2 or 4, it is not included in the measurement result.

The mask position can be set in the **Pattern Editor** dialog box.

Table 5.13.1-2 Bit Window ON/OFF setting

Bit Window	Description
ON	Enables the Bit Window function.
OFF	Disables the Bit Window function.

[3] Enables (ON) or disables (OFF) the External Mask signal.

This control is available only when **External Mask** is selected from the **AUX Input** list box on the **Misc1** tab in the MU195040A window.

Table 5.13.1-3 External Mask ON/OFF setting

External Mask	Description
ON	Enables the External Mask signal.
OFF	Disables the External Mask signal.

5.13.2 Setting HSSB Data

MU195040A can measure BER by loading the 8b10b, 128b130b, and 128b132b patterns set using the SI PPG Sequence Editor.

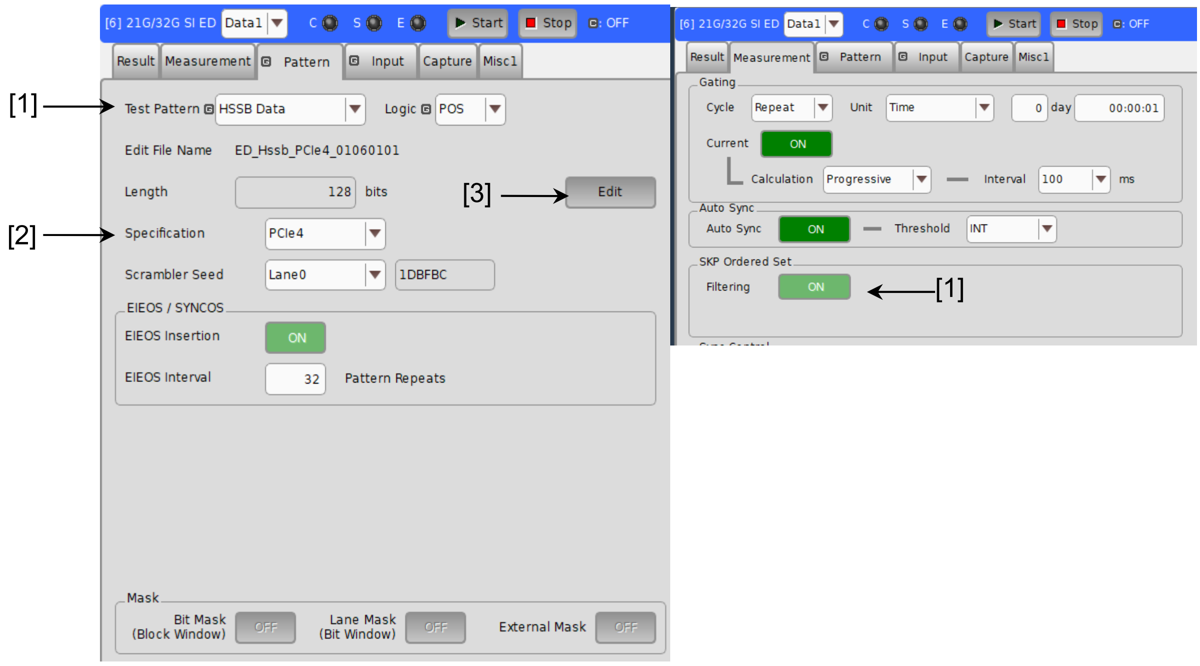


Figure 5.13.2-1 Setting HSSB Data

[1] On the **Pattern** tab for MU195040A, select **HSSB Data** in the Test Pattern box. When HSSB Data is selected, Filtering under SKP Ordered Set is always set to **ON**.

[2] Select a test specification.

[3] When **Edit** is touched, the pattern for the selected specification is displayed in the Editor screen. The following table shows the correspondence between specifications and encoding rules.

Table 5.13.2-1 Specification and encoding rules

Specification	Encoding rule
PCIe1	8b10b
PCIe2	8b10b
PCIe3	128b130b
PCIe4	128b130b
USB3.0	8b10b
USB3.1 Gen2	128b132b

5.13.3 Example of How to Configure BER Measurement Settings

This chapter describes how to measure BER using a DUT.
As examples, BER measurement procedures for the following patterns are described.

- TS pattern in the PCIe4.0 Recovery.Equalization Phase 1 state for PCIe4
- MCP pattern

5.13.3.1 Example 1: PCIe4.0 Recovery EQ Phase1-TS1

1. On the **Pattern** tab forMU195020A, select **Sequence** in the Test Pattern box.
2. In the **Specification** box, select **PCIe4**.
3. To set 128b130b for the last block of the default sequence, touch **Sequence Edit**. Touch **File** → **Open** to load the following file:

   C:\Anritsu\MP1900A\AppServers\bin\Pattern Files\Sequence_Default\PCIe4

   PCIe4_RECOVERY_EQUALIZATION_PHASE1.ptn128b130b
4. Set **Manual** for Break of the added block.
5. Set “32” for EIEOS Interval of the added block.
6. Touch **OK**.
7. On the **Pattern** tab for MU195020A, touch **Transmit** to make the DUT to enter the Loopback.Active state.
   The DUT enters a state where it loops back the TS pattern of the PCIe4.0 Recovery EQ Phase1 state output by the MU195020A.
8. On the **Pattern** tab for MU195040A, select **HSSB Data** in the **Test Pattern** box.
9. In the **Specification** box, select **PCIe4**.
10. Touch **Edit** → **File** → **Open** to load the same pattern file loaded to MU195020A.

    C:\Anritsu\MP1900A\AppServers\bin\Pattern Files\Sequence_Default\PCIe4

    PCIe4_RECOVERY_EQUALIZATION_PHASE1.ptn128b130b
11. Set “32” for EIEOS Interval.
12. Touch **Start** to start BER measurement.

5

Operation Method

5.13.3.2 Example 2: PCIe4.0 MCP

Steps 1 and 2 are the same as Example 1 in Section 5.12.13.1.

3. No changes are required from the default sequence. The default sequence can be restored by one of the following procedures:
   - Touch Menu → **Initialize**.
   - In Sequence Editor, touch **File** → **Open** to load the following file:

     C:\Anritsu\MP1900A\AppServers\bin\Pattern Files\Sequence_Default\PCIe4

     dB-PCIe4_Default.seqpcie4
4. Touch **Transmit** to make the DUT to enter the Loopback.Active state. The DUT enters a state where it loops back the MCP pattern output by the MU195020A.
5. On the **Pattern** tab for MU195040A, select **Data** in the **Test Pattern** box.
6. Touch **Edit**. Touch **File** → **Open** to load the following pattern file:

   C:\Anritsu\MP1900A\AppServers\bin\Pattern Files\PCIe

   128b130b_MCP_L0_Gen4_SRIS_NOSKP.ptn
7. On the **Measurement** tab, under **SKP Ordered Set**, set Specification to **PCIe4** and set Filtering to **ON**.
8. Touch **Start** to start BER measurement.

5.13.4 Restrictions on SI PPG Sequence Editor and SI ED HSSB Data

This chapter explains new restrictions on MU195020A and MU195040A.

- To measure BER for PCIe1 and PCIe2, set SKP OS Symbol Length x2 to ON in the Sequence Editor of the MU195020A. This is to prevent the running disparity of the pattern from varying depending on where SKP Ordered Sets are inserted when SKP Ordered Set is inserted an odd number of times during BER measurement for PCIe.

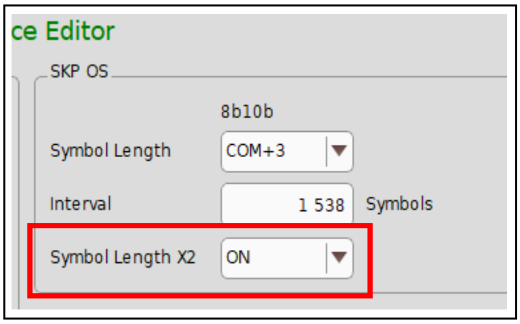


Figure 5.13.4-1 Setting for Symbol Length x2

- Combination, Channel Sync, and Grouping cannot be performed when **Sequence** is selected in the Test Pattern box on the **Pattern** tab for MU195020A.
- When **PCIe2**, **PCIe3**, or **PCIe4** is selected in the Specification box on the **Pattern** tab for MU195020A, the Error Addition function cannot be used for blocks with bitrate lower than the specified bitrate. The following table shows options available in the Specification box and their bitrates.

Table 5.13.4-1 Specification and Bitrate

Specification	Bitrate
PCIe2	5.0 Gbit/s
PCIe3	8.0 Gbit/s
PCIe4	16.0 Gbit/s

- When measuring BER, set EIEOS Interval of EIEOS/SYNCOS to be inserted to the same value as EIEOS Interval in the Sequence Editor screen of the MU195020A.

  In the following example, set EIEOS Interval to 32.

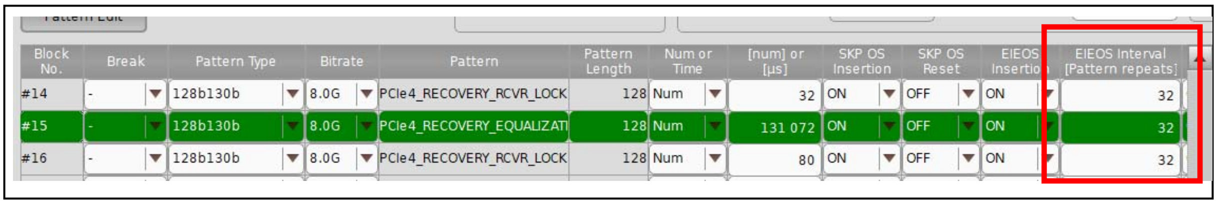


Figure 5.13.4-2 EIEOS Interval in the Sequence Editor Screen

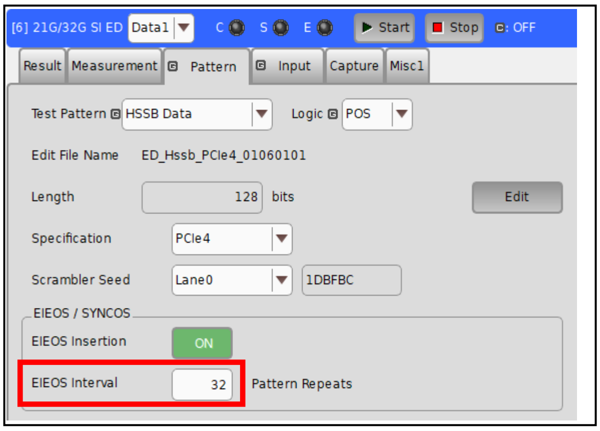


Figure 5.13.4-3 EIEOS Interval Setting for MU195040A

- To place the MU195040A in an error-free state when loading a 8b10b pattern file, perform one of the following:
  - On the **Input** tab of the MU195040A, adjust the Delay value.
- **HSSB Data** is available for Data1 only, not for Data2.
- BER of HSSB Data can be measured at the following bitrate only

Table 5.13.4-2 Bitrates at Which BER of HSSB Data Can Be Measured

Specification	Bitrate
PCIe1	2.5 Gbit/s
PCIe2	5.0 Gbit/s
PCIe3	8.0 Gbit/s
PCIe4	16.0 Gbit/s
USB3.0	5.0 Gbit/s
USB3.1 Gen2	10.0 Gbit/s

- **Combination** cannot be selected when on the **Pattern** tab of the MU195040A, **HSSB Data** is selected for MU195040A. Similarly, **HSSB Data** cannot be selected for Data2 when in the **Grouping** dialog box, Pattern is set to **ON**.
- **Eye Contour**, **Bathtub**, and **Eye Margin** cannot be used when on the **Pattern** tab of the MU195040A, **HSSB Data** is selected for Test Pattern.

5.14 Setting Input Interface

To set input interface, touch the **Input** tab on the MU195040A operation screen.

5.14.1 Input setting items

The **Input** tab consists of three areas: Data setting area, Clock setting area and Measurement Restart setting area.

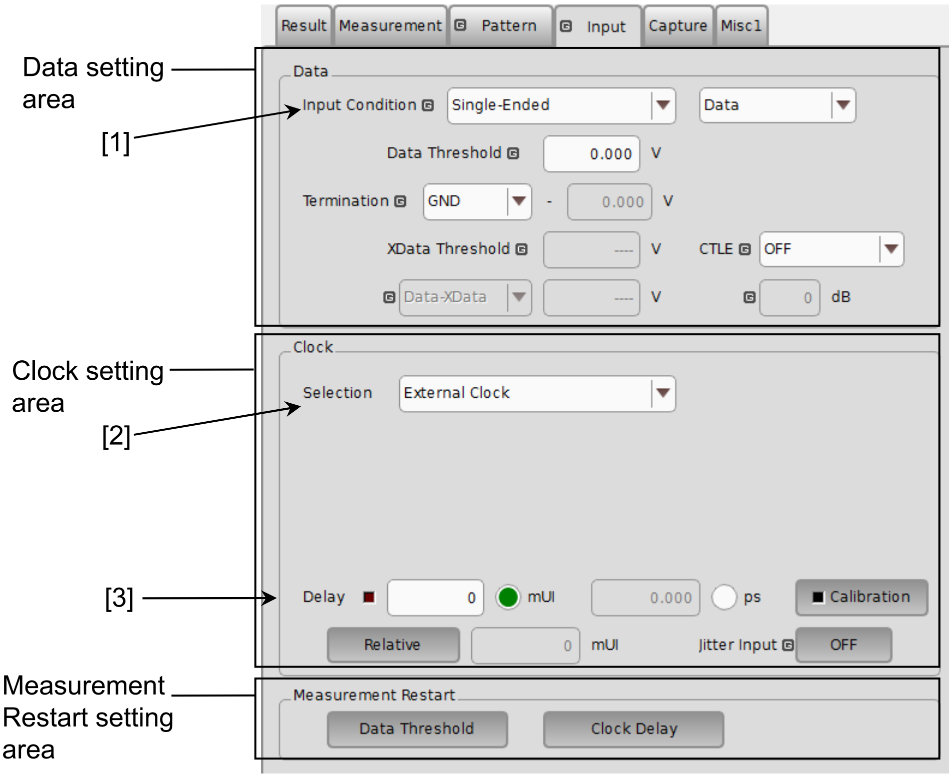


Figure 5.14.1-1 Input tab

1. Set the data input conditions.

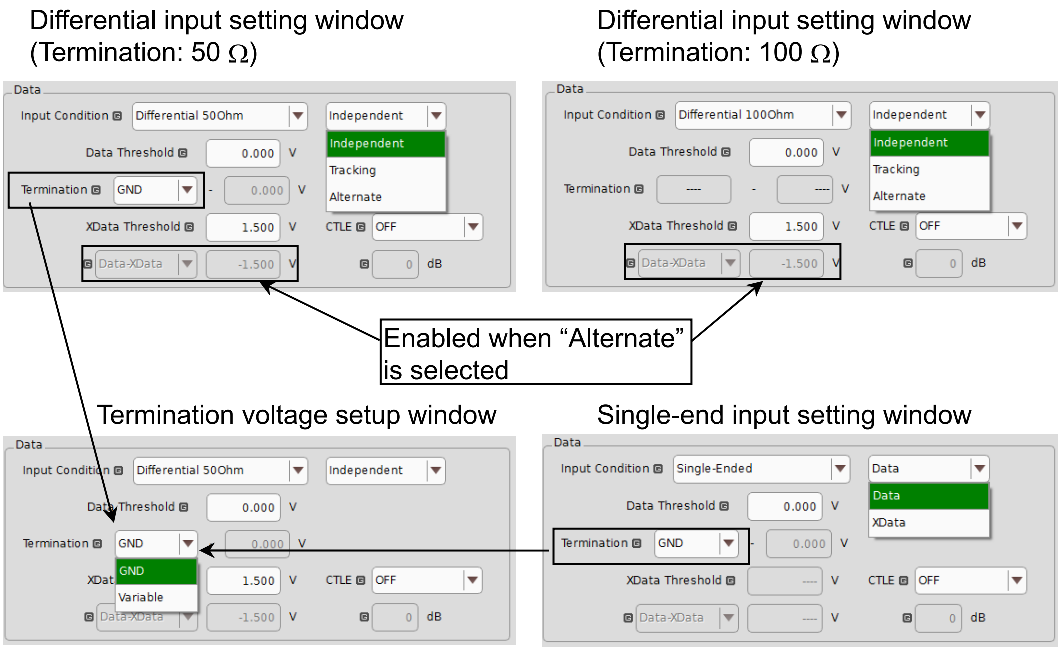


Figure 5.14.1-2 Setting Data input conditions

Table 5.14.1-1 Data input condition setting items (Input Condition)

Data input condition setting items			Description
Differential 100Ohm, Differential 50Ohm	Independent		Uses Data and XData as the differential input. Thresholds for Data and XData can be changed independently.
	Tracking		Uses Data and XData as the differential input. Thresholds for Data and XData can be changed while tracking each other.
	Alternate	Data-XData	Uses Data and XData as the differential input. The Data threshold and XData threshold can be changed interrelatedly, in conjunction with a difference between Data and XData (Data-XData).
		XData-Data	Uses Data and XData as the differential input. The Data threshold and XData threshold can be changed interrelatedly, in conjunction with a difference between XData and Data (XData-Data).
Single-Ended	Data		Used the Data side as single-ended input.
	XData		Used the XData side as single-ended input.

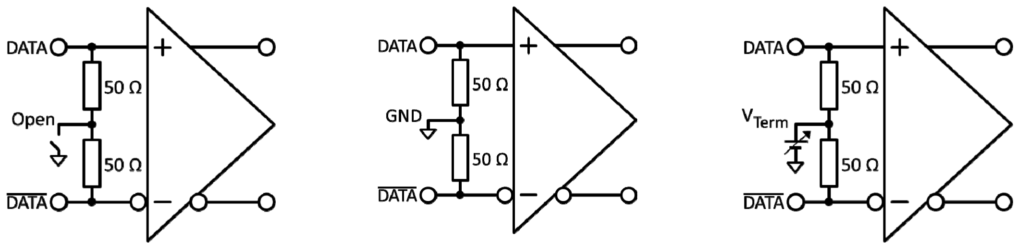
⚠ CAUTION

When data input condition is set to single-ended input, be sure to connect a standard accessory Open (J1341A) of Accessory to unused side of data input connector.

Operating while signal is inputting to unused side connector causes malfunction.

Table 5.14.1-2 Setting items in Data Termination Setting Dialog Box (Data Termination)

Data Termination Setting item		Description
Differential 100Ohm	None	Releases 50 Ω terminations of Data and XData sides from GND, and connects 50 Ω terminations so that the resistance between Data and XData becomes 100 Ω. For protection of equipment, the 50 Ω terminations at the Data and XData sides are fixed to the ground potential via a high resistor when input connectors are open.
Differential 50Ohm Single-Ended	GND	50 Ω terminations at the Data and XData sides are terminated to GND.
	Variable	Terminates to 50 Ω and an arbitrary set voltage within the range from –2.5 to +3.5 V. The voltage can be set in 10 mV steps.



Termination GND

Termination Variable

Differential 100 Ω

Differential 50 Ω / Single-Ended

Figure 5.14.1-3 Termination Methods in Different Setups

⚠ CAUTION

- **Do not allow an excessively large current to flow to the terminator in the MU195040A. Otherwise, performance may become degraded or failure may occur.**
- **If a differential signal is input via the Data or XData connector when Single-Ended is selected, the threshold margin becomes double.**

When the MU195040A-x11/x21 is installed, the CTLE (Continuous Time Linear Equalizer) band can be set. The range is as follows:

OFF, 8-10Gbit/s, 16-20Gbit/s, 25-28Gbit/s, PCIe3, PCIe4, PCIe5

When the CTLE is set to other than **OFF**, set the band in the range of Gain 0 to –12 dB, in 0.1 dB steps.

2. The installation of MU195040A-x22 allows you to select the clock source from the following: External Clock, Recovered Clock, and Clock and Data Recovery. If the option is not installed, this is fixed to **External Clock**.

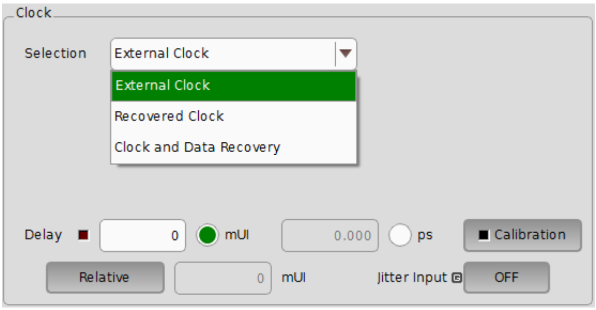


Figure 5.14.1-4 Clock setting area

If **Recovered Clock** or **Clock and Data Recovery** is selected when MU195040A-x22 is installed, the clock recovered from Data1 by built-in clock recovery circuit is used as system clock. **Recovered Clock** (Figure 5.14.1-5) allows Eye analyses such as Bathtub, Eye Margin, and Eye Contour using the recovered clock. **Clock and Data Recovery** (Figure 5.14.1-6) allows the BER measurement of the recovered data. Select this clock source to perform the BER measurement of stressed signals such as SSC, for it enables jitter or noise resistance test.

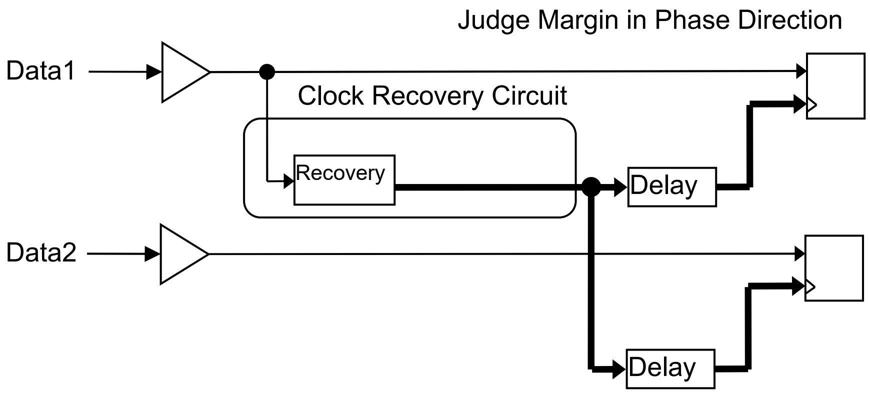


Figure 5.14.1-5 Recovered Clock Circuit

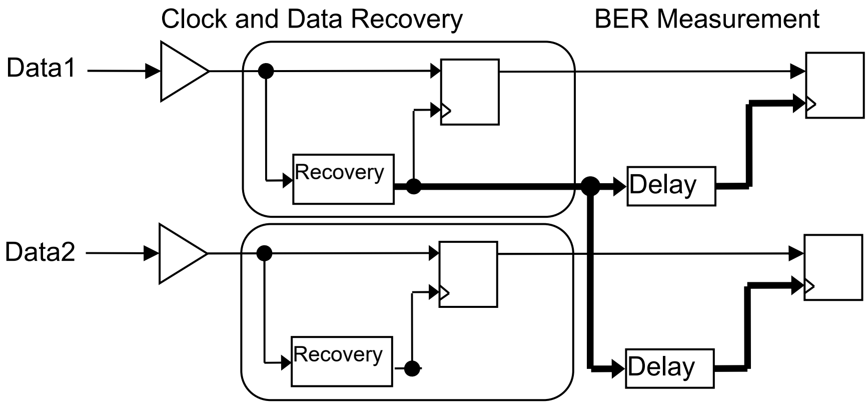


Figure 5.14.1-6 Clock and Data Recovery Circuit

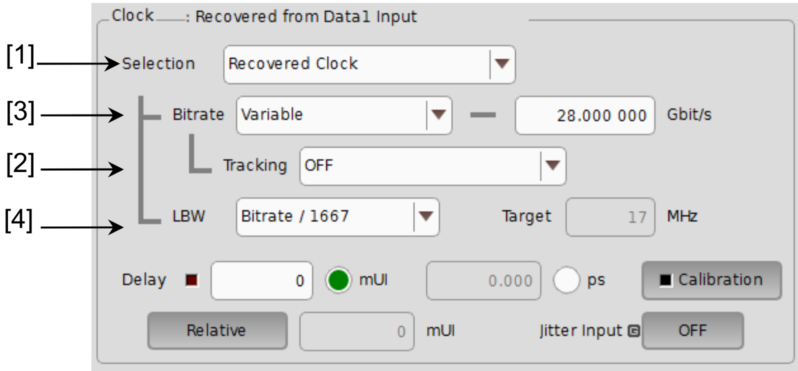


Figure 5.14.1-7　Clock setting area (When Recovered Clock Is Selected With MU195040A-x22 Installed)

[1]　Touch **External Clock**, **Recovered Clock**, or **Clock and Data Recovery**. **Recovered Clock** and **Clock and Data Recovery** are available only when MU195040A-x22 is installed on MU195040A. The setting items in the **Clock** area differ according to your option.

Note:

When your option is MU195040A-x22, check that the data signal is being input to the Data Input 1 connector because the clock is recovered from the data signal.

External clock and recovered clock have difference in waveform quality. So the following measurements may have inaccurate results.

- Sensitivity Measurement
- Phase Margin Measurement
- Eye Margin Measurement
- Bathtub Measurement
- PAM BER Measurement
- Eye Contour Measurement

When using output clock of MU195020A as external clock, the residual jitter is smaller compared with the case where recovered clock is used as external clock. Thus, the measurement result decrease due to clock quality is minimized.

When **Recovered Clock** is selected, SSC-modulated data may not be measured properly. When inputting SSC-modulated data into the MU195040A for stress input tests of PCI Express, USB3.1, and Thunderbolt receivers, etc., select **External Clock** or **Clock and Data Recovery**.

[2] When selecting the MU195020A mounted on the same MP1900A, the recovered clock tracks MU195020A's operation bit rate setting.

Note:

When the bit rate setting of the MU195020A is out of the operating range of the Clock Recovery option, the bit rate of the recovery clock will be set to the upper or lower limit of the operating range.

[3] In the **Bitrate** box, touch one of the preset standards listed in the following tables or touch **Variable**. When touching **Variable**, enter the bit rate in the **Gbit/s** box according to the input signal.

Table 5.14.1-3 When the MU195040A-x22 Is Installed

Preset Standard	Bit rate [Gbit/s]
OC-48/STM-16	2.488320
PCIe 1	2.500000
InfiniBand SDR	2.500000
OTU1	2.666060
DisplayPort HBR	2.700000
SATA 3Gb/s	3.000000
XAUI	3.125000
4G FC	4.250000
USB3.0	5.000000
InfiniBand DDR	5.000000
PCIe 2	5.000000
DisplayPort HBR2	5.400000
SATA 6Gb/s	6.000000
HSBI	6.250000
PCIe 3	8.000000
DisplayPort HBR3	8.100000
8G FC	8.500000
OC-192/STM-64	9.953280
USB3.1 Gen2	10.000000
USB4 Gen2	10.000000
DisplayPort UHBR 10	10.000000
InfiniBand QDR	10.000000
Thunderbolt1	10.312500
10GbE	10.312500
10G FC	10.518750
G975 FEC	10.664228
OTU2	10.709225
10GbE over FEC	11.095700
10GFC over FEC	11.316800
SAS3	12.000000
DisplayPort UHBR 13.5	13.500000
16G FC	14.025000
InfiniBand FDR	14.062500
PCIe 4	16.000000
Thunderbolt2	20.625000
PCIe 4	16.000000
USB4 Gen3	20.000000
DisplayPort UHBR 20	20.000000

Table 5.14.1-4 When the MU195040A-x22 Is Installed (Cont’d)

Preset Standard	Bit rate [Gbit/s]
Thunderbolt2	20.625000
SAS4	22.500000*
SAS	24.000000*
InfiniBand EDR	25.781250*
100GbE(25.78x4)	25.781250*
100G OTU4	27.952496*
32G FC	28.050000*
PCIe 5	32.000000*
100G ULH	32.100000*
Variable	2.400000 to 21.000000 Gbit/s 2.400000 to 32.100000 Gbit/s*

*: Available only when MU195040A-x01 is installed.

[4] You can select a loop band (Loop band width).
When **Variable** is touched in the **LBW** box, you can set a loop band in the range that corresponds to the bit rate.

Operation Bitrate [Gbit/s]	Range [MHz] (Step: 1 MHz)
2.400000 to 5.500000	Fixed to 3 MHz
5.500001 to 7.500000	3 to 4 MHz
7.500001 to 9.500000	3 to 5 MHz
9.500001 to 10.500000	3 to 6 MHz
10.500001 to 12.500000	3 to 7 MHz
12.500001 to 14.500000	3 to 8 MHz
14.500001 to 15.500000	3 to 9 MHz
15.500001 to 17.500000	3 to 10 MHz
17.500001 to 19.500000	3 to 11 MHz
19.500001 to 20.500000	3 to 12 MHz
20.500001 to 22.500000	3 to 13 MHz
22.500001 to 24.500000	3 to 14 MHz
24.500001 to 25.500000	3 to 15 MHz
25.500001 to 27.500000	3 to 16 MHz
27.500001 to 29.500000	3 to 17 MHz
29.500001 to 31.500000	11 to 18 MHz
31.500001 to 32.100000	11 to 19 MHz

When **Bitrate/1667** or **Bitrate/2578** is selected in the **LBW** box, the value obtained by the following formula will be set: (Bitrate/1667 or 2578) MHz.
When **Jitter Tolerance** is touched, the loop band is set to the maximum value for the Jitter Tolerance measurement.

3. MU195040A can vary delay time of clock output.

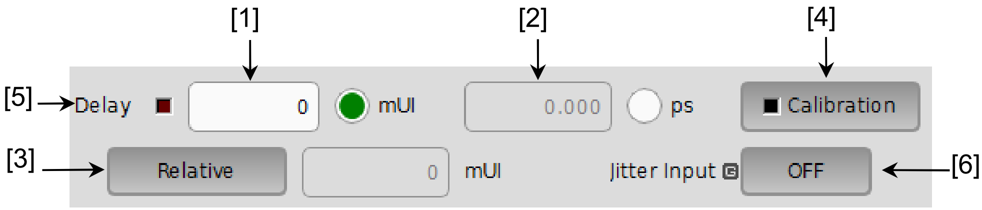


Figure 5.14.1-8 Clock delay setting items

[1] Touch this radio button to set the clock delay in 2 mUI units. The MU195040A operates based on the UI units. Setting a greater value increases the clock delay.

[2] Delay time can be set by ps unit. The frequency counter value is converted into ps units, based on the 2 mUI units. If the value read from the frequency counter is out of the range, "----ps" is displayed.

[3] When **Relative** is touched and green, the text box on the right becomes enabled. The clock delay can be set in this text box by a relative value in 2 mUI units, based on the current delay as 0 mUI. When **Relative** is touched again to be gray, the clock delay is calculated from the set relative value and set.

[4] Touching **Calibration** starts a short-time self-calibration. When the LED on the Calculation button glows red, it indicates that calibration should be performed. When it glows green, it indicates that the operation is normal and calibration is not required. Note that the delay fluctuates greatly during calibration.

[5] This LED glows red while the "Delay" is being changed.

[6] Set the jitter input. When executing jitter tolerance test by inputting jitter-modulated clock, set **Jitter Input** of Delay to **ON**. Refer to 5.11.7 "When inputting jitter-modulated signals".

Notes:

- When the frequency or the temperature condition is changed, the LED on the "Calibration" lights, prompting performance of calibration. If calibration is not performed at this time, the error in the phase setting may be greater than at a normal phase setting.

- Values displayed in ps units vary as the bit rate changes, because the MU195040A sets phases in mUI units as an internal standard.

- When setting **Pattern Sequence** to **Burst** on the **Misc1** tab, the phase setting is less accurate than it is when setting to **Repeat**.

- During Auto Adjust execution, the delay amount of **Delay** is always changed in order to drive the clock phase to the optimum point. Therefore, the LEDs of **Delay** and **Calibration** light up in red continuously. This is not abnormal.

Refer to 5.11.7 “When inputting jitter-modulated signals” for operation and precautions in case of Combination or inputting jitter-modulated signals.

5.14.2 Measurement Restart area

The items to restart the measurement when its setting is changed can be selected.

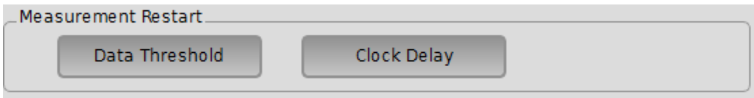


Figure 5.14.2-1 Selecting measurement restart item

Table 5.14.2-1 Items in Measurement Restart area

Setting item	Description
Data Threshold	Measurement is restarted when the Data/XData Threshold on the **Input** tab is changed.
Clock Delay	Measurement is restarted when Delay on the **Input** tab is changed.

5.15 Capturing Test Patterns

To capture the input test pattern data, touch the **Capture** tab on the MU195040A operation screen.

5.15.1 Setting items on the Capture tab

This section describes how to capture and analyze a test pattern on the Capture tab.

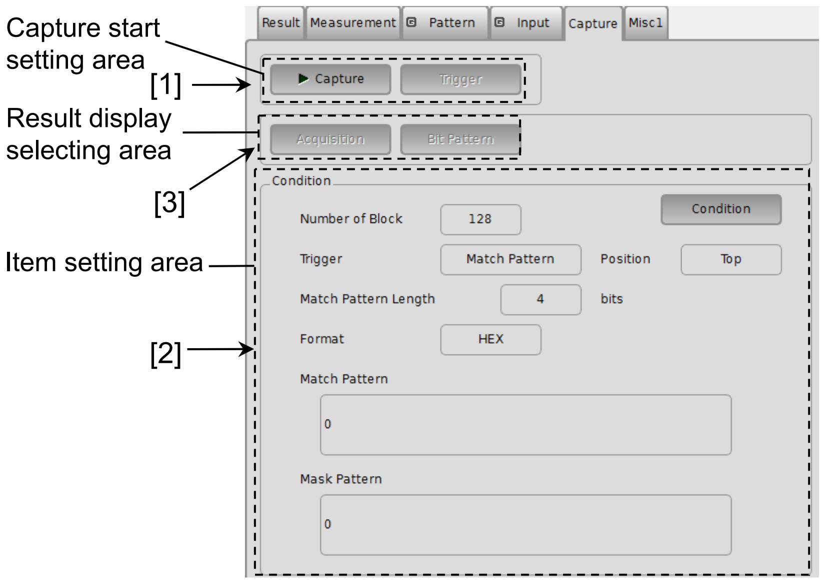


Figure 5.15.1-1 Capture tab

1. Start capturing of a test pattern. Manual trigger can be executed when **Manual** is selected from the **Trigger** list box in the **Condition Setting** dialog box.

Note:

Capture cannot be executed in the following settings.

- **Pattern Sequence** of **Misc1** tab is set to **Burst**, or **Sync Control** is set to **Quick**.
- Sync Loss is generated in BER measurement.
- Capture has been already executed by other data interface.

Figure 5.15.1-2 Buttons in capture start setting area

Table 5.15.1-1 Capture/Trigger buttons

Buttons	Description
Capture	Starts capturing a test pattern. Its LED turns green during test pattern capturing. The MU195040A enters and stays in the standby state until the trigger conditions match. When the trigger conditions match and the test pattern has been captured into the internal memory, the capturing operation is stopped and the LED on **Capture** turns off.
Trigger	When **Manual** is selected from the **Trigger** list box in the **Condition Setting** dialog box, test pattern capturing can be started manually by touching this button (manual trigger).

2. When **Condition** in the item setting area is touched, the **Condition Setting** dialog box is displayed. Be sure to set the trigger conditions before starting test pattern capturing. When the trigger conditions are set, touch **OK** to apply the set conditions. When **Cancel** is touched instead, the set conditions are canceled and the **Condition Setting** dialog box is closed.

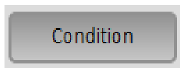


Figure 5.15.1-3 Condition button in item setting area

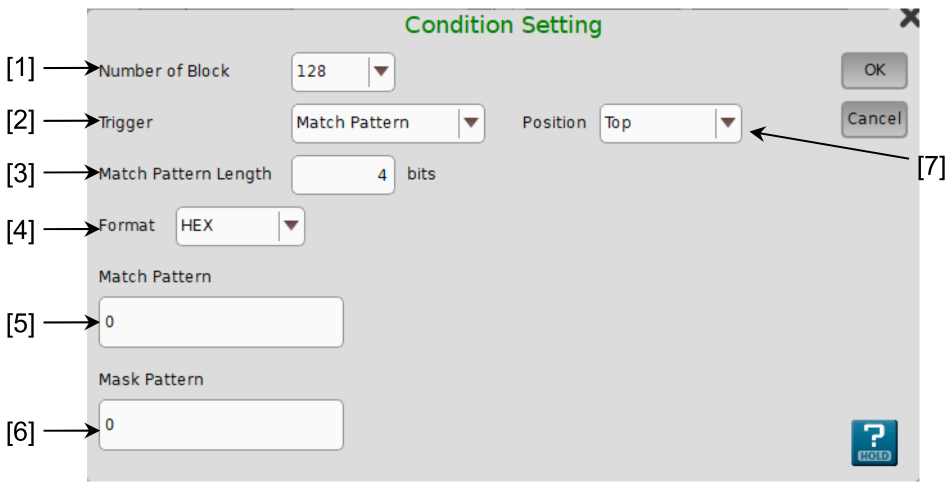


Figure 5.15.1-4 Condition Setting Dialog Box

[1] Select the number of blocks of the test pattern to be captured into the MU195040A, from 1, 2, 4, 8, 16, 32, 64, or 128. The size of each block to be captured can be calculated from the following expression:

Block size = 8 Mbits / Number of Block

[2] Select the type of the trigger to capture the test pattern.

Table 5.15.1-2 Trigger setting

Item	Description
Error Detect	Capturing starts when an error is detected.
Match Pattern	Capturing starts when a pattern that matches the set specific pattern is detected.
Manual	Capturing of one block starts when **Trigger** in the capture start setting area (refer to Figure 5.15.1-2) is touched. To perform capturing for all the blocks, touch **Trigger** for the number of times equal to the number of blocks set from the Number of Block list box in the **Condition Setting** dialog box.
External	Capturing starts at the falling edge of the signal input to the AUX Input connector.

[3] Set the length of the pattern used for match detection from 4 to 64 bits, in 4-bit units. This is enabled when **Match Pattern** is selected from the **Trigger** list box.

[4] Select the display format of the pattern used for match detection. This is enabled when **Match Pattern** is selected from the **Trigger** list box.

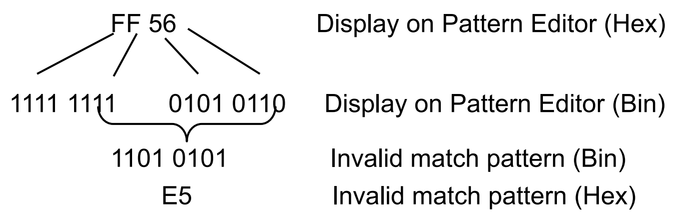
Table 5.15.1-3 Format setting

Item	Description
BIN	The match pattern is displayed in binary format.
HEX	The match pattern is displayed in hexadecimal format.

[5] Set the pattern used for match detection when **Match Pattern** is selected for **Trigger**.

Note:

When setting a match pattern while the 2Ch Combination is configured, set it in 4-bit units, as displayed in the **Pattern Editor** dialog box of the MU195040A in hexadecimal. If the match pattern that is displayed in hexadecimal format crosses bit boundaries, it becomes invalid and cannot be captured.



[6] Set the bits to be masked in the pattern used for match detection. To mask a bit for match detection, set “1” for that bit. This is enabled when **Match Pattern** is selected from the **Trigger** list box.

[7] Set the capturing start position based on the trigger position.

Table 5.15.1-4 Capture start position setting

Item	Description
Top	Captures a test pattern after the trigger position.
Middle	Captures a test pattern around the trigger position.
Bottom	Captures a test pattern before the trigger position.

3. The capture result display format can be specified using the buttons in the result display selecting area.

Figure 5.15.1-5 Buttons in result display selecting area for selecting capture result display format

Table 5.15.1-5 Buttons for selecting capture result display format

Button	Description
Acquisition	Touch to open the **Capture Acquisition** dialog box to acquire the results of capturing a test pattern to the MU195040A. The captured results can be viewed in three display formats: Bit Pattern, Bitmap, and Block. When **Acquisition** is touched and the test pattern capture results are acquired, **Bit Pattern**, **Bitmap**, and **Block** on the right become available and the display format can be switched.
Bit Pattern	The captured test pattern is displayed in a bit pattern string, so that Insertion Error and Omission Error can be distinguished.

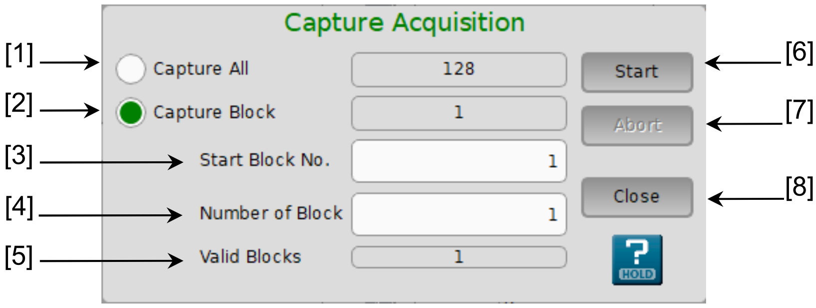


Figure 5.15.1-6 Capture Acquisition Dialog Box

[1] Select to display all the captured blocks.

[2] Select to display the specified captured blocks only.

[3] Specify the block number to be displayed first (**Start Block No.**).

[4] Specify the number of blocks to be displayed following the **Start Block No.** specified in [3].

[5] Displays the number of blocks that have been captured.

[6] Touch **Start** to start loading the captured data of the blocks specified in Step [1] to [4]. The loading time depends on the number of blocks.

[7] Touch **Abort** to abort loading the captured data. When aborted, the block results that are already loaded can be displayed.

[8] Touch **Close** to close the screen.

5.15.2 Displaying captured test pattern (Bit Pattern)

After the captured data is acquired by touching **Acquisition**, touching **Bit Pattern** (refer to Figure 5.15.1-5) displays the Bit Pattern window. In this window, the captured test patterns are displayed in a bit pattern string so that Insertion Error and Omission Error can be distinguished.

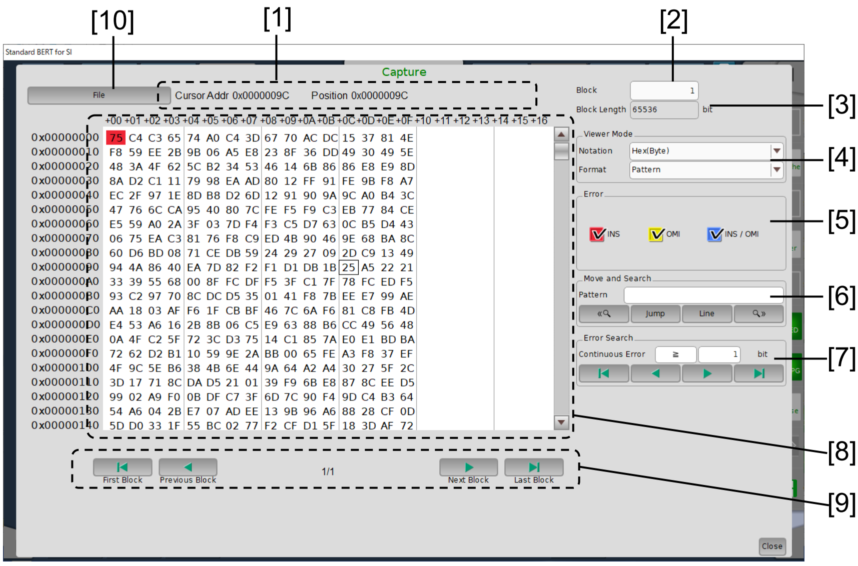


Figure 5.15.2-1 Bit Pattern window

Note:

The bit pattern display is based on the positive logic, with H = “1” and L = “0”.

Table 5.15.2-1 Description of Screen Items

No.	Item	Description
[1]	Cursor Addr/ Position	Cursor Addr: Displays the cursor position within the current block. Position: Displays the position within the entire captured data (all blocks).
[2]	Block	Sets the block number to display.
[3]	Block Length	Displays the block length. Block Length = 8M bits/ Number of Block
[4]	Viewer Mode	Notation: Bin Hex(Byte) Format: Select a view mode of the Capture Data display area. Pattern: String of binary (0, 1) or hexadecimal (0 to 9, A to F) numbers Pattern + Waveform: String of binary (0, 1) numbers and image of NRZ signal

Table 5.15.2-1 Description of Screen Items (Cont'd)

No.	Item	Description
[5]	Error	Displays the legend (color sample) for each of error bits. INS: Insertion Error (0 → 1) Red OMI: Omission Error (1 → 0) Yellow INS / OMI: Insertion and Omission Error Blue ***Note:*** The captured results are displayed as a bit pattern. The MU195040A reference pattern is displayed in binary (0, 1) or hexadecimal (0 to 9, A to F), and its background color depends on the error type. Bits where no error occurred are displayed without background color. To show/hide each error in the Capture Data display area, select/clear its check box.
[6]	Move and Search	Searches for the string specified by binary (0, 1) or hexadecimal (0 to 9, A to F) numbers from the captured data. Pattern: Searches any pattern using and . Jump: Move the cursor to the specified address or pattern. Head: Moves the cursor to the head of the captured data pattern. Tail: Moves the cursor to the tail of the captured data pattern. Address: Moves the cursor to the specified address position. Forward Next: Searches forward for a pattern that matches the pattern set in the **Pattern** box. If found, the cursor is placed at the position. Backward Next: Searches backward for a pattern that matches the pattern set in the **Pattern** box. If found, the cursor is placed at the position. Line: Sets how many characters to display per line, in the Capture Data display area.
[7]	Error Search	Performs an error search, specifying the number and type of continuous errors. Continuous Error: Specifies the number of continuous errors to search for. 1 to 256 bits, 1-bit step In the **Search Condition** box, select **=** (Exact match) or ≥ (Greater than or equal to).
[8]	Capture Data display area	Displays the captured results (including error information) by binary (0, 1) or hexadecimal (0 to 9, A to F) numbers. The background colors of bits where errors occurred depend on the error types. When displayed in binary format, select **Pattern + Waveform** in the **Notation** list of the **Viewer Mode** area, and you will view a pattern image.

Table 5.15.2-1 Description of Screen Items (Cont'd)

No.	Item	Description
[9]	Block scroll buttons	Scrolls the block view.
[10]	File	Saves the captured results and pattern data to a file. Also, opens the saved pattern data file. Save: Saves the captured results and pattern to a file. The available file types are as follows: Binary, BIN Text, HEX Text: Select when redisplaying the results in the Bit Pattern window. Binary(export), BIN Text(export), HEX Text(export): Select when saving a pattern file including error information. The saved file can be loaded by Pattern Editor of the PPG and ED. Open: Loads the saved captured result data (Binary, BIN Text, HEX Text) to display the results.

5.16 Misc1 Function (MU195040A)

Pattern sequence and auxiliary input and output can be set by the Misc1 function.

On the **Misc1** tab of the MU195040A operation window, you can set the Misc1 function.

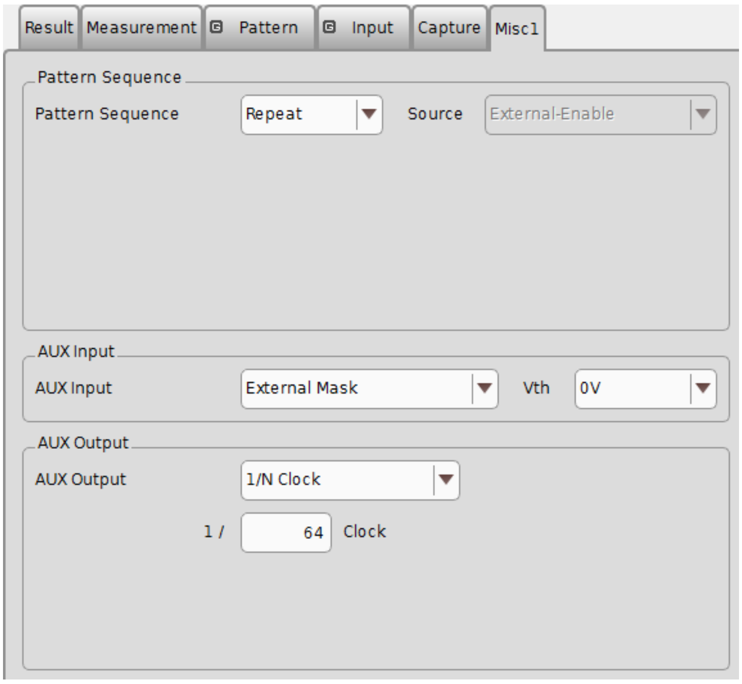


Figure 5.16-1 Misc1 tab

Table 5.16-1 Misc1 setting items

Item	Description
Pattern Sequence	Test pattern receiving method can be set.
AUX Input	The settings for the auxiliary input function can be configured.
AUX Output	The settings for the auxiliary output function can be configured.

Note:

AUX Input settings are common to Data1 and Data2 at MU195040A-x20.

5.16.1 Setting Pattern Sequence

Select the method for generating test patterns to be measured.

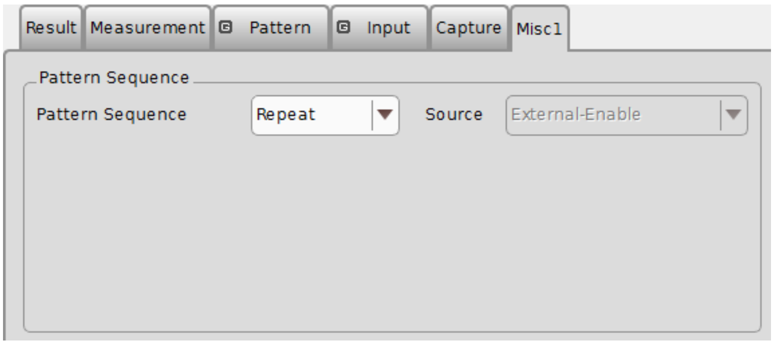


Figure 5.16.1-1 Selecting pattern sequence

Table 5.16.1-1 Selecting pattern sequence

Selection item	Description
Repeat	Select when receiving Repeat data of the test pattern. Mainly used for electric device evaluation.
Burst	Select when receiving Burst data of the test pattern. Mainly used for long-distance optical transmission tests such as an optical circulating loop test, and packet communications evaluation. The target test patterns are PRBS, ZeroSubstitution, Data, and Mixed.

5.16.1.1 Setting Repeat pattern

Select **Repeat** from the **Pattern Sequence** list box to receive Repeat data of the test pattern. No setting items are required.

5.16.1.2 Setting Burst pattern

Select **Burst** from the **Pattern Sequence** list box to receive Burst data of the test pattern.

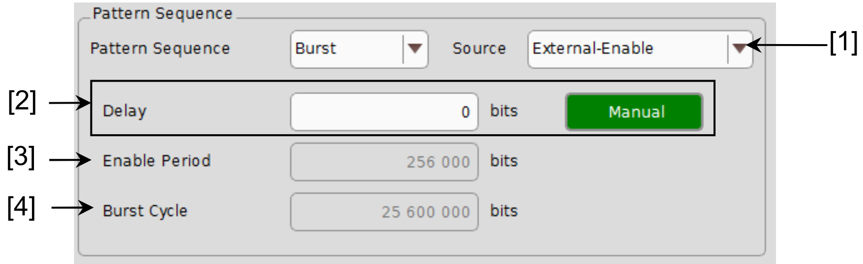


Figure 5.16.1.2-1 Pattern Sequence area when Burst is selected

[1] Select the definition method for the switching timing between the input test pattern valid period and invalid period.

Table 5.16.1.2-1 Burst setting items

Setting item	Description
Internal*	Select this item when setting the gate signal that determines the measuring period of the intermittently-input test pattern within the MU195040A, instead of inputting it from external equipment. Select this item when the input signal valid period and the repetition cycle are known.
External-Trigger*	Select this item when defining the start timing of the input test pattern valid period. The length of the valid period can be set by the Enable Period text box (refer to [3] below).
External-Enable	Select this item when defining the start timing and the length of the input test pattern valid period.

*: When the test patterns of Burst Cycle and Enable Period are not constant, select **External-Enable**.

[2] Set the **Delay** for the input test pattern and source signal (selected by [1]). When **Auto** is selected, the delay is automatically adjusted within the MU195040A.

When having chosen **Auto** and Enable Period of [3] is changed, operate **Manual** → **Auto** once.

When **Manual** is selected, set the number of relative delay bits used in the MU195040A. At this time, the signal input from the AUX Input connector indicates the period during which the test pattern is valid.

The setting range is as follows.

In the case of Independent:
0 to 2 147 483 640 bits, 8 bit step
In the case of 2ch Combination:
0 to 4 294 967 280 bits, 16 bit step

[3] When **External-Trigger** or **Internal** is selected from the **Source** list box, specify the period during which Burst cycle signals of the test pattern to be input to the AUX Input connector are continuously generated by the number of bits.

The setting ranges for Enable Period are shown in Table 5.16.1.2-2.

[4] When **Internal** is selected from the **Source** list box, set the Burst cycle (one cycle of the Burst signal of the input test pattern).
The setting ranges for Burst Cycle are shown in Table 5.16.1.2-2.

Table 5.16.1.2-2 Setting ranges for Enable Period and Burst Cycle

No. of Channel Combinations	Enable Period (bits)	Burst Cycle (bits)	Setting Steps (bits)
1	When **Internal** is set: 12800 to 2147482624	25600 to 2147483648	256
	When **External-Trigger** is set: 12800 to 2147483392		
2	When **Internal** is set: 25600 to 4294965248	51200 to 4294967296	512
	When **External-Trigger** is set: 25600 to 4294966784		

Notes:

- A Disable period of at least 512 bits is required between Burst Cycle and Enable Period.
  The Disable period is doubled at 2ch Combination.

- When **Auto** is selected for the delay setting, set **Sync Control** to **Frame ON**.
  If any of the following items is changed when **Auto** is selected for the delay setting, change the delay setting to **Manual** and set to **Auto** again.
  - **Burst Cycle** or **Enable Period** of the test pattern
  - **Burst Cycle** when **External - Trigger** is selected
  - **Burst Cycle** or **Enable Period** when **External - Enable** is selected

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Operation Method

5.16.2 Setting AUX Input Setting AUX Input

Set the use of timing signal to input the AUX Input connector.

Input signal to the AUX Input connector can be used for synchronizing the timing of receiving Burst signal.

The setting items for AUX Input are shown in the table below.

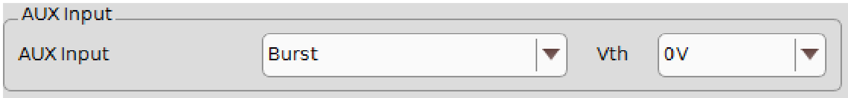

Figure 5.16.2-1 Selecting auxiliary input

Table 5.16.2-1 AUX Input setting items

Setting item	Description
Burst	Select when **Burst** is selected from the **Pattern Sequence** list box, and **External-Trigger** or **External Enable** is selected from the **Source** list box. External-Trigger: Data is valid for the set Enable period after a rising edge is detected. External-Enable: Data is valid when the level of the signal is high.
External Mask	Measurement is masked when a low-level signal is input.
Capture External Trigger	Inputs the Capture start trigger when set to **External**.
Vth	Select input threshold from 0V, –0.25V, or –0.5V.

5.16.3 Setting AUX Output

The output settings of auxiliary signals, such as the synchronization signal, can be configured.

5.16.3.1 Setting 1/N Clock

When **AUX Output** is set to **1/N Clock**, frequency dividing clock is generated in synchronization with generation pattern.

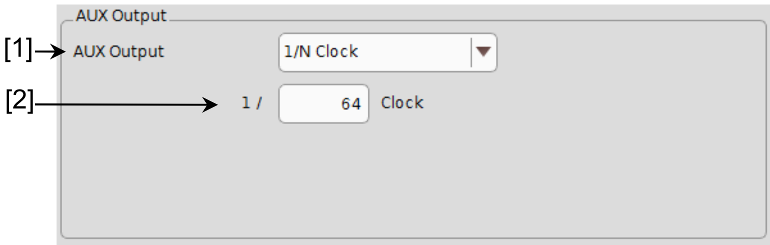

Figure 5.16.3.1-1 Setting items for AUX Output Clock

[1] Select **1/N Clock** from the **AUX Output** list box.

[2] The division ratio for the synchronization clock can be set.
The setting division ratio (N) can be set from 4 to 512, in even numbers.

5.16.3.2 Setting Pattern Sync

When **AUX Output** is set to **Pattern Sync**, a timing signal from the AUX Output connector is generated in synchronization with the test pattern period.

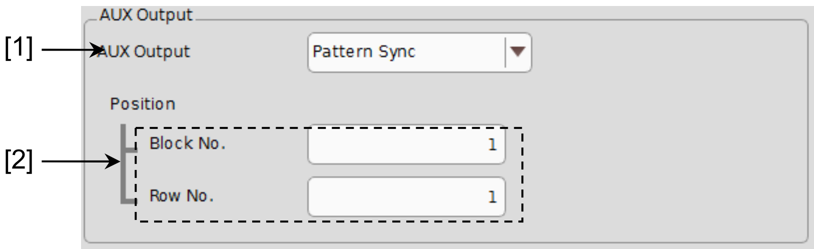

Figure 5.16.3.2-1 AUX Output Pattern Sync Setting Items

[1] Select **Pattern Sync** from the **AUX Output** list box.

[2] The synchronization signal pulse generation position can be set.
The setting method varies depending on the test pattern.

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Operation Method

Table 5.16.3.2-1 Synchronization signal pulse generation position setting

Test pattern	Description
PRBS, Data, ZeroSubstitution	A signal pulse is generated in a pattern period. The pulse position can be specified within the range below, starting from the beginning of the pattern. 1 to {(Least common multiple of Pattern Length* and 128) – 135}, in 8-bit steps. The maximum settable number is 34359738105. In the case of 2ch Combination: 1 to {(Least common multiple of Pattern Length* and 128) – 271}, in 16-bit steps. The maximum settable number is 68719476209.
Mixed	A signal pulse is generated during the entire block generation pattern period. The pulse position can be specified in the positions of Block and Row.

*: The pattern length described here is the number multiplied by an integer so that it becomes 512 bits or more, when the length on the Figure 5.13-1 Pattern tab is 511 bit or less.

At 2ch Combination, the pattern length described here is the number multiplied by an integer so that it becomes 1024 or more, when the length on the Figure 5.13-1 Pattern tab is 1023 or less.

5.16.3.3 Setting Sync Gain

A signal indicating synchronization establishment can be output. When this signal is high, it indicates that synchronization is established.

5.16.3.4 Setting Error Output

A signal indicating MU195040A has detected an error is output to the AUX Output connector. No setting items are required.
When the voltage of the AUX Output connector is high, it indicates that an error is detected.

5.17 Auto Search Function

The Auto Search function is used to optimize the threshold voltage and phase for the input data.

To display Auto Search setting items, touch **Auto Search** on the top right of the screen.

The Auto Search function optimizes the threshold voltage, and phase delay of the Data and XData input signals.

Figure 5.17-1 Auto Search

Note:

When grouping the **Input** tab, Auto Search cannot be executed.

5.17.1 Input setting items in Auto Search dialog box

The **Auto Search** dialog box consists of the Auto Search operation setting area (upper of the dialog box, including [1], [2], [4], [5] and [7] in Figure 5.17.1-1 below), operation target slot and result display area (lower left of the dialog box, indicated by [3] and [6] in Figure 5.17.1-1).

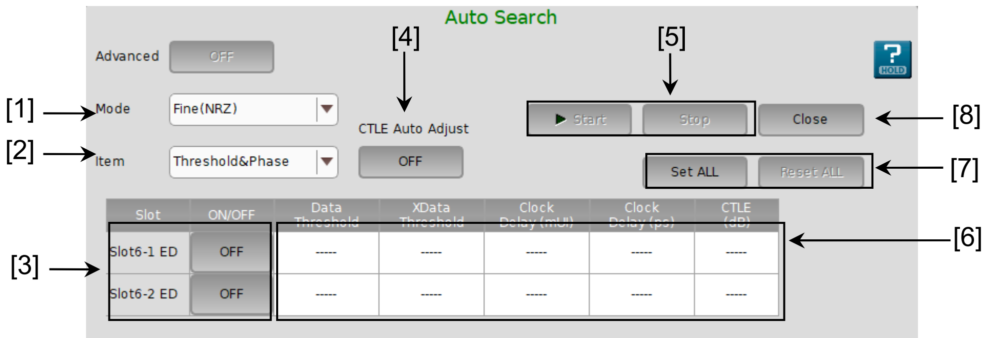


Figure 5.17.1-1 Auto Search Dialog Box

Advanced is not available for MU195040A.

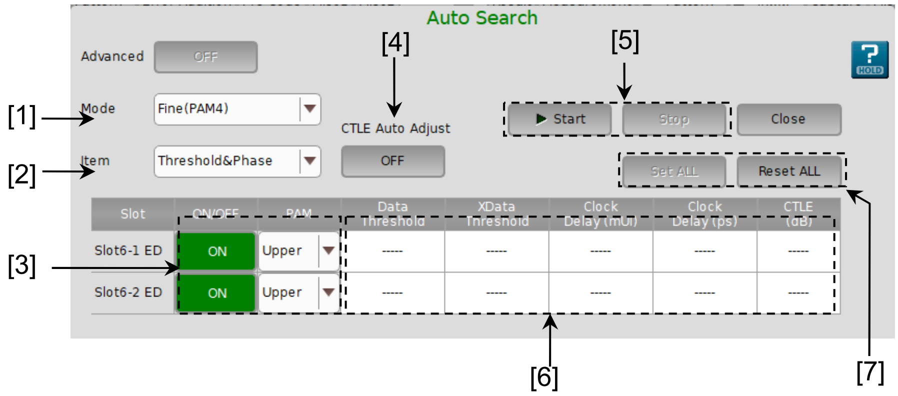


Figure 5.17.1-2 Auto Search Dialog Box (PAM mode)

[1] Select the Auto Search execution method from the **Mode** list box.

Table 5.17.1-1 Execution method setting

Mode	Description
Coarse (NRZ)	Coarse adjustment is executed by the hardware. Adjustment will be finished faster than by **Fine (NRZ)** adjustment. The obtained result will be almost the same as that after the Auto Adjust function is executed and finished.
Fine (NRZ)	In addition to coarse adjustment by the hardware, fine adjustment is executed with a software algorithm. It takes longer to finish the adjustment compared to **Coarse (NRZ)** adjustment.
Coarse (PAM4)	Searches for an optimum threshold point of each level (Top, Middle, Bottom) of PAM4 (Pulse-Amplitude Modulation) waveforms by detecting High and Low levels of the waveforms input.
Fine (PAM4)	Performs fine adjustment by software algorithm in addition to auto search in **Coarse (PAM4)** mode. It takes longer to finish the adjustment compared to **Coarse (PAM4)** adjustment.

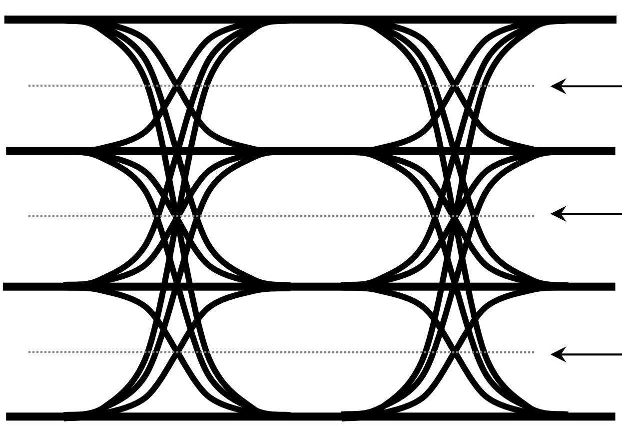


Figure 5.17.1-3 Vth image of PAM4 waveform

[2] Select the Auto Search target item from the **Item** list box.

Table 5.17.1-2 Execution target setting

Item	Description
Threshold&Phase	Auto Search is executed for both Threshold and Phase.
Threshold	Auto Search is executed for Threshold.
Phase	Auto Search is executed for Phase.

[3] Turn **ON** the button of interface on which Auto Search is executed. When **PAM Coarse** or **PAM Fine** is selected in the **Mode** list box, select a level (**Top**, **Middle**, or **Bottom**) of the PAM waveform to search.

[4] This is available when CTLE is set to other than **OFF** on the **Input** tab.
When set to **ON**, the gain of CTLE is searched.

[5] Touch **Start** to start Auto Search on the slot(s) whose buttons are turned **ON**. Auto Search can be started when a button or more are turned **ON**. Touching **Stop** stops Auto Search.

[6] Auto Search results are displayed.

Table 5.17.1-3 Result display items

Displayed result	Description
----	Indicates items for which Auto Search is not executed.
Failed	Indicates items for which Auto Search has failed.
XXXX mV	Indicates the result of Data/XData Threshold Auto Search in mV units.
XXXX mUI	Indicates the result of Phase Auto Search in mUI units.
XXXX ps	Indicates the result of Phase Auto Search in ps units. Data Delay in ps units is converted from that in mUI units, using the frequency counter value.

[7] Touch **Set All** to turn **ON** all slot buttons.
Touch **Reset All** to turn **OFF** all slot buttons.

[8] Touching **Close** closes the **Auto Search** dialog box. The **Close** becomes disabled during Auto Search.

5.18 Auto Adjust Function

The Auto Adjust function automatically adjusts the threshold voltage and phase to the optimum values when the interface conditions for the signals to be input to the MU195040A have changed.
To display the Auto Adjust setting items, touch **Auto Adjust** on the menu. Start or stop Auto Adjust by operating this button.

Figure 5.18-1 Auto Adjust

Note:

When grouping the **Input** tab, Auto Adjust cannot be executed.

5.18.1 Input setting items in Auto Adjust dialog box

The **Auto Adjust** dialog box consists of the Auto Adjust operation setting area (upper of the dialog box, including [1], [3], and [4] in Figure 5.18.1-1 below) and operation target slot setting area (lower of the dialog box, indicated by "[2]" in Figure 5.18.1-1).

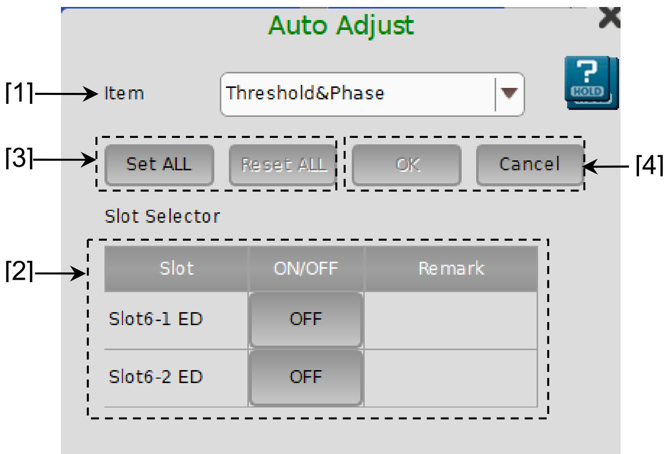


Figure 5.18.1-1 Auto Adjust Dialog Box

[1] Select the Auto Adjust target item from the **Item** list box.

Table 5.18.1-1 Execution target setting

Item	Description
Threshold&Phase	Auto Adjust is executed for both Threshold and Phase. Threshold and Delay in **Input** tab of Table 5.14.1-1 cannot be changed during Auto Adjust.
Threshold	Auto Adjust is executed for Threshold. Threshold in **Input** tab of Table 5.14.1-1 cannot be changed during Auto Adjust.
Phase	Auto Adjust is executed for Phase. Delay in Input tab of Table 5.14.1-1 cannot be changed during Auto Adjust.

[2] Turn **ON** the slot number(s) to be targeted for Auto Adjust in the **Slot** list. In case of MU195040A-x20, turn **ON** the channel number(s).

[3] Touch **Set ALL** to turn **ON** all slot buttons.
Touch **Reset ALL** to turn **OFF** all slot buttons.

[4] Touching **OK** starts Auto Adjust for the specified slots. Auto Adjust can be started when a button or more of valid slots are turned **ON**. Touching **Cancel** stops Auto Adjust and closes the **Auto Adjust** dialog box.

The Auto Adjust executing status is displayed in the lower part of the **Result** tab. "----" is displayed when the Auto Adjust is stopped, and displayed for items that are not targeted for Auto Adjust. Threshold is displayed in XXXX V units, and Data Delay is displayed in XXXX mUI or XXXX ps units. Data Delay in ps units is converted from that in mUI units, using the frequency counter value.

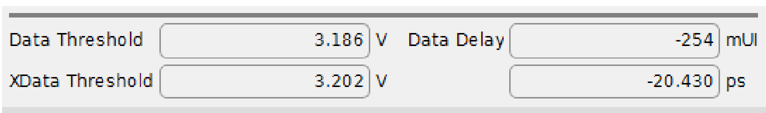


Figure 5.18.1-2 Auto Adjust executing status on the Result tab

Note:

Input the signal that makes the cross points at 50% when using the Auto Adjust. If inputting the signal that does not make the cross points at 50%, the Auto Adjust may not function properly.

5.19 Auto Measurement

MU195040A has automatic measurement function that judges and detects the margin in the clock phase direction (phase margin) and in the threshold voltage direction (threshold margin).

- Eye Margin Measurement
- Bathtub Measurement
- PAM BER Measurement
- Eye Contour Measurement

For details of Auto Measurement, refer to the *MX190000A Signal Quality Analyzer-R Control Software Operation Manual*.

5.20 Noise Generation Function

Noise generation can be set on the MU195050A operation window.

5.20.1 MU195050A Operation Window

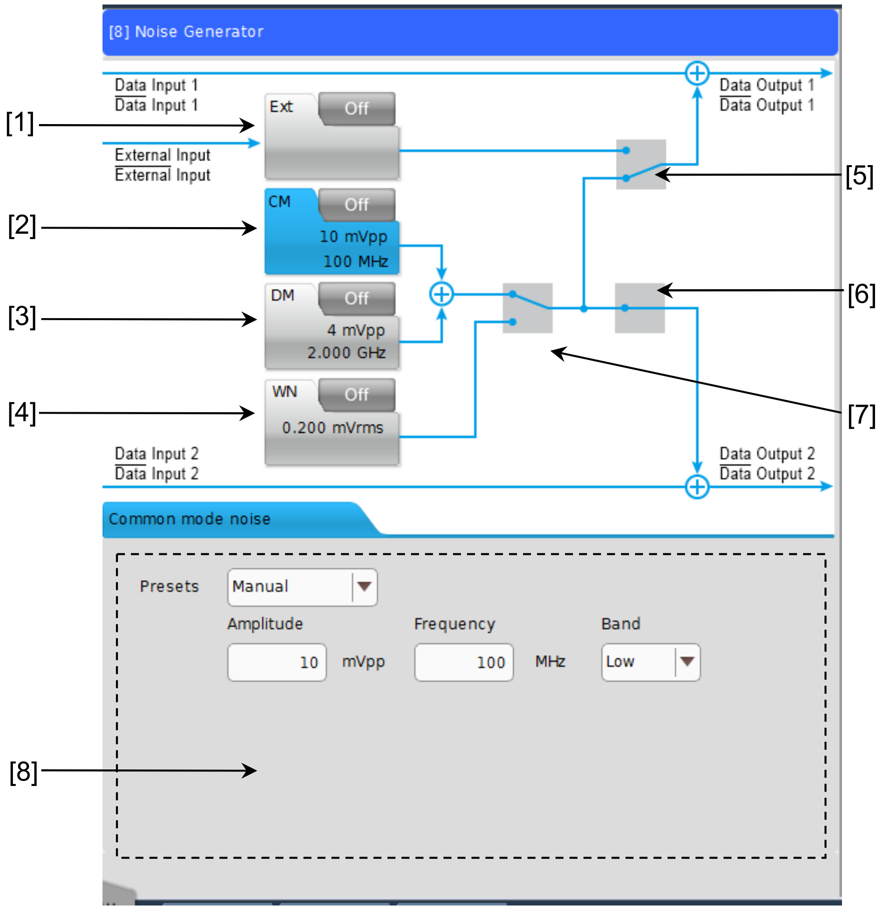


Figure 5.20.1-1 MU195050A Operation Window

Table 5.20.1-1 Items on MU195050A Operation Window

No.	Item	Function	
[1]	Ext button	Turns On or Off External Input.	
[2]	CM button	Turns On or Off Common Mode Noise and displays the setting items in [8].	
		Presets	Select a value from the preset standard list of Common Mode Noise or select **Manual** and enter a numerical value. Manual: Allows numerical values for amplitude and frequency. TBT3: Amplitude 100 mV Frequency 400 MHz PCIe 4: Amplitude 150 mV Frequency 120 MHz PCIe 5: Amplitude 150 mV Frequency 120 MHz
		Amplitude	Available when Presets is set to **Manual**. Setting range: 10 to 250 mV, 2 mV step
		Frequency	Available when Presets is set to **Manual**. Setting range: 100 to 1000 MHz, 1 MHz step @Low Band 1 to 6 GHz, 10 MHz step @High Band
[3]	DM button	Turns On or Off Differential Mode Noise and displays the setting items in [8].	
		Presets	Select a value from the preset standard list of Differential Mode Noise or select **Manual** and enter a numerical value. Manual: Allows numerical values for amplitude and frequency. PCIe 3: Amplitude 16 mV Frequency 2.1 GHz PCIe 4: Amplitude 16 mV Frequency 2.1 GHz PCIe 5: Amplitude 10 mV Frequency 2.1 GHz
		Amplitude	Available when Presets is set to **Manual**. Setting range: 10 to 250 mV, 2 mV step
		Frequency	Available when Presets is set to **Manual**. Setting range: 100 to 1000 MHz, 1 MHz step @Low Band 1 to 6 GHz, 10 MHz step @High Band
[4]	WN button*	Turns On or Off White Noise and displays the setting items in [8].	
		Amplitude	Setting range: 0.2 to 25 mVrms, 0.2 mVrms step
[5] [6]	Noise Selector per CH	Controls noise selection to add to Data1 and Data2. They are linked in operation.	
[7]	Noise Selector	Selects CM/DM or WN for noise type to add to Data1 or Data2.	
[8]	Advanced Setting Area	Advanced setting is allowed by selecting a desired item from [1] to [4].	

*: When the MU195050A-x01 is installed.

Chapter 6 Usage Examples

This chapter describes usage examples of measurement using the MP1900A modules.

6.1 Measuring Optical Transceiver Module

This section describes how to test the electrical interface input sensitivity of a CFP2 optical transceiver module by using MU195020A and MU195040A.

In the following test example, the MU195020A and MU195040A are mounted onto the MP1900A. The options configuring the test system are as follows:

MP1900A

MU181000B

MU195020A-x20

MU195040A-x20

Measurement

1. Connect the MP1900A and DUT to GND.
2. Use a coaxial connector to connect the Clock Output connector of the MU181000B and the Ext. Clock In connector of the MU195020A.
3. Use a coaxial connector to connect the Clock Out connector of the MU195020A and the Ext. Clock In connector of the MU195040A.

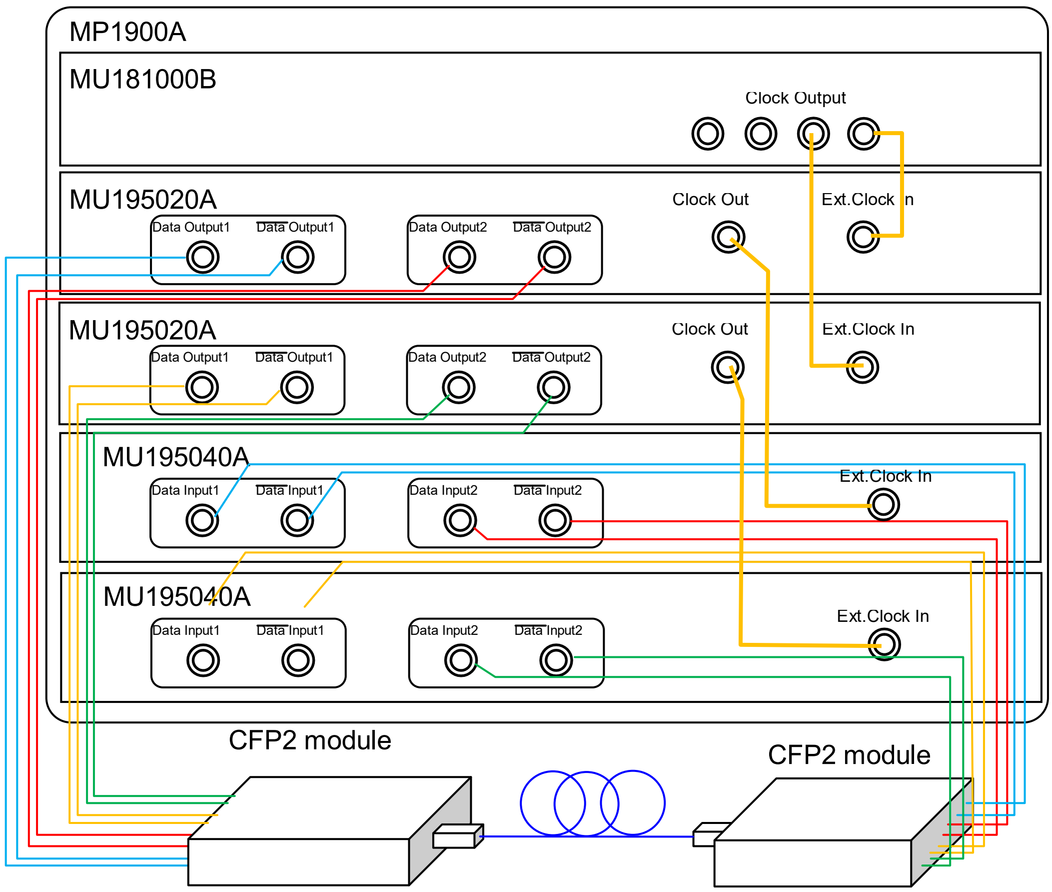


Figure 6.1-1 Connection diagram for CFP2 module evaluation

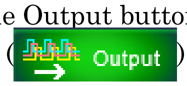
4. Use coaxial cables to connect the Data Output 1-2 connectors and $\overline{\text{Data}}$ Output 1-2 connectors of the MU195020A to the Data Input connectors of the CFP2 module (8 connections).
5. Use coaxial cables to connect the Data Input 1-2 connectors and $\overline{\text{Data}}$ Input 1-2 connectors of the MU195040A to the Data Output connectors of the CFP2 module (8 connections).

Test method

1. Connect the power cord of the MP1900A.
2. Turn on the MP1900A.
3. Turn **OFF** data output. Match MU195020A data output interface to DUT's input by adjusting the amplitude and offset in the **Output** tab.
4. Set the pattern by selecting a test pattern in the **Pattern** tab of the MU195020A and MU195040A.
5. Set the operation bit rate in the **Output** tab of the MU195020A.
6. Adjust the data input interface of the MU195040A to the output interface of the DUT.
   Select a terminal condition at the Input Condition in the **Input** tab of the MU195040A. Since the CFP2 module is connected by the differential interface, select **Differential 100 Ohm**, and then “Tracking”.
7. Turn on the CFP2 module.
   Be sure to turn on the MP1900A first, and then the CFP2 module.

CAUTION

The DUT may be damaged if a signal line is connected or disconnected while the output is ON. Be sure to turn off the MP1900A before changing the cable connection.

8. Set Data/XData to **ON** in the **Output** tab of the MU195020A, and then touch the Output button on the top of the screen to turn it from grey to green (

).
9. Adjust the threshold voltage of the MU195040A.
   Select the **Auto Adjust** module function button.
10. Start the measurement on the **Result** tab of the MU195040A, and check the BER measurement result.
11. After checking that the DUT is operating normally, the CFP2 module data input (TD+ and TD−) sensitivity can be measured by decreasing the output level of the MU195020A.

6.2 Generating 56 Gbit/s DQPSK Signals

This section describes how to generate 56G band DQPSK signals by using the MU195020A-x20 and the DQPSK modulator.

In the following test example, the MU195020A is mounted onto the MP1900A. The options configuring the test system are as follows:

MU181000A

MU195020A-x20

Measurement

1. Connect the MP1900A and DUT to GND.
2. Use a coaxial connector to connect the Clock Output connector of the MU181000A and the Ext. Clock In connector of the MU195020A.
3. Use coaxial cables to connect the Data Output 1 and 2 and $\overline{\text{Data}}$ Output 1 and 2 connectors of the MU195020A to the DQPSK modulator (four connections).

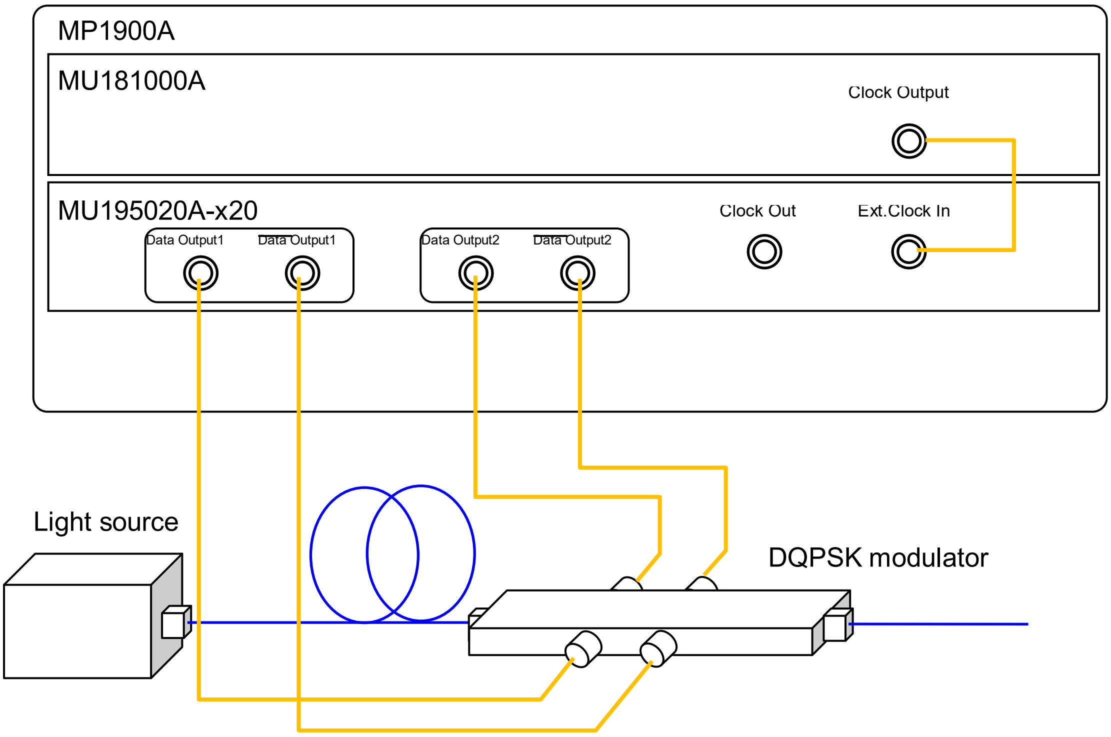
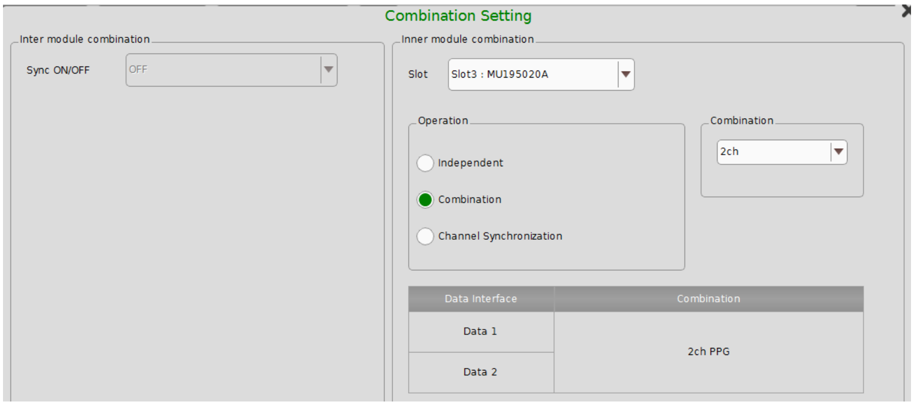
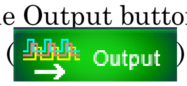


Figure 6.2-1 Connection diagram for generating 56 Gbit/s DQPSK signals

Test method

1. Connect the power cord of the MP1900A.
2. Turn on the MP1900A.
3. Turn **OFF** data output. Match MU195020A data output interface to DUT's input by adjusting the amplitude and offset in the **Output** tab.
4. Set the operation bit rate to 28 Gbit/s in the **Output** tab of the MU195020A.
5. Select a test pattern in the **Pattern** tab of the MU195020A.
6. Touch  to open the **Combination Setting** window. Select **Combination** for operation and select **2ch** for combination.



7. In the **Pre-Code** tab of the MU195020A, set Pre-Code to **ON**, select **DQPSK** in the Type dropdown list.
8. Set Data Output to **ON** in the **Output** tab of the MU195020A, and then touch the Output button on the top of the screen to turn it from grey to green ().

By adding MU195020A signals to the DQPSK modulator, optical signals modulated to 56 Gbit/s are outputted.

Chapter 7 Remote Command

For the explanation of the SCPI format and status, refer to the *MX190000A Signal Quality Analyzer-R Control Software Operation Manual Remote Control.*

Chapter 8 Performance Test

This chapter describes the performance testing of the MP1900A modules.

8

Performance Test

8.1 Performance Test Items

Performance test is executed to check that the major functions of the MP1900A Modules meet the required specifications.
Execute performance test at acceptance inspection, operation check after repair, and periodic testing (once every six months).

8.2 Devices Required for Performance Tests

Before starting performance test, warm up the MP1900A and the measuring instruments for at least 30 minutes. Table 8.2-1 shows the required devices for performance test.

Table 8.2-1 Devices Required for Performance Tests

Device name	Model	Required performance	
Error detector	MP1900A + MU195040A-x01	Operating frequency: Data input sensitivity:	2.4 to 32.1 GHz 300 mVp-p or more
Sampling oscilloscope		Electrical interface:	70 GHz or more band
Signal generator	MP1900A + MU195020A + MU181000A/B or MG3690 series	When using Ext Clock: Operating frequency: Output level: Waveform:	 1.2 to 16.05 GHz 300 to 1000 mVp-p Rectangular wave or sine wave
coaxial cables (80 cm K connector)	J1439A	Bandwidth:	40 GHz
Coaxial Attenuator	J0541E	Attenuation:	6 dB
Power Meter	ML2437A or ML2438A		
Power Sensor + cable	MA2444D		

Note:

Before starting the performance test, warm up the device under test and the measuring instruments for at least 30 minutes, and wait until they become sufficiently stabilized unless otherwise specified.

Maximum measurement accuracy is assured under the following conditions:
Measurement is performed at room temperature.
Fluctuations of AC power supply voltage are small.
Noise, vibration, dust, and humidity are insignificant.

8.3 Performance Test Items

This section describes the following test items.

(1) Operating bit rate range

(2) Waveform

8.3.1 Operating frequency range

(1) Specifications

Table 8.3.1-1 Specifications

Option	Specifications
MU195020A	2.4 to 21.0 Gbit/s
MU195020A-x01	2.4 to 32.1 Gbit/s
MU195040A	2.4 to 21.0 Gbit/s
MU195040A-x01	2.4 to 32.1 Gbit/s

(2) Device connection

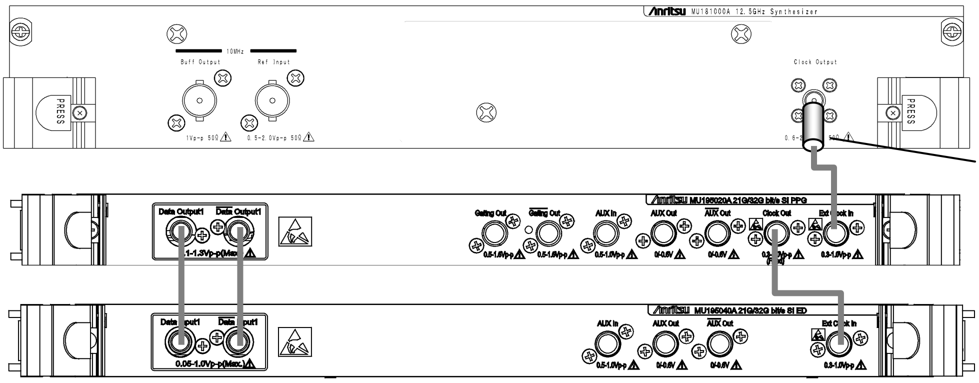


Figure 8.3.1-1 Connection diagram for operating frequency range test

When using the MU181000A, attach the 6 dB Coaxial Attenuator to the Clock Output connector.

8 Performance Test

(3) Test procedure

1. Mount the MU195020A onto the MP1900A, and turn on the MP1900A with the cables unconnected.
2. Set the Data signal output amplitude of the MU195020A to 500 mVp-p, offset (Vth) to 0 V, test pattern to PRBS31, and mark ratio to 1/2.
3. Turn off the MP1900A when setting the parameters completely.
4. Connect the measuring instrument cables as shown in Figure 8.3.1-1.
5. Turn on the MP1900A and the measuring instruments, and warm them up.
6. After warming up the instruments, enable the MP1900A signal output (ON) to output signals from the MU195020A.
7. Adjust the phase and threshold voltage of the MU195040A to the optimum values.
8. Check that no error is detected by the MU195040A.
9. Change the operating frequency and check if no error occurs within the rated operating frequency range.

8.3.2 Waveform Evaluation Test

(1) Specifications

Table 8.3.2-1 Specifications for MU195020A

Item	Specification
	MU195020A-x10/x20
Amplitude	0.1 to 1.3 Vp-p
Offset (Vth)	$-2.0-\frac{\text{Amp.}}{2}$ to $+3.3-\frac{\text{Amp.}}{2}$ V
Cross point	Amplitude: 1.0 Vp-p 50%
Tr/Tf	14 ps (20 to 80%)*1,*2
Jitter	8 ps p-p*1,*2,*3

*1: If MU195020A-x01 is not available, then this is at 21.0 Gbit/s.
If MU195020A-x01 is available, then this is at 32.1 Gbit/s.

*2: Typical value

*3: The jitter specification value is defined assuming that the oscilloscope with residual jitter less than 200 fs (RMS) is used.

(2) Device connection

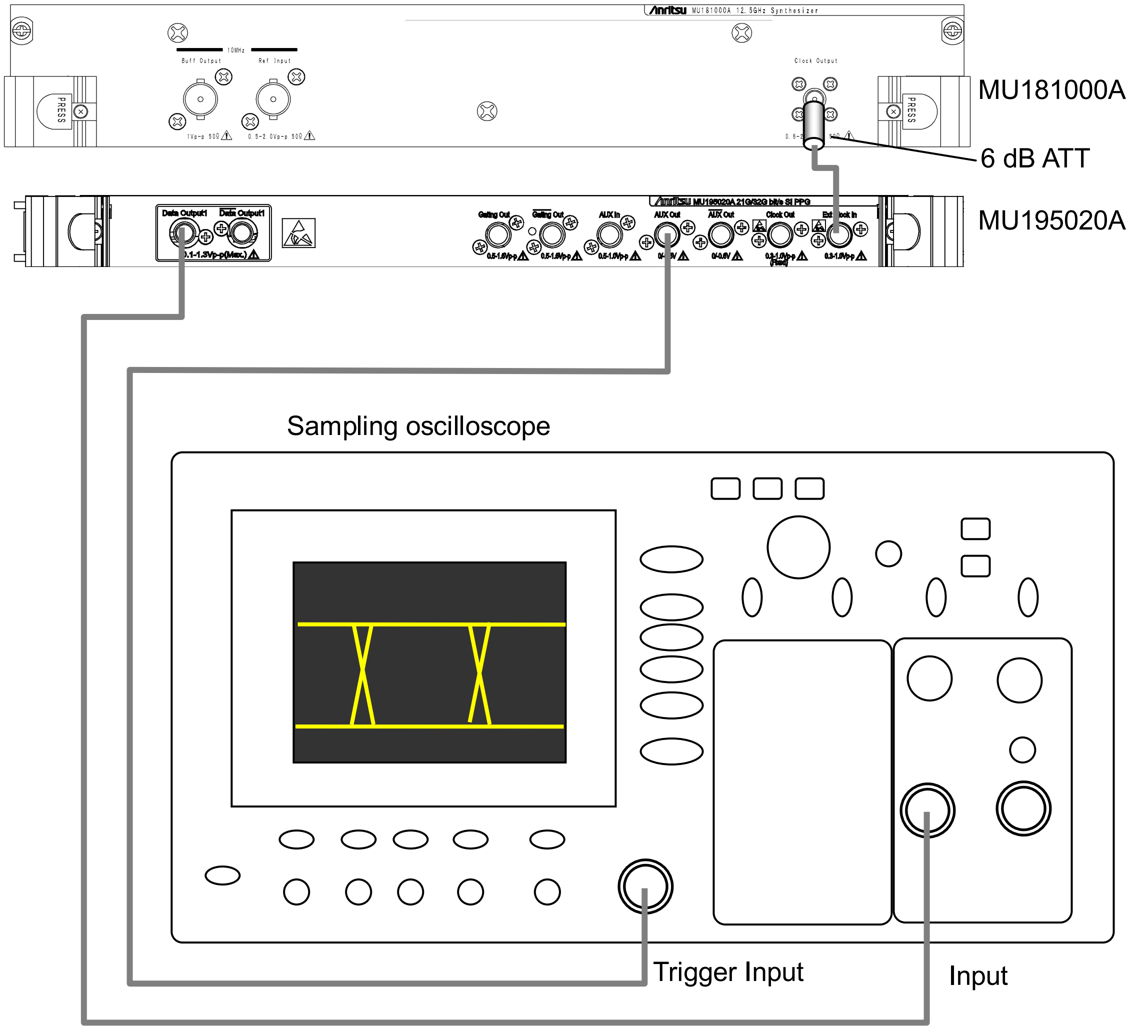


Figure 8.3.2-1 Connection diagram for waveform test

When using the MU181000A, attach the 6 dB Coaxial Attenuator to the Clock Output connector.

(3) Test procedure

1. Mount the MU195020A onto the MP1900A, and turn on the MP1900A with the cables unconnected.
2. Set the Data output amplitude, offset, and cross point to be tested in the MU195020A **Output** tab window.
3. Set the test pattern in the **Pattern** tab of the MU195020A.

   Since the specification parameters are evaluated by the eye pattern observation, set the test pattern to PRBS31, and the mark ratio to 1/2.

4. Select a trigger signal to input to the oscilloscope. Select **1/N Clock** in the AUX Output dropdown list in the **Misc1** tab of the MU195020A, and set the division ratio according to the sampling oscilloscope used.
5. Turn off the MP1900A when setting the parameters completely.
6. Connect the measuring instrument cables as shown in Figure 8.3.2-1.
7. Turn on the MP1900A and the measuring instruments, and warm them up.
8. After warming up the instruments, enable the MP1900A signal output (ON) and output signals.
9. Observe the output waveform on the sampling oscilloscope, and check that all the items meet the specifications.
10. Use a coaxial cable to connect the XData Output connector of the MU195020A and the Input connector of the sampling oscilloscope. Repeat the observation in Step 9.
11. If there are multiple channels, repeat the observation in Step 9 for all Data Output and XData Output.

8.3.3 Input level

(1) Specifications

Table 8.3.3-1 Specifications

Option	Specifications
MU195040A-x10/x20	Input amplitude: 0.05 to 1.0 Vp-p Threshold voltage: –3.5 to +3.3 V

(2) Connection

Refer to Figure 8.3.1-1 for the device connection.

(3) Procedure

1. Connect devices and configure the settings in the same manner as shown in Steps 1 to 5 in Section 8.3.1.
2. Set the output level of the MU195020A and the threshold voltage of the MU195040A as shown in Table 8.3.3-2. Next, set the output of the MU195020A to ON and tauch **Start** of the MU195040A. Adjust the phase as required, and check that no error occurs.

Table 8.3.3-2 Input level test setting (MU195040A)

	MU195020A			MU195040A	
No.	Termination	Amplitude [Vp-p]	Offset (Vth) [V]	Termination	Threshold voltage [V]
1	GND	1.0	–2.5	GND	–2.500
2		0.05*	–2.25		–2.250
3		1.0	+2.8		+2.800
4		0.05*	+3.05		+3.050
5	NECL	0.8	–1.3	Variable: – 2.0 V	–1.300
6	LVPECL	0.8	+2.0	Variable: + 1.3 V	+2.000
7	PCML	0.5	+3.05	Variable: + 3.3 V	+3.050

*: For the signals of amplitude 0.05 Vp-p, set the MU195020A to 0.5 Vp-p and use the Precision Fixed Attenuator (20 dB, application part 41KC-20).

Note:

When changing the termination condition, configure the settings of the MU195020A and the MU195040A in the following order. The MU195020A and the MU195040A may be damaged if the settings are configured in an incorrect order or the termination condition is not set correctly.

(1) Set the output of the MU195020A to OFF.

(2) Set the termination condition for the MU195040A to GND.

(3) Change the termination condition for the MU195020A.

(4) Set the termination condition for the MU195040A to that for the MU195020A set in Step [3].

3. Remove the cable from the Data Input connectors, and then connect the XData Input connectors, using a coaxial cable. In the MU195040A **Input** tab window, set **Input Condition** to **Single-Ended** and **XData**. Next, set the output level of the MU195020A and the threshold voltage of the MU195040A as the procedure 2, and check that no error occurs.

8.3.4 Pattern

(1) Specifications

- PRBS pattern
- Zero Substitution pattern

(2) Connection

Refer to Figure 8.3.1-1 for the device connection.

(3) Procedure

1. Connect devices and configure the settings in the same manner as shown in Steps 1 to 5 in Section 8.3.1.
2. Set the output of the MU195020A to ON and touch **Start** of the MU195040A. Adjust the phase as required, and check that no error occurs.
3. For both the MU195040A and the MU195020A, set the PRBS pattern length to $2^n–1$, changing the value of n to 7, 9, 10, 11, 15, 20, 23, and 31, and check that no error occurs.
   For the MU195040A, the PRBS pattern length can be set in the **Pattern** tab window.
4. Set the PRBS pattern length to $2^{31}–1$.
   For the MU195040A, this operation can be performed by changing Logic POS/NEG on the **Pattern** tab window. Check that no error occurs.
5. For both the MU195040A and the MU195020A, set the test pattern to Zero Substitution, then, set Length to $2^n–1$, changing the value of n to 7, 9, 10, 11, 15, 20, and 23, and check that no error occurs. Next, set Length to 2^n, changing the value of n to 7, 9, 10, 11, 15, 20, and 23, and confirm that no error occurs.

8.3.5 Error detection

(1) Specifications

Error rate:	0.0000×10^{-16} to 1.0000
Error count:	0 to 1×10^{16}
Error free interval (EFI):	0.0000 to 100.0000%
Error interval (EI):	0 to 1×10^{16}
Clock frequency:	
MU195040A-x01 is not installed	1.2 to 10.5 GHz, accuracy: ± (10 ppm + 1 kHz)
MU195040A-x01 is installed	1.2 to 16.05 GHz, accuracy: ± (10 ppm + 1 kHz)

(2) Connection

Refer to Figure 8.3.1-1 for the device connection.

(3) Procedure

1. Connect devices and configure the settings in the same manner as shown in Steps 1 to 5 in Section 8.3.1.
2. Set the frequency of the MU181000A to 10 GHz, set the output of the MU195020A to ON, and then touch **Start** of the MU195040A. Adjust the phase as required, and check that no error occurs.
3. Turn On error insertion of the MU195020A, and make sure that the ER measurement results on the **Result** tab of the MU195040A match the values set on the **Error Addition** tab on the MU195020A.
4. Set "Single" for error insertion of the MU195020A (set Variation to **Single** in the MU195020A **Error Addition** tab window). In the Gating field on the MU195040A **Measurement** tab window, set **Cycle** to **Single**, and set the measurement time to 10 seconds.
5. Touch the **Start** button of the MU195040A. While the measurement is running for 10 seconds, touch **Single** once on the **Error Addition** tab of the MU195020A.

   When the measurement has finished, check that the measurement results are as follows.

Error rate (ER):	5.0000E–12
Error count (EC):	1.0000E–00
Error free interval (%EFI):	99.9900%
Error interval (EI):	1

8.3.6 Noise Evaluation Test

(1) Specifications

Table 8.3.6-1 Specifications for MU195050A

Item	Specification
Common Mode Noise (CMI)	10 to 250 mVp-p
Differential Mode Noise (DMI)	4 to 200 mVp-p (Differential)
White Noise*	0.2 to 25 mVrms

*: Available when MU195050A-x01 is installed.

(2) Connection for CMI/DMI evaluation

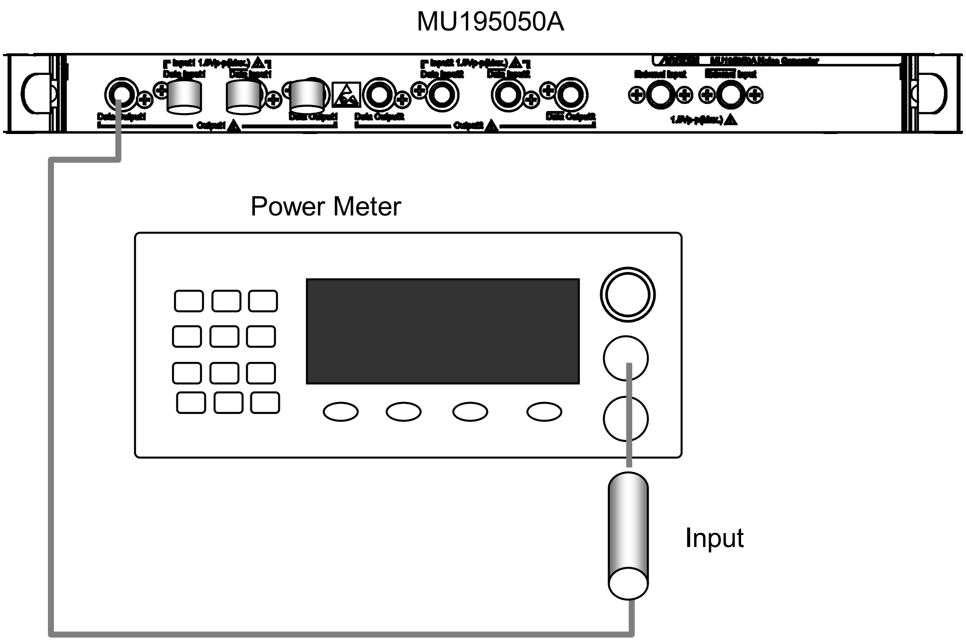


Figure 8.3.6-1 Connection for CMI/DMI Test

(3) Connection for White Noise evaluation

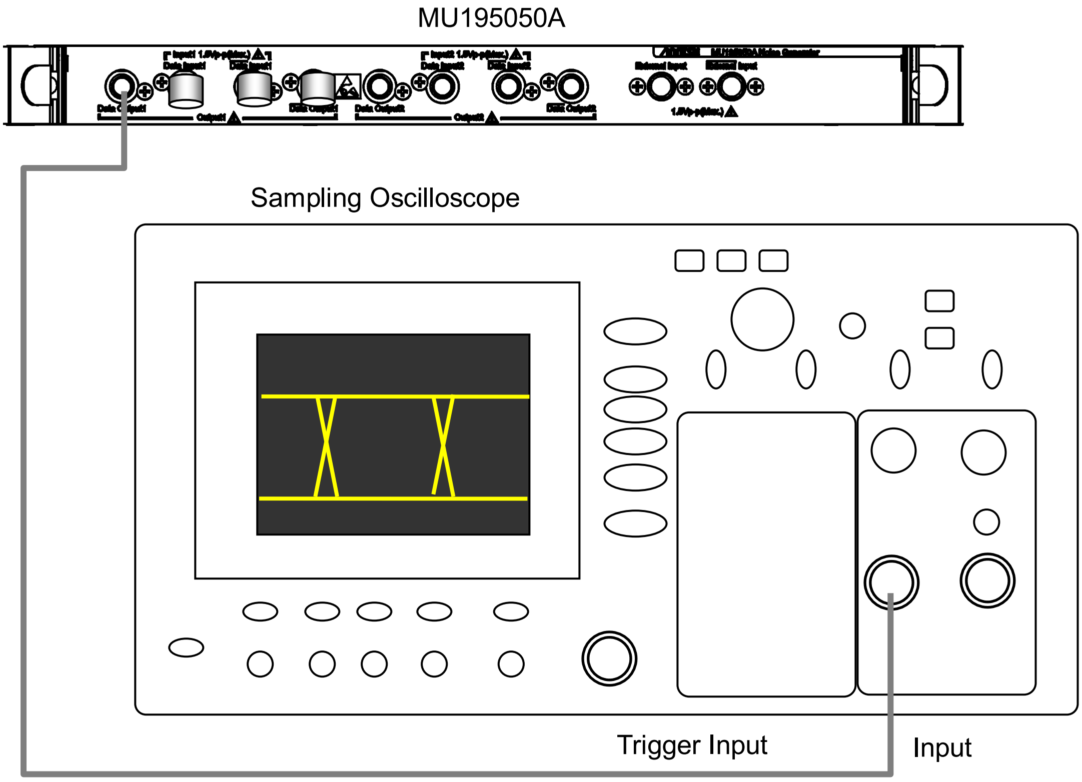


Figure 8.3.6-2 Connection for White Noise Test

(4) Test procedure

CMI/DMI evaluation procedure

1. Install the MU195050A on the MP1900A and install Terminators to the connectors that are not used for the channel measurement. Turn On the MP1900A without connecting the cables to the connectors used for the measurement.
2. Specify output amplitude and frequency of CMI or DMI to be evaluated by the MU195050A module application.
3. When the setup is completed, turn Off the MP1900A.
4. Refer to Figure 8.3.6-1 “Connection for CMI/DMI Test” and connect the MU195050A and the Power Meter by coaxial cable.
5. Turn On the MP1900A and the Power Meter for warming up.
6. After warming up, turn On the MU195050A connector to test and output signal. Turn Off the connector outputs that are not tested.
7. Measure the power of output amplitude by Power Meter and check that all the items meet the standard.

8. Perform the measurement in Step 7 for every Data output and XData output.

White Noise evaluation procedure

1. Install the MU195050A on the MP1900A and install Terminators to the output connectors that are not used for the measurement. Turn On the MP1900A without connecting the cables to the connectors used for the measurement.
2. Specify the output amplitude of White Noise on the MU195050A module application.
3. When the setup is completed, turn Off the MP1900A.
4. Refer to Figure 8.3.6-2 “Connection for White Noise Test” and connect the MU195050A and the sampling oscilloscope by coaxial cable.
5. Turn On the MP1900A and the sampling oscilloscope for warming up.
6. After warming them up, turn On the White Noise output of the MU195050A to output signal. Turn Off the connector outputs that are not tested.
7. Set the sampling oscilloscope to 50 GHz band and Free Run to observe the MU195050A output waveform. Make sure that all items meet the standards. Measure the output level of White Noise by histogram (1σ = rms).
8. Perform the measurement in Step 7 for every Data output and XData output.

Chapter 9 Maintenance

This chapter describes maintenance of the MP1900A modules.

9.1 Daily Maintenance

- Wipe off any external stains with a cloth damped with diluted mild detergent.
- Vacuum away any accumulated dust or dirt with a vacuum cleaner.
- Tighten any loose parts fixed with screws, using the specified tools.

9.2 Cautions on Storage

Wipe off any dust, soil, or stain on the MP1900A modules prior to storage. Install the supplied Opens or Terminators to the connectors on the panel.

Avoid storing the MP1900A modules in any of the following locations:

- In direct sunlight for extended periods
- Outdoors
- In excessively dusty locations
- Where condensation may occur
- In liquids, such as water, oil, or organic solvents, and medical fluids, or places where these liquids may adhere
- In salty air or in place chemically active gases (sulfur dioxide, hydrogen sulfide, chlorine, ammonia, nitrogen dioxide, or hydrogen chloride etc.) are present
- Where toppling over may occur
- In the presence of lubricating oil mists
- In places at an altitude of more than 2,000 m
- In the presence of frequent vibration or mechanical shock, such as in cars, ships, or airplanes
- Under the following temperature and humidity conditions:
  Temperature range of ≤–20°C or ≥60°C
  Humidity range of ≥85%

Recommended storage conditions

In addition to the abovementioned storage cautions, the following environment conditions are recommended for long-term storage.

- Temperature range of 5 to 30°C
- Humidity range of 40 to 75%
- Slight daily fluctuation in temperature and humidity

9.3 Transportation

Use the original packing materials, if possible, when packing the MP1900A modules for transport. If you do not have the original packing materials, pack the MP1900A modules according to the following procedure. When handling the MP1900A modules, always wear clean gloves, and handle it gently so as not to damage it.

<Procedure>

1. Use a dry cloth to wipe off any stain or dust on the exterior of the MP1900A module.
2. Check for loose or missing screws.
3. Provide protection for structural protrusions and parts that can easily be deformed, and wrap the MP1900A module with a sheet of polyethylene. Finally, cover with moisture-proof paper.
4. Place the wrapped MP1900A module into a cardboard box, and tape the flaps with adhesive tape. Furthermore, store it in a wooden box as required by the transportation distance or method.
5. During transportation, place it under an environment that meets the conditions described in 9.2 “Cautions on Storage”.

9.4 Calibration

Regular maintenance such as periodic inspections and calibration is essential for the Signal Quality Analyzer-R series for long-term stable performance. Regular inspection and calibration are recommended for using the Signal Quality Analyzer Series in its prime condition at all times. The recommended calibration cycle after delivery of the Signal Quality Analyzer Series is twelve months.

If you require support after delivery, contact an Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file on the PDF version.

We may not provide calibration or repair if any of the following cases apply.

- Seven or more years have elapsed after production and parts for the instrument are difficult to obtain, or it is determined that reliability cannot be maintained after calibration/repair due to significant wear.
- Circuit changes, repair, or modifications are done without our approval.
- It is determined that the repair cost would be higher than the price of a new item

9.5 Disposal

Confirm the notes described in the *Signal Quality Analyzer-R Operation Manual* and observe national and local regulations when disposing of the MP1900A modules.

Chapter 10 Troubleshooting

This chapter describes how to check whether a failure has arisen when an error occurs during the operation of the MP1900A modules.

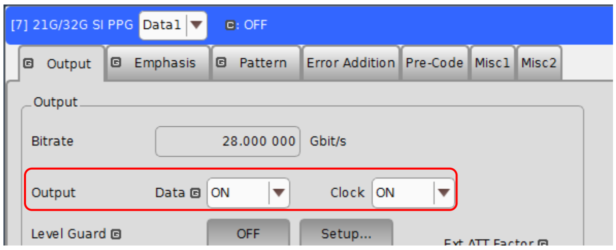
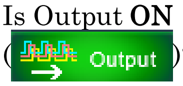
10.1 Problems Discovered during Module Replacement

Table 10.1-1 Remedies for problems discovered during replacement of MP1900A modules

Symptom	Location to Check	Remedy
A module is not recognized.	Is the module installed properly?	Install the module again by referring to 3.3 “Installing and Removing Modules” in the *MP1900A Signal Quality Analyzer-R Operation Manual*.
	Are the appropriate modules installed?	Confirm the MP1900A software version and the supported modules by visiting the MP1900A Series Signal Quality Analyzers-R product information page in the Anritsu web site (https://www.anritsu.com). If the appropriate modulus are not recognized, it may have failed. Contact an Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file.

10.2 Problems Discovered during Output Waveform Observation

Table 10.2-1 Remedies for problems discovered during waveform observation

Symptom	Location to Check	Remedy
Output waveform cannot be monitored normally.	Is the **Data** or **Clock** on the **Output** tab window set to **ON**?	In the **Output** tab window, set **Data** or **Clock** to be output to ON.  When Output is **OFF**, turn it **ON** by touching the list box.
	Is Output **ON** ()?	Touch  on the top left corner of the screen to turn **Output ON**.
	Is the operating clock supplied normally?	When using the internal clock, check the bit rate setting. When the clock is supplied externally, check the connection interface. Refer to 3.1 “Panel Layout” for the interface.
	Is the trigger clock set correctly?	It is recommended to use the signal output from AUX output connector as the trigger clock. Check the AUX output connector settings and interface with the sampling oscilloscope to be measured.
	Is the electrical interface cable loose?	Tighten the connector.
	Do the cables used have good high-frequency characteristics?	Use cables and connectors with bandwidth of 40 GHz or more.

10.3 Problems Discovered during Error Rate Measurement

Table 10.3-1 Remedies for problems discovered during error rate measurement

Symptom	Location to Check	Remedy
An error occurs.	Is the connection interface with the DUT to be measured correct?	Check that the data rate, level, offset and termination conditions are the same.
	Are the logical patterns correctly set on the MU195020A and the error detector (ED)?	Check if the patterns generated by the MU195020A are set such that they can be received by the DUT, and if the set patterns generated by the DUT and detected by the ED are the same. If the DUT outputs the patterns from the MU195020A as they are, connect the MU195020A and ED directly to check if an error is detected.
	Is the error addition function set to off?	Check that the Error Addition switch on the **Error Addition** tab is set to **OFF**.
	Is the electrical interface cable loose?	Tighten the connector.
	Do the cables used have good high-frequency characteristics?	Use cables and connectors with bandwidth of 40 GHz or more.
	Are sufficient phase margin and threshold margin are secured?	Adjust the phase and offset to be optimal between the MU195020A and the DUT as well as between the DUT and ED, respectively.

10.4 Synchronization Failure

Table 10.4-1 Troubleshooting List of Synchronization Failures

Item	Location to Check	Remedy
Input conditions	Do the quality, status and length of the connection cables comply with the specifications?	Replace the cables with appropriate ones in the following cases. • Frequency characteristics are not sufficient. • Loss is large. • Cables and connectors are damaged. • Connectors are contaminated.
	Is the cable connection correct and secure?	Confirm the destination and check if the connector is tightened securely.
	Are the single and differential (50/100 Ω) inputs set correctly?	Set the correct value.
	Is the input level correct?	Check the level by using an oscilloscope, etc.
	Are the input bit rate and clock frequency set correctly?	Set the bit rate and clock frequency correctly. ***Note:*** Use the frequency counter to check the current clock frequency.
	Is the frequency set near the bit rate when using clock recovery?	Set the frequency near the bit rate to be used.
	Has the clock loss display disappeared?	Check the data and clock signals to be input or clock recovery settings.
Termination conditions	Was the termination potential adjusted?	Set the termination potential correctly. ***Note:*** Incorrect setting may result in unit failure.

Table 10.4-1 Troubleshooting List of Synchronization Failures (Cont'd)

Item	Location to Check	Remedy
Threshold	During differential input, is the difference between the Data and XData threshold voltages above 3 V?	The difference value should be within 3 V.
	Is the operating limit for Auto Adjust or Auto Search out of range?	Adjust it manually.
Phase	Is the operating limit for Auto Adjust or Auto Search out of range?	Adjust it manually.
Pattern	Are the patterns matched?	Match the patterns between MU195020A and MU195040A.
Synchronization	Is Auto Sync set to **ON**?	Set it to **ON**. Re-synchronization is performed automatically.
	Have you tried with a different Sync Control setting?	Optimal synchronization method varies according to the pattern type. ***Note:*** Can be set for patterns except PRBS.
Other	Is Bit/Block Window set to **OFF**?	Set it to **OFF**.
	Is MU195040A External Mask set to **OFF**?	Set it to **OFF**.
	Is the **Repeat** mode set?	Set the **Repeat** mode.

If a problem cannot be solved using any of the items listed above, perform initialization and check the items again. If the problem still occurs, contact an Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file on the PDF version.

Appendix A Pseudo-Random Pattern

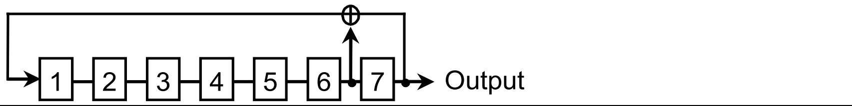
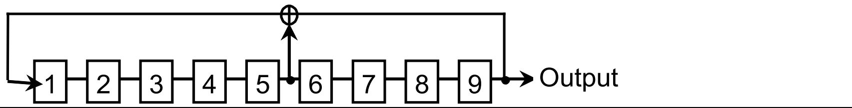
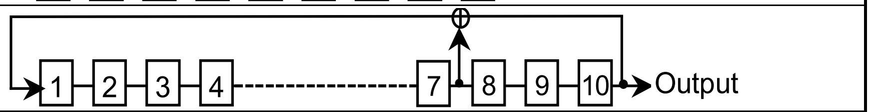
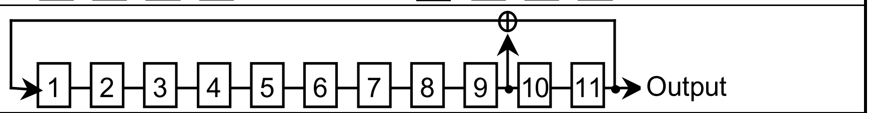
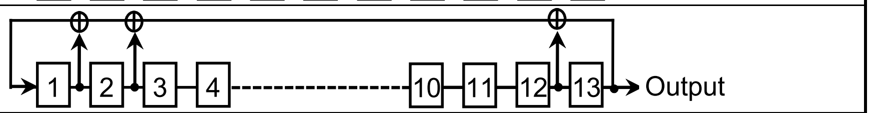
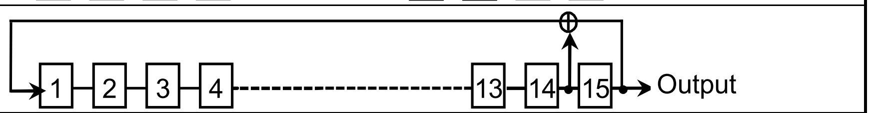
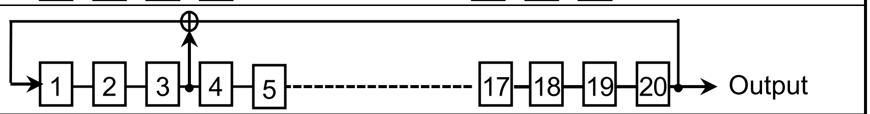
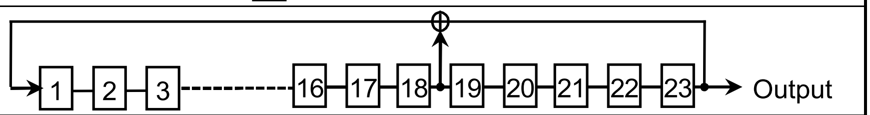
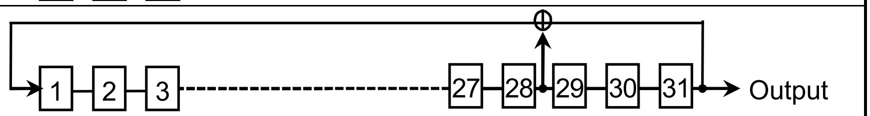
A.1 Pseudo-Random Pattern

Table A.1-1 shows the principle of pseudo-random pattern generation. A pseudo-random pattern is expressed in an N-th degree generating polynomial, with one cycle of 2^n-1. For a PRBS pattern with a cycle of 2^n-1, a pattern of successive "1s" for the number N is generated once in a cycle.

For the output level of the PRBS pattern, "1" indicates the low level and "0" indicates the high level when Logic is set to POS (positive).

The mark ratios of the PRBS pattern are generated as shown in the block diagrams of Table A.1-1.

Table A.1-1 Principle of pseudo-random pattern generation

Cycle	Generating polynomial	Pattern generation block diagram
2^7-1	$1+X^6+X^7$	
2^9-1	$1+X^5+X^9$	
$2^{10}-1$	$1+X^7+X^{10}$	
$2^{11}-1$	$1+X^9+X^{11}$	
$2^{13}-1$	$1+X+X^2+X^{12}+X^{13}$	
$2^{15}-1$	$1+X^{14}+X^{15}$	
$2^{20}-1$	$1+X^3+X^{20}$	
$2^{23}-1$	$1+X^{18}+X^{23}$	
$2^{31}-1$	$1+X^{28}+X^{31}$	

$\boxed{N}$: Shift register (N=1, 2, 3….)

$\oplus$: Exclusive OR

A.2 Zero-Substitution Pattern

A string of successive “0s” for the number of set bits is made by substituting “0” for the pattern that follows the longest bit string of successive 0s in a PRBS pattern. In this event, if the bit immediately after the bit substituted to “0” is also “0”, it is inverted to “1”.

Example: For a PRBS pattern with a cycle of 2^7, the largest number of successive 0s is 6 bits (7 – 1), and zero substitution starts from the following position:

```
         1000000100000011000010 10....←PRBS pattern with a cycle of 2^7

7 bits   1000000010          The bit immediately after the
11 bits  10000000000011      zero-substituted bit is inverted from 0 to 1.

13 bits  1000000000000010
```

Figure A.2-1 Zero-Substitution Pattern

Appendix B List of Initial Settings

B.1 List of Initialized Settings

This appendix shows the MP1900A Modules settings that are initialized to the defaults at factory shipment.

Select **Menu** → **Initialize** initializes all the setting items.

Table B.1-1 List of MU195020A Initialized Items

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Output	Bitrate			Variable
		Bitrate		10.000 000 Gbit/s
	Data, XData Output			ON
	Clock Output			ON
	Data/XData			
		Level Guard		OFF
		Level Guard Setup	Amplitude	1.000 Vp-p
			Offset limit	–4.000 to 3.300 V
	Defined Interface			Variable
			Amplitude	1.000 Vp-p
			Offset switching	AC OFF
			Offset	0.000 V
			External ATT Factor	0 dB
	Half Period Jitter			0
	Delay			0 mUI
			Calibration	–
		Jitter Input		OFF

Table B.1-1   List of MU195020A Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Emphasis	Manual Setting	Emphasis Function		OFF
		Standard/Preset		USER
				De-Emphasis
				Preset0
		Amplitude		1.000 Vp-p
		Each Cursor Value		0 dB
	ISI	ISI Function		OFF
		Standard/Channel		USER
				–
		Board Type		Not Use
		NF Insertion Loss		10.00 dB
		1/2 NF Insertion Loss		5.00 dB
	Channel Emulator	Channel Emulator Function		OFF
		Response		Inverse

Table B.1-1 List of MU195020A Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Pattern	PRBS	Length		2^15–1
		Logic		POS
		Mark Ratio		1/2
	ZeroSubstitution	Length		2^15
		Zero-Substitution Length		1 bit
		Additional Bit		1
	Data	Logic		POS
		Current Outputting Pattern		No.1
		Length		2 bits At 2ch Combination: 4 bits
		Maximum List Num		1
	Mixed Data	Logic		POS
		Row Length		2048 bits At 2ch Combination: 4096 bits
		Data Length		1024 bits At 2ch Combination: 2048 bits
		Number of Block		1
		Number of Row		1
		PRBS	Pattern	PRBS15
			Mark Ratio	1/2
		Scramble		OFF
		Scramble Setup		All OFF
		PRBS Sequence		Consecutive
	PAM4*1	Logic		POS
		Sequence		PRBS31Q
	Sequence*2	Logic		POS
		PRBS Inversion		ON
		Specification		PCIe1
		Trigger Block No.		1

*1: Configurable when 2ch Combination or 64G x 2ch Combination is set

*2: Configurable when Independent is set
This function is available for the MU195020A-x50.

Table B.1-1 List of MU195020A Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Pattern (Cont'd)	Pattern Editor	Zoom		× 1
		Row Length		2048 bits At 2ch Combination: 4096 bits
		Data Length	Data	2 bits At 2ch Combination: 4 bits
			Mixed	1024 bits At 2ch Combination: 2048 bits (When Mixed-Data is selected)
		Number of Block		1
		Number of Row		1
		Format		Hex
		Edit Mode		Overwrite
	Sequence Editor	Preset	2.5G	P4
			5.0G	P0
			8.0G	P7
			16.0G	P7
		8b10b SKP OS	Symbol Length	COM+3
			Interval	1538
			Symbol Length x2	OFF
		128b130b SKP OS	Symbol Length	16
			Interval	20
			Symbol Length x2	OFF
		Scrambler Seed	8b10b	FFFF
			128b130b	Lane0: 1DBFBC
	8b10b Pattern Editor	Data Length		32 bits
		Notation		Symbol(8b10b)
		Edit Mode		Overwrite
	128b130b Pattern Editor	Data Length		128 bits
		Notation		Hex(Byte)
		Edit Mode		Overwrite
	128b132b Pattern Editor	Data Length		128 bits
		Notation		Hex(Byte)
		Edit Mode		Overwrite

Table B.1-1 List of MU195020A Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Error Addition	Error Addition			OFF
		Source		Internal
		Variation		Repeat
		Route		Select, 1
		Error Rate		1E–3
		When Test Pattern is Mixed Row 1		Data: Unselected PRBS: Unselected
Pre-Code*3	Pre-Code			
		Pre-Code		OFF
		Type		DQPSK
		Initial Data		1
Misc1	Pattern Sequence			Repeat
		Repeat	Pulse Width	128 bits
			Delay	128
		Burst	Source	Internal
			Data Sequence	Restart
			Enable Period	128 000 bits 2ch Combination: Default × 2
			Burst Cycle	12 800 000 bits 2ch Combination: Default × 2
			Delay	0 bits
			Pulse Width	128 000 bits 2ch Combination: Default × 2
	Aux Input			Error Injection
			Vth	0 V
	Aux Output			1/N Clock
		1/N Clock	(Divide ratio)	1/64 clock
		Pattern Sync	For PRBS, Zero-Substitution, Data Position	 1 bits
			For Mixed Data Block No. Row No.	 1 1
		Burst Output 2	Delay	0
			Pulse Width	128 000 bits 2ch Combination: Default × 2
		Pattern change Trigger		OFF

*3: This function is available for the MU195020A-x20.

Appendix B

Appendix

Table B.1-1 List of MU195020A Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Misc2	Clock Setting			
		Clock Source		External
		Bit Rate		12.500 000 Gbit/s
		Offset		0 ppm
		Output Clock Rate		Half rate
		Reference Clock		Internal
		Operation Bit Rate		2.4 to 32.1

Table B.1-2 List of MU195040A Initialized Items

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Result	Switch of setting items	Setting display format		Gating
		Result display format		Error/Alarm
		Time display format		Date&Time
		Error/Alarm display	Zoom	OFF
			Overall Ch	OFF
	Start of Error/Alarm measurement			–
	Stop of Error/Alarm measurement			–
Measurement	Measurement Period (Gating)	Measurement period unit (Unit)		Time
		Measurement period time		00 00:00:01
		Clock count for measurement period		>E+10
		Error count for measurement period		>E+10
		Block count for measurement period		>E+2
		Measurement processing method (Cycle)		Repeat
		Measurement result data display (Current)		ON
		Known data processing method (Calculation)		Progressive
		Known data display update cycle		100 ms
	Re-synchronization (Auto Sync)	Re-synchronization execution		ON
		Threshold for automatic synchronization function		INT
	SKP Ordered Set filter (SKP Ordered Set)	Filtering		OFF
		Specification		PCIe4
	Synchronization method (Sync Control)	Synchronization method		Invalid
		Unique pattern length for frame synchronization		64 bits
		PRGM pattern start position		1 bit
		Edit of synchronization mask pattern		All 0
	Measurement Condition (Error/Alarm Condition)	Bit error, alarm measurement processing method		Insertion/Omission
		Interval for EI and EFI measurements		100 ms

Table B.1-2 List of MU195040A Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Pattern*	Mask	Block Window execution		OFF
		Block Window setting		All 0
		Bit Window execution		OFF
		Bit Window bit string setting		All 0
		External Mask ON/OFF		OFF
	HSSB Data	Logic		POS
		Length		32
		Specification		PCIe1
		Scrambler Seed		FFFF
		EIEOS Insertion		OFF
		EIEOS Interval		32

*: Items shared with the pulse pattern generator are omitted.
See Table B.1-1 “List of MU195020A Initialized Items” for details.

Table B.1-2 List of MU195040A Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Input	Data	Input condition		Single-Ended
		Differential type		Independent
		Data/XData selection		Data
		Data input threshold		–0.500 V
		XData input threshold		–0.500 V
		Data input threshold differential type		Data-XData
		Data input threshold differential		0.000 V
		Data input termination setup dialog box display		–
		Data input termination condition		GND
		Data input termination voltage		0.00 V
		CTLE		OFF
	Clock	Selection		External Clock
		Standard for Recovered Clock Bitrate		Variable (MU195040A-x22)
		Recovered Clock Bitrate		28.000 000 Gbit/s (MU195040A-x22)
		Loop Bandwidth		17 MHz (MU195040A-x22)
		The value of division for calculating the Loop Bandwidth		1667 (MU195040A-x22)
		Clock phase unit		mUI
		Clock phase variable (mUI)		0 mUI
		Clock phase variable (ps)		0.00 ps
		Clock phase calibration		–
		Clock phase reference		OFF
		Clock phase variable (reference mUI)		0 mUI
		Clock phase variable (reference ps)		0.00 ps
		Clock phase variable (Jitter Input)		OFF
	Measurement Restart	Data Threshold		OFF
		Clock Delay		OFF

Table B.1-2 List of MU195040A Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Capture	Condition	Number of Block		128
		Trigger		Match Pattern
			Position	Top
		Match Pattern Length		4 bits
		Format		Hex
		Match Pattern		0
		Mask Pattern		0
	Capture Acquisition	Start Block No.		1
		Number of Block		1
	Capture	Block		1
		Viewer Mode	Notation	Hex(Byte)
			Format	Pattern
		Error Search	Continuous Error	≧ 1 bit
Misc1	Pattern Sequence			Repeat
		Burst	Source	External-Enable
			Delay	0 bits
			Auto/Manual	Manual
			Enable Period	128 000 bits*
			Burst Cycle	12 800 000 bits*
	Aux Input			External Mask
			Vth	0 V
	Aux Output			1/N Clock
		1/N Clock	(Divide ratio)	1/64 clock
		Pattern Sync	For PRBS, Zero-Substitution, Data Position	 1 bits
			For Mixed Data Block No. Row No.	 1 1

*: 2ch Combination: Default × 2

Table B.1-3 List of MU195050A Initialized Items

Setting Function	Item	Default Setting
Common Mode Noise	Presets	Manual
	Output	OFF
	Amplitude	10 mVp-p
	Frequency	100 MHz
	Band	Low
Differential Mode Noise	Presets	Manual
	Output	OFF
	Amplitude	4 mVp-p
	Frequency	2 GHz
White Noise	Output	OFF
	Amplitude	0.2 mVrms
External Input	Output	OFF